

## CRD89C51R

8-bit microcontroller with 4KB Flash and 256B RAM

### Product List

CRD89L51R-25, 3V, 25MHz, 4KB Flash 256B RAM  
CRD89C51R-25, 5V, 25MHz, 4KB Flash 256B RAM  
CRD89C51R-40, 5V, 40MHz, 4KB Flash 256B RAM

### Description

The CRD89C51R series product is an 8-bit single chip micro controller with 4 KB flash embedded. It provides hard-ware features and a powerful instruction set, necessary to make it a versatile and cost effective controller for those applications demand up to 32 I/O pins or need up to 4 KB flash memory either for program or for data or mixed. The flash can be programmed by a commercial programmer.

### Ordering Information

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**CRD89C51R-40-QG**

4KB Flash, 40 MHz, 5V, 44 QFP

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**CRD89C51R-40-LG**

4KB Flash, 40 MHz, 5V, 44 PLCC

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**CRD89C51R-40-PG**

4KB Flash, 40 MHz, 5V, 40 PDIP

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**CRD89L51R-25-QG**

4KB Flash, 25 MHz, 3V, 44 QFP

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**CRD89L51R-25-LG**

4KB Flash, 25 MHz, 3V, 44 PLCC

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**CRD89L51R-25-PG**

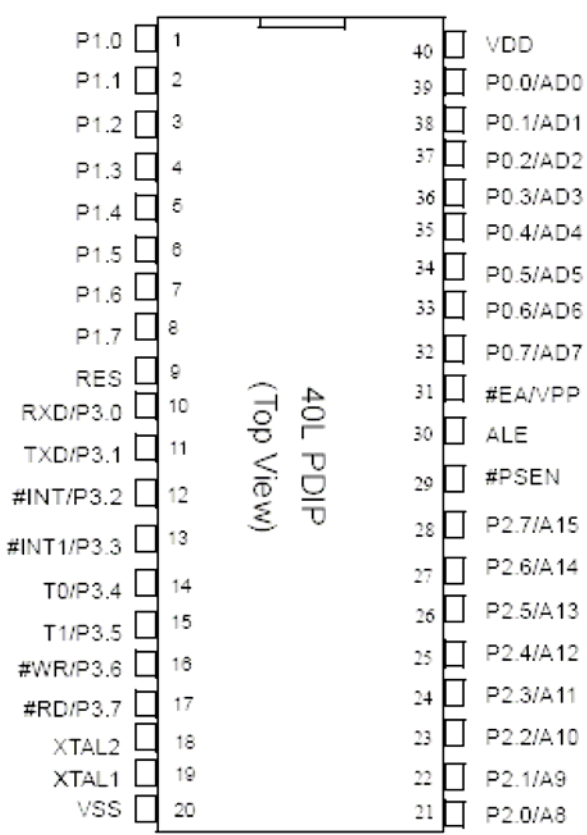
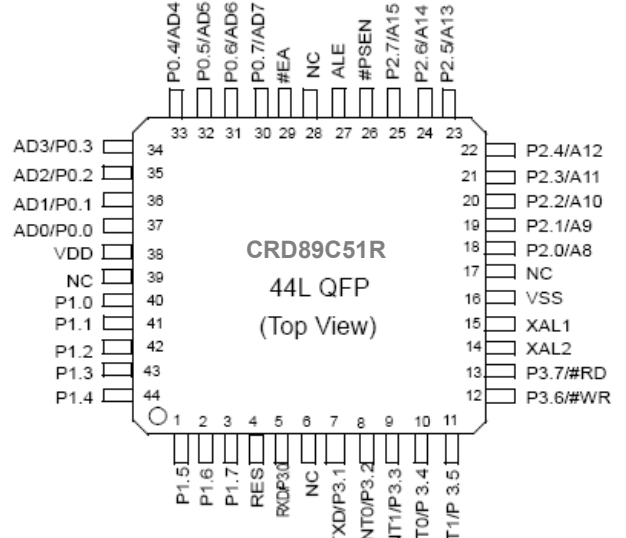
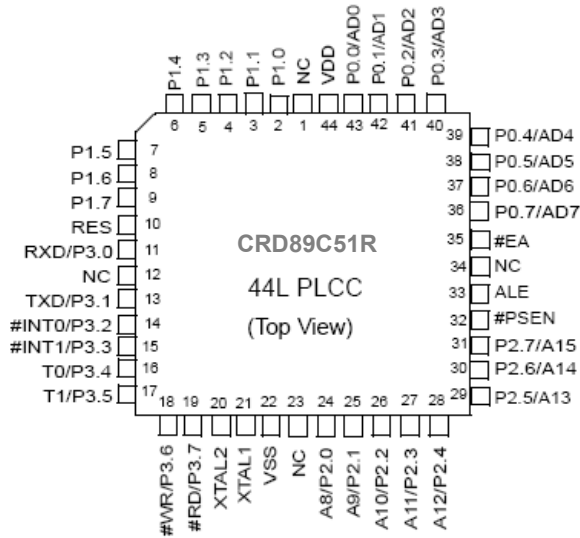
4KB Flash, 25 MHz, 3V, 40 PDIP

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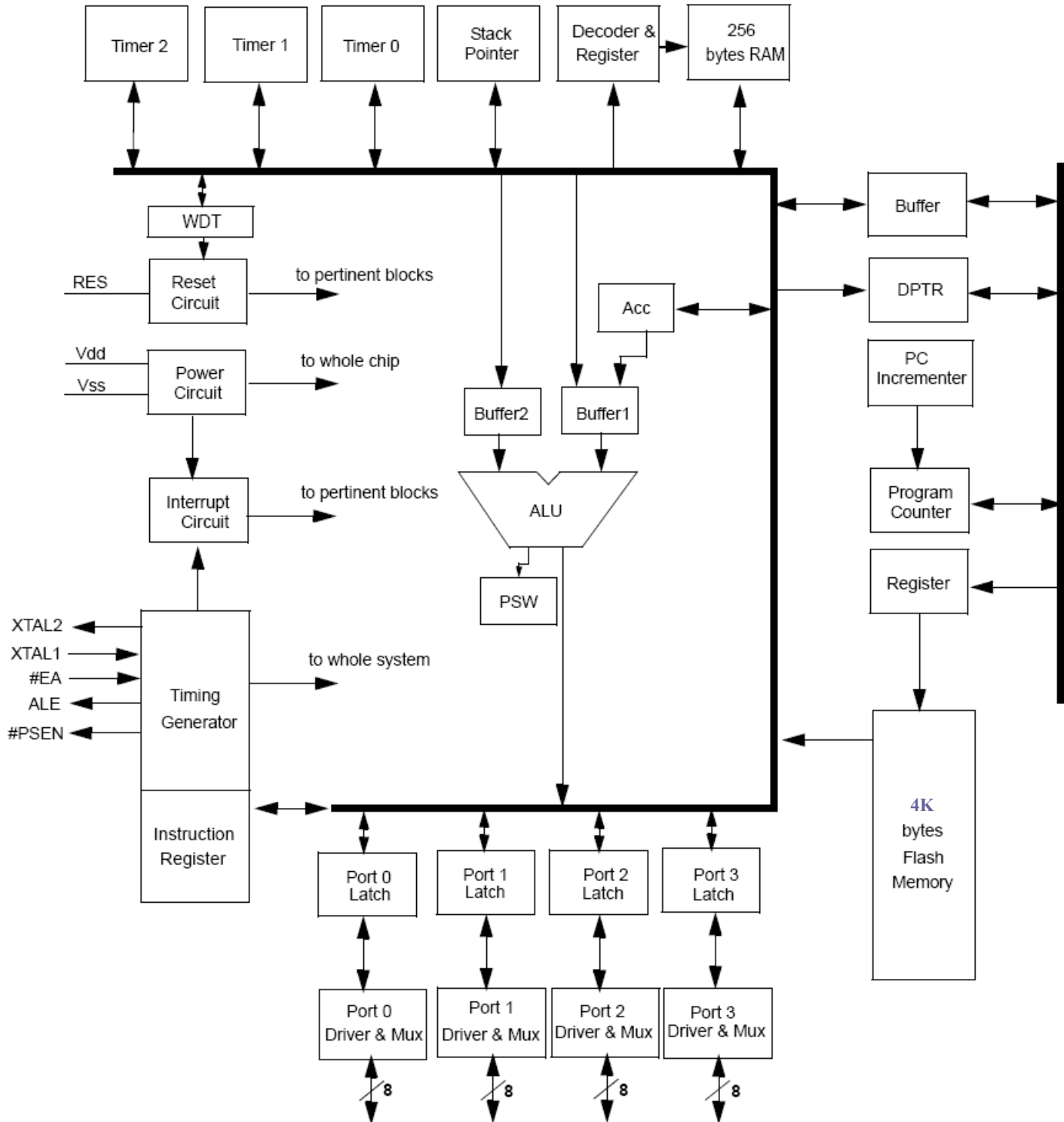
### Features

- Working Voltage: 3.0V ~ 3.6V L Version  
4.5V ~ 5.5V C Version
- General 8052 family compatible
- 12 clocks per machine cycle
- 4K internal flash memory
- 256 bytes data RAM
- 2 16 bit timers/counters
- Four 8-bit I/O ports
- Full duplex serial channel
- Bit operation instruction
- Industrial temperature level
- 8-bit unsigned division
- 8-bit unsigned multiply
- BCD arithmetic
- Direct addressing
- Indirect addressing
- Nested interrupt
- Two priority level interrupt
- A serial I/O port
- Power save modes:  
Idle mode and Power down mode
- Code protection function
- One watch dog timer(WDT)
- Low EMI (inhibit ALE)

**Pin Configuration**



**Block Diagram**



## Pin Description

40L PDIP Pin#	44L QFP Pin#	44L PLCC Pin#	Symbol	Active	I/O	Names
1	40	2	P1.0		i/o	bit 0 of port 1
2	41	3	P1.1		i/o	bit 1 of port 1
3	42	4	P1.2		i/o	bit 2 of port 1
4	43	5	P1.3		i/o	bit 3 of port 1
5	44	6	P1.4		i/o	bit 4 of port 1
6	1	7	P1.5		i/o	bit 5 of port 1
7	2	8	P1.6		i/o	bit 6 of port 1
8	3	9	P1.7		i/o	bit 7 of port 1
9	4	10	RES	H	i	Reset
10	5	11	P3.0/RXD		i/o	bit 0 of port 3 & Receiver data
11	7	13	P3.1/TXD		i/o	bit 1 of port 3 & Transmit data
12	8	14	P3.2/#INT0	L/-	i/o	bit 2 of port 3 & low true interrupt 0
13	9	15	P3.3/#INT1	L/-	i/o	bit 3 of port 3 & low true interrupt 1
14	10	16	P3.4/T0		i/o	bit 4 of port 3 & Timer 0
15	11	17	P3.5/T1		i/o	bit 5 of port 3 & Timer 1
16	12	18	P3.6/#WR	L/-	i/o	bit 6 of port 3 & external memory write
17	13	19	P3.7/#RD	L/-	i/o	bit 7 of port 3 & external memory Read
18	14	20	XTAL2		o	Crystal out
19	15	21	XTAL1		i	Crystal in
20	16	22	VSS			Sink Voltage, Ground
21	18	24	P2.0/A8		i/o	bit 0 of port 2 & bit 8 of external memory address
22	19	25	P2.1/A9		i/o	bit 1 of port 2 & bit 9 of external memory address
23	20	26	P2.2/A10		i/o	bit 2 of port 2 & bit 10 of external memory address
24	21	27	P2.3/A11		i/o	bit 3 of port 2 & bit 11 of external memory address
25	22	28	P2.4/A12		i/o	bit 4 of port 2 & bit 12 of external memory address
26	23	29	P2.5/A13		i/o	bit 5 of port 2 & bit 13 of external memory address
27	24	30	P2.6/A14		i/o	bit 6 of port 2 & bit 14 of external memory address
28	25	31	P2.7/A15		i/o	bit 7 of port 2 & bit 15 of external memory address
29	26	32	#PSEN	L	o	program storage enable
30	27	33	ALE	-	o	address latch enable
31	29	35	#EA	L	i	external access
32	30	36	P0.7/AD7		i/o	bit 7 of port 0 & data/address bit 7 of external memory
33	31	37	P0.6/AD6		i/o	bit 6 of port 0 & data/address bit 6 of external memory
34	32	38	P0.5/AD5		i/o	bit 5 of port 0 & data/address bit 5 of external memory
35	33	39	P0.4/AD4		i/o	bit 4 of port 0 & data/address bit 4 of external memory
36	34	40	P0.3/AD3		i/o	bit 3 of port 0 & data/address bit 3 of external memory
37	35	41	P0.2/AD2		i/o	bit 2 of port 0 & data/address bit 2 of external memory
38	36	42	P0.1/AD1		i/o	bit 1 of port 0 & data/address bit 1 of external memory
39	37	43	P0.0/AD0		i/o	bit 0 of port 0 & data/address bit 0 of external memory
40	38	44	VDD			Drive Voltage, +5 Vcc

## SFR Memory Map

\$F8								\$FF
\$F0	<b>B</b>							\$F7
\$E8								\$EF
\$E0	<b>ACC</b>							\$E7
\$D8								\$DF
\$D0	<b>PSW</b>							\$D7
\$C8	<b>T2CON</b>		<b>RC2L</b>	<b>RC2H</b>	<b>TL2</b>	<b>TH2</b>		\$CF
\$C0								\$C7
\$B8	<b>IP</b>						<b>SCONF</b>	\$BF
\$B0	<b>P3</b>							\$B7
\$A8	<b>IE</b>							\$AF
\$A0	<b>P2</b>							\$A7
\$98	<b>SCON</b>	<b>SBUF</b>					<b>WDTC</b>	\$9F
\$90	<b>P1</b>							\$97
\$88	<b>TCON</b>	<b>TMOD</b>	<b>TL0</b>	<b>TL1</b>	<b>TH0</b>	<b>TH1</b>		\$8F
\$80	<b>P0</b>	<b>SP</b>	<b>DPL</b>	<b>DPH</b>			<b>PCON</b>	\$87

Note: The text of SFRs with bold type characters are Extension Special Function Registers for CRD89C51R

## Functional Description

### Watch Dog Timer

The Watch Dog Timer (WDT) is a 16-bit free-running counter that generate reset signal if the counter overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electronics discharge which causing software dead loop or runaway. The WDT function can help user software recover from abnormal software condition. The WDT is different from Timer0, Timer1 and Timer2 of general 8052. To prevent a WDT reset can be done by software periodically clearing the WDT counter.

The CRD89C51R WDT has selectable divider input for the time base source clock. To select the divider input, the setting of bit2~bit0 (PS2~PS0) OF Watch Dog Timer Control Register (WDTC) should be set accordingly.

To enable the WDT is done by setting 1 to the bit 7 (WDTE) of WDTC. After WDTE set to 1, the 16-bit counter starts to count with the RC oscillator. It will generate a reset signal when overflows. The WDTE bit will be cleared to 0 automatically when CRD89C51R been reset, either hardware reset or WDT reset.

To reset the WDT is done by setting 1 to the CLEAR bit of WDTC before the counter overflow. This will clear the content of the 16-bit counter and let the counter re-start to count from the beginning.

**Watch Dog Timer Registers - WDT Control Register (WDTC, \$9F)**

	WDTE	R	Clear	Unused	Unused	PS2	PS1	PS0
Read / Write:	R/W	-	-	-	-	R/W	R/W	R/W
Reset value:	0	*	0	*	*	0	0	0
	MSB				LSB			

WDTE: Watch Dog Timer enable bit

CLEAR: Watch Dog Timer reset bit

If CLEAR bit set to 1, Watch Dog Timer will be reset. The user doesn't reset the value to 0.

PS2~PS0: clock source divider bit

PS [2:0]	Divider (OSC in)	Time Period (ms) @40MHZ
000	8	13.1
001	16	26.21
010	32	52.42
011	64	104.8
100	128	209.71
101	256	419.43
110	512	838.86
111	1024	1677.72

**Watch Dog Timer Register - System Control Register (SCONF, \$BFH)**

	bit-7						bit-0
	WDR	Unused	Unused	Unused	Unused	Unused	ALEI
Read / Write:	R/W	-	-	-	-	-	R/W
Reset value:	0	*	*	*	*	*	0

WDR: Watch Dog Timer Reset. When system reset by Watch Dog Timer overflow, WDR will be set to 1

ALEI: ALE output inhibit bit, to reduce EMI

The bit 7(WDR) of SCONF is Watch Dog Timer Reset bit. It will be set to 1 when reset signal generated by WDT overflow. User should check WDR bit whenever un-predicted reset happened.

## Reduced EMI Function

The CRD89C51R allows users to reduce the EMI emission by setting 1 to the bit 0 (ALE) of SCONF register. This function will inhibit the clock signal in Fosc/6Hz output to the ALE pin. This function is available when there is no external program memory or no external data RAM in the system.

## Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	°C	Ambient temperature under bias
VCC5	Supply voltage	4.5	5.0	5.5	V	For C Version
VCC3	Supply voltage	3	3.3	3.6	V	For L Version
Fosc 25	Oscillator Frequency	3.0	25	25	MHz	For 5V, 3.3V application
Fosc 40	Oscillator Frequency	3.0	40	40	MHz	For 5V application

## DC Characteristics

(TA = -40 degree C to 85 degree C, Vcc = 3.0V to 5.5V)

Symbol	Parameter	Valid	Min.	Max.	Unit	Test Conditions
VIL1	Input Low Voltage	port 0,1,2,3,#EA	-0.5	0.8	V	
VIL2	Input Low Voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High Voltage	port 0,1,2,3,#EA	2.0	Vcc+0.5	V	
VIH2	Input High Voltage	RES, XTAL1	70%Vcc	Vcc+0.5	V	
VOL1	Output Low Voltage	port 0, ALE, #PSEN		0.45	V	IOL=8mA (5V) / IOL=6mA (3.3V)
VOL2	Output Low Voltage	port 1,2,3		0.45	V	IOL=6.5mA (5V) / IOL=5mA (3.3V)
VOH1	Output High Voltage	port 0	2.4		V	IOH=-800uA (only for VCC =5V)
			90%Vcc		V	IOH=-80uA
VOH2	Output High Voltage	port 1,2,3,ALE,#PSEN	2.4		V	IOH=-60uA (only for VCC =5 V)
			90%Vcc		V	IOH=-10uA
IIL	Logical 0 Input Current	port 1,2,3,4		-75	uA	Vin=0.45V
ITL	Logical Transition Current	port 1,2,3,4		-650	uA	Vin=2.0V
ILI	Input Leakage Current	port 0, #EA		±10	uA	0.45V<Vin<Vcc
R RES	Reset Pull-down Resistance	RES	50	300	Kohm	
C IO	Pin Capacitance			10	pF	Freq=1MHz, Ta=25 °C
I CC	Power Supply Current	Vdd		20	mA	Active mode, 16MHz
				6.5	mA	Idle mode, 16MHz
				50	uA	Power down mode

Note1: Under steady state (non-transient) conditions, IOL must be externally limited as follows:

Maximum IOL per port pin: 10mA

Maximum IOL per 8-bit port: port 0:26mA port 1,2,3: 15mA

Maximum total IOL for all output pins: 71mA

If IOL exceeds these conditions, VOL may exceed the related specification. Pins are not guaranteed to sink current greater than the listed test conditions.

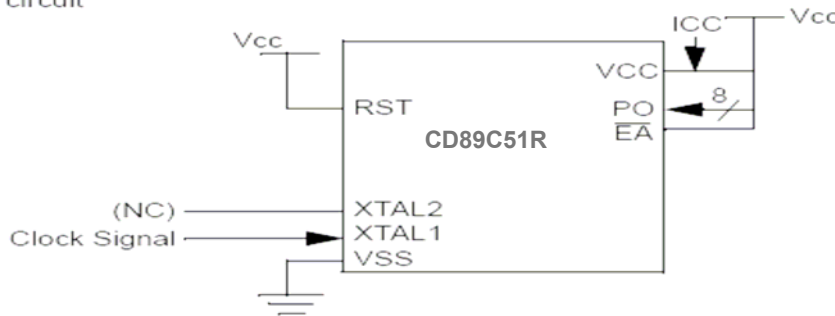
Note2: Minimum VCC for Power-down is 2V.

**AC Characteristics**

(16/25/40MHz, operating conditions; CL for Port 0, ALE and PSEN Outputs=100pF; CL for all Other Output=80pF)

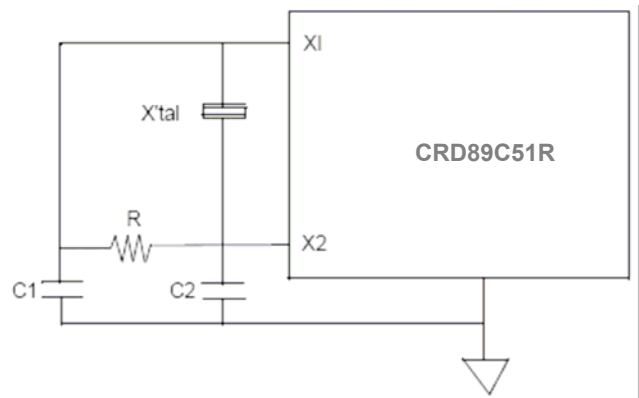
Symbol	Parameter	Valid Cycle	f <sub>osc</sub> =16MHz			Variable f <sub>osc</sub>			Unit	Remarks
			Min	T <sub>vp</sub>	Max	Min	T <sub>vp</sub>	Max		
T <sub>THI</sub>	ALE pulse width	RD/WRT	115			2xT - 10			nS	
T <sub>AVI</sub>	Address Valid to ALE low	RD/WRT	43			T - 20			nS	
T <sub>HA</sub>	Address Hold after ALE low	RD/WRT	53			T - 10			nS	
T <sub>ILV</sub>	ALE low to Valid Instruction In	RD			240			4xT-10	nS	
T <sub>ILP</sub>	ALE low to #PSEN low	RD	53			T - 10			nS	
T <sub>PIPH</sub>	#PSEN pulse width	RD	173			3xT - 15			nS	
T <sub>PIV</sub>	#PSEN low to Valid Instruction In	RD			177			3xT-10	nS	
T <sub>PXIX</sub>	Instruction Hold after #PSEN	RD	0			0			nS	
T <sub>PXIZ</sub>	Instruction Float after #PSEN	RD			87			T+25	nS	
T <sub>AVIV</sub>	Address to Valid Instruction In	RD			292			5xT-20	nS	
T <sub>PIA7</sub>	#PSEN low to Address Float	RD			10			10	nS	
T <sub>RI RH</sub>	#RD pulse width	RD	365			6xT - 10			nS	
T <sub>WI WH</sub>	#WR pulse width	WRT	365			6xT - 10			nS	
T <sub>RI DV</sub>	#RD low to Valid Data In	RD			302			5xT-10	nS	
T <sub>RHD</sub>	Data Hold after #RD	RD	0			0			nS	
T <sub>RHD7</sub>	Data Float after #RD	RD			145			2xT+20	nS	
T <sub>IL DV</sub>	ALE low to Valid Data In	RD			590			8xT-10	nS	
T <sub>AVDV</sub>	Address to Valid Data In	RD			542			9xT-20	nS	
T <sub>IL YI</sub>	ALE low to #WR High or #RD low	RD/WRT	178		197	3xT - 10		3xT+10	nS	
T <sub>AVYI</sub>	Address Valid to #WR or #RD low	RD/WRT	230			4xT - 20			nS	
T <sub>QVWH</sub>	Data Valid to #WR High	WRT	403			7xT - 35			nS	
T <sub>QVWX</sub>	Data Valid to #WR transition	WRT	38			T - 25			nS	
T <sub>WHOX</sub>	Data hold after #WR	WRT	73			T + 10			nS	
T <sub>RIA7</sub>	#RD low to Address Float	RD						5	nS	
T <sub>YAIH</sub>	#WR or #RD high to ALE high	RD/WRT	53		72	T - 10		T+10	nS	
T <sub>CHCI</sub>	clock fall time								nS	
T <sub>CLCX</sub>	clock low time								nS	
T <sub>CLCH</sub>	clock rise time								nS	
T <sub>CHCX</sub>	clock high time								nS	
T <sub>TCICI</sub>	clock period			63			1/f <sub>osc</sub>		nS	

ICC Active mode test circuit



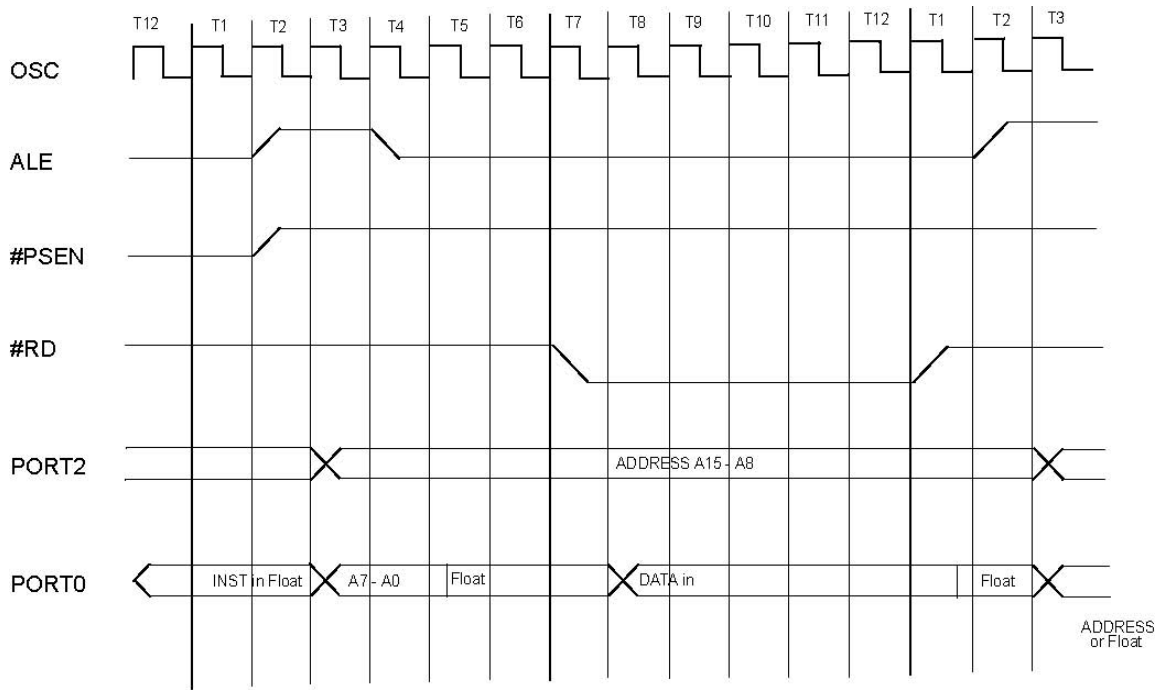
Application Reference

Valid for CRD89C51R				
X'tal	3MHz	6MHz	9MHz	12MHz
C1	30 pF	30 pF	30 pF	30 pF
C2	30 pF	30 pF	30 pF	30 pF
R	open	open	open	Open
X'tal	16MHz	25MHz	33MHz	40MHz
C1	30 pF	15 pF	5 pF	2 pF
C2	30 pF	15 pF	5 pF	2 pF
R	open	62KΩ	6.8KΩ	4.7KΩ

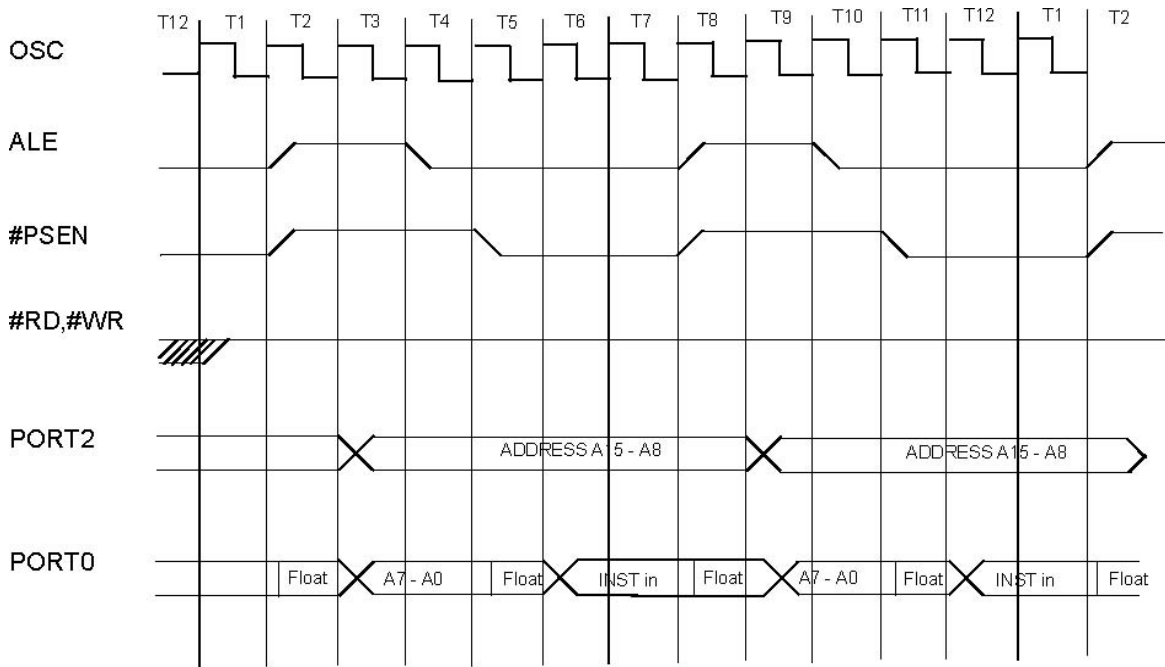


NOTE: Oscillation circuit performance may differ with different crystal or ceramic resonators using higher oscillation frequencies since each crystal or ceramic resonator has its own characteristics. User should check with the crystal or ceramic resonator manufacturer for appropriate value of external components.

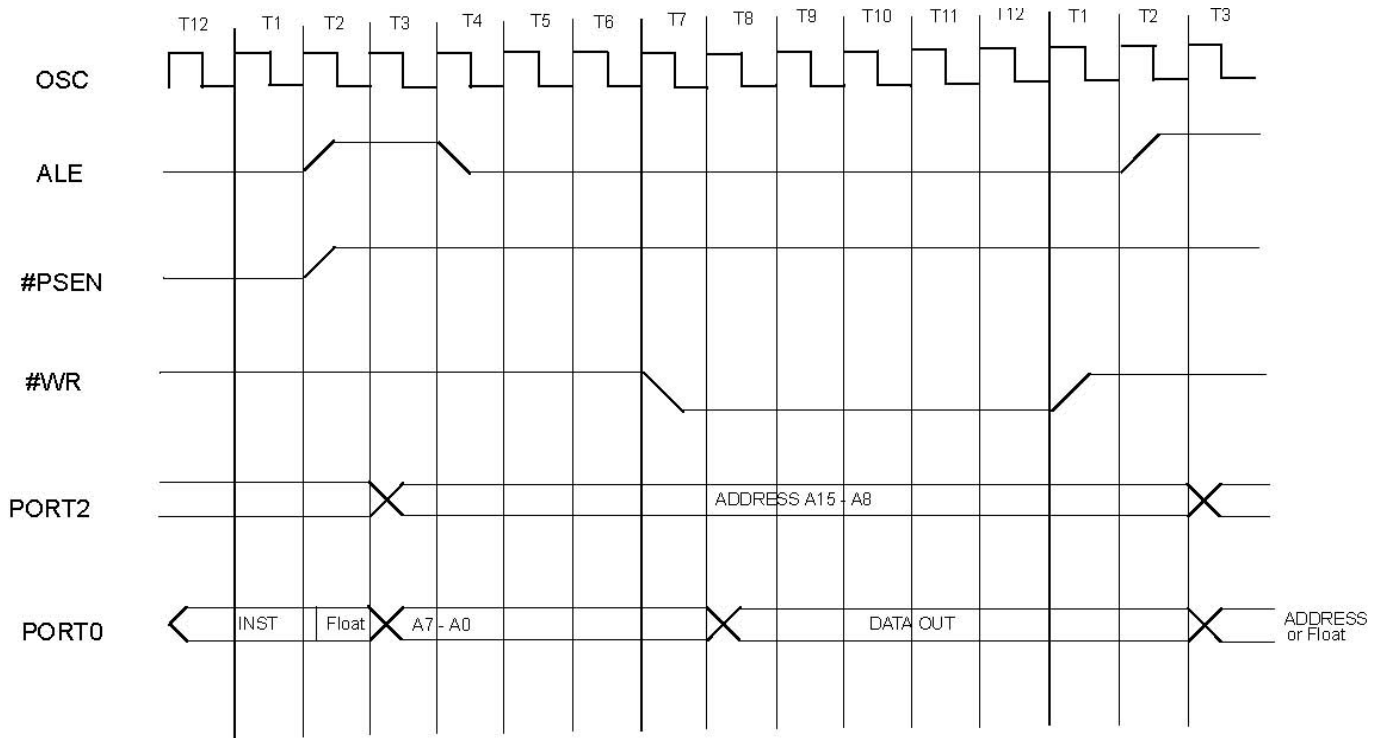
Data Memory Read Cycle Timing



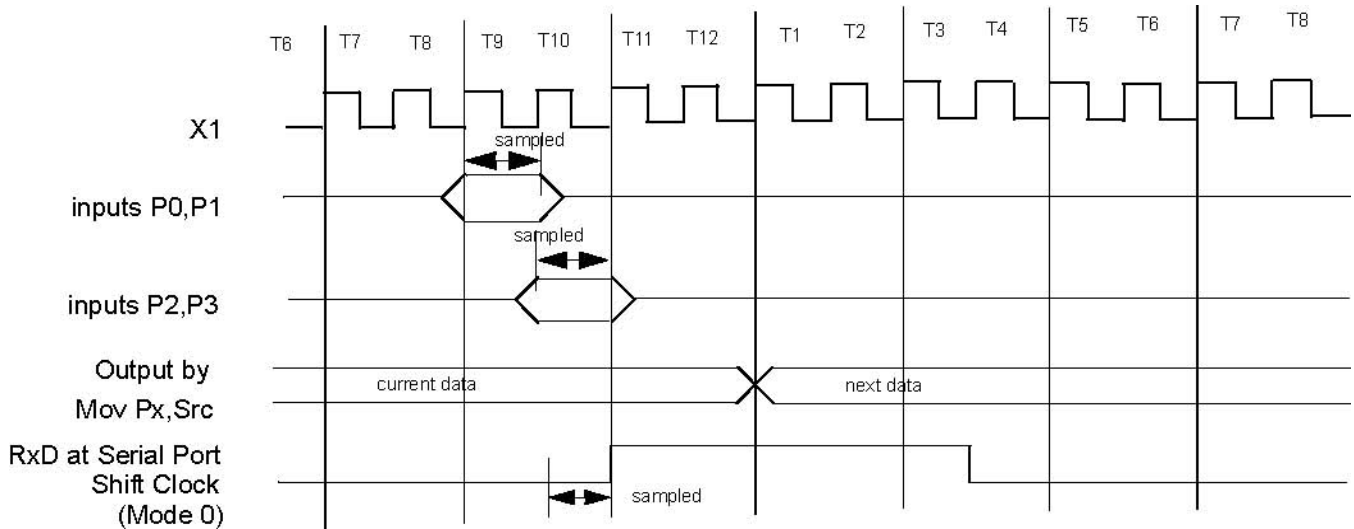
Program Memory Read Cycle Timing



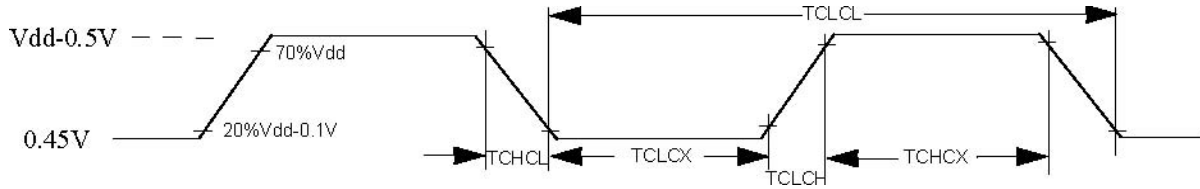
Data Memory Write Cycle Timing



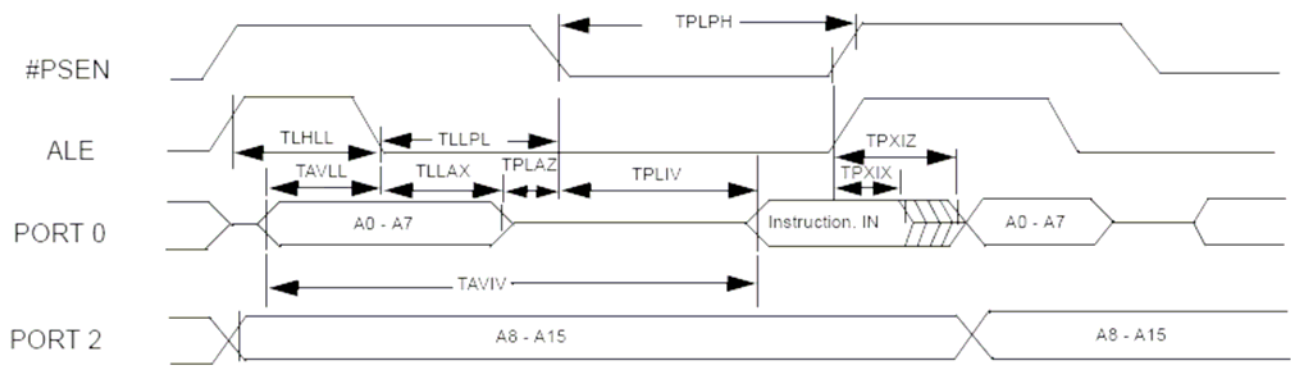
I/O Ports Timing



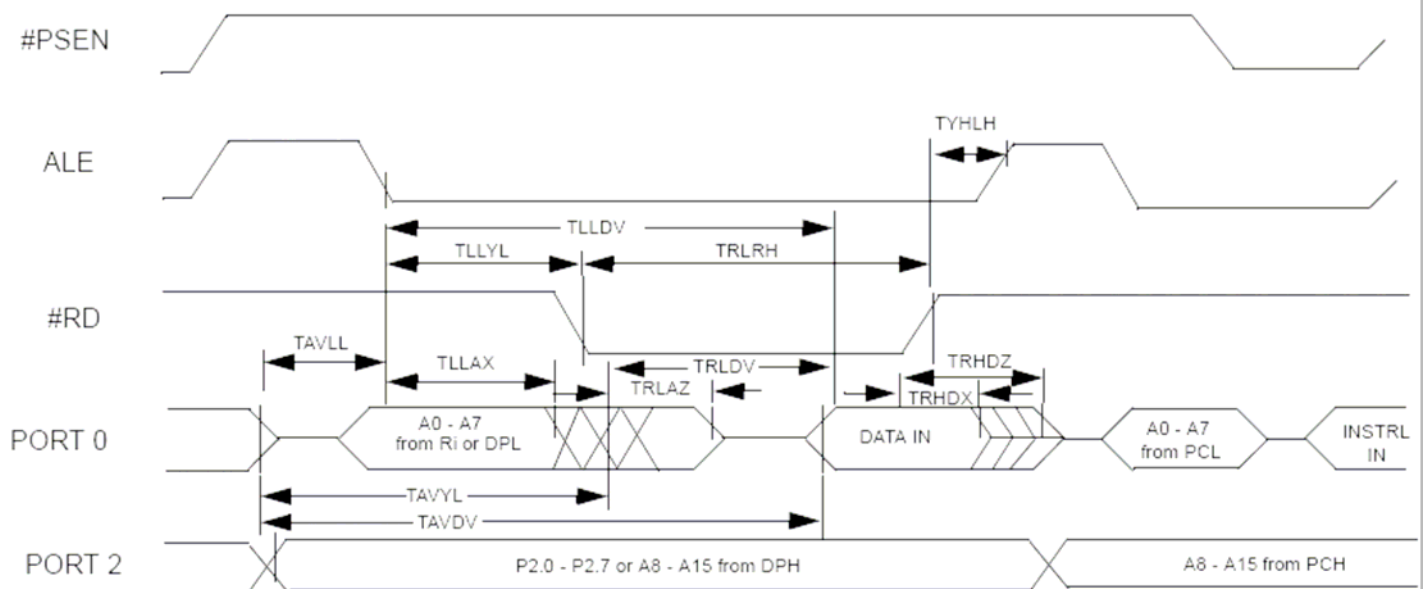
Timing Critical, Requirement of External Clock (Vss=0.0V is assumed)



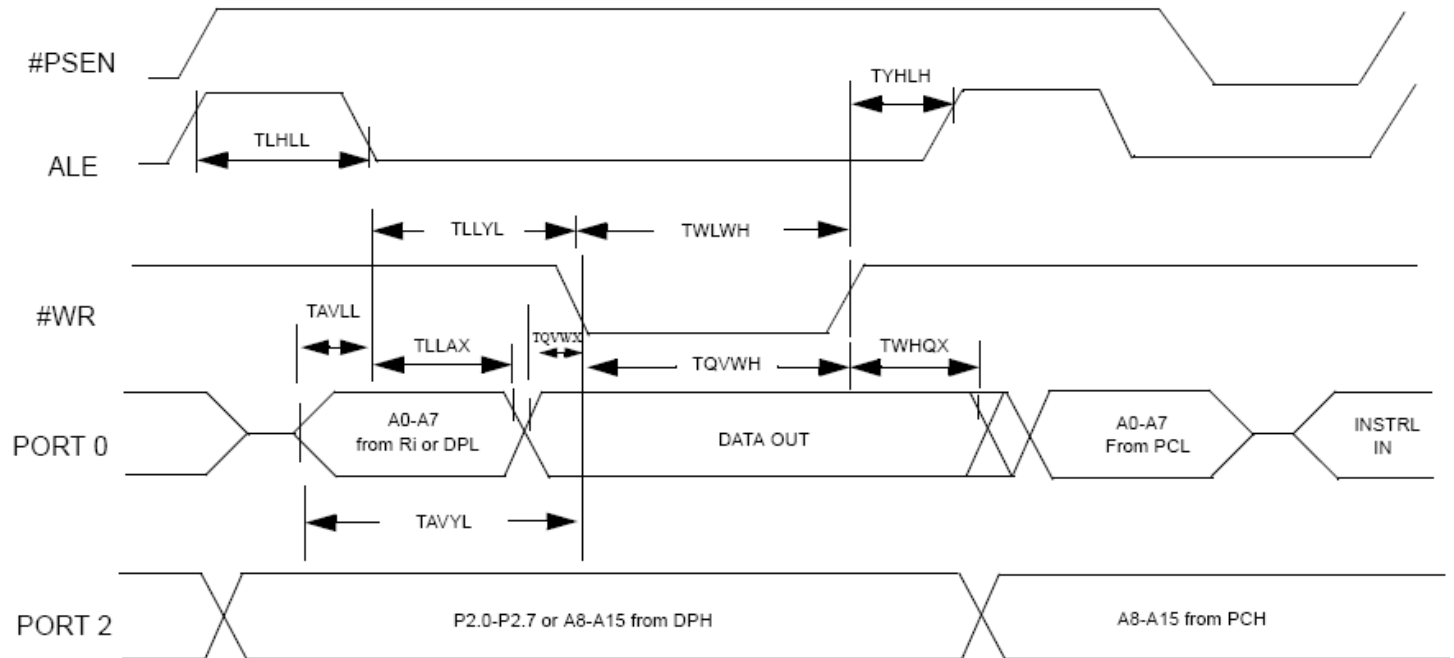
**Tm.I External Program Memory Read Cycle**



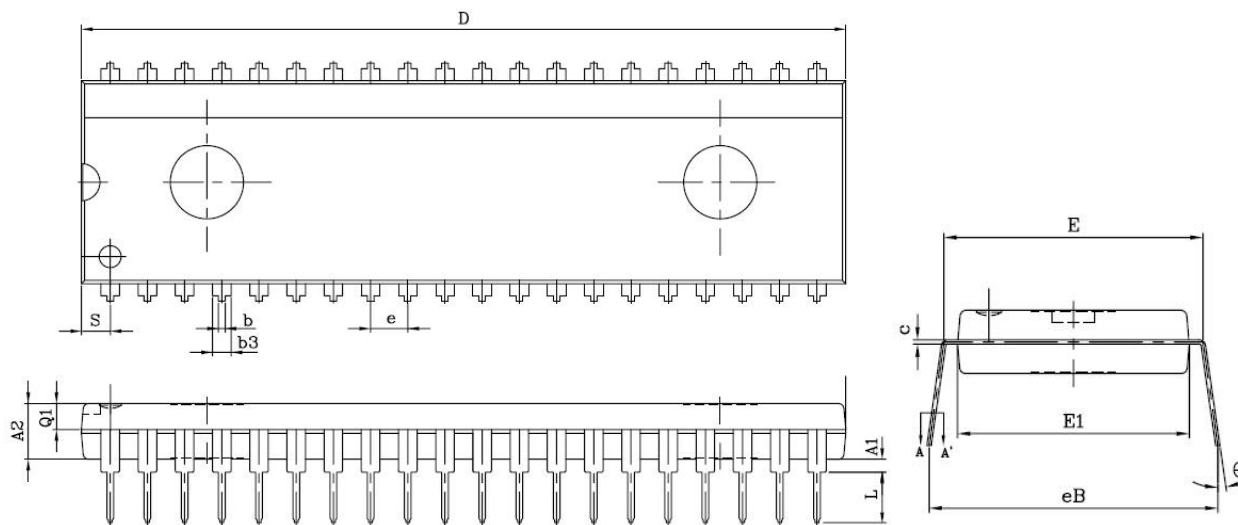
**Tm.II External Data Memory Read Cycle**

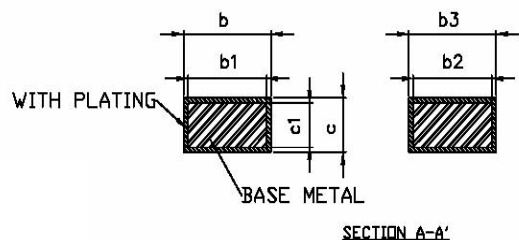


Tm.III External Data Memory Write Cycle



**PDIP 40L (600mil) Package Information :**



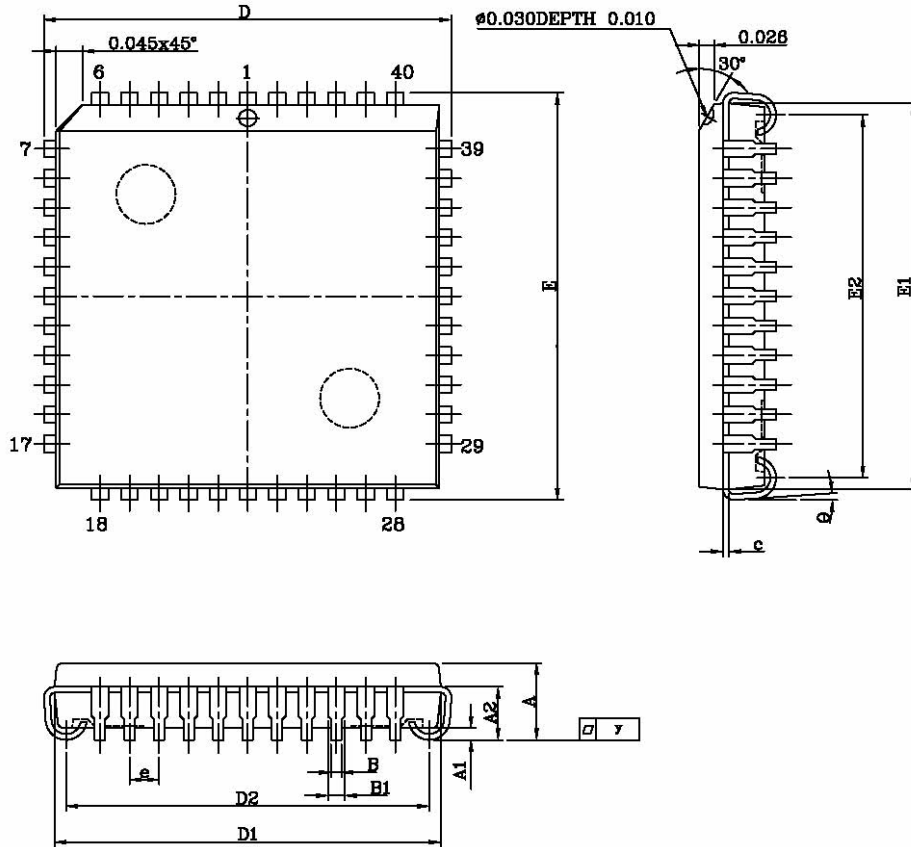


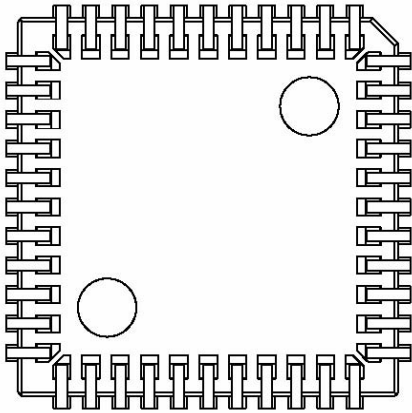
Note:

1. Refer to JEDEC STD.MS-011(AC).
2. Dimension D and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D and E1 are maximum plastic body size dimension include mold mismatch.
3. Dimension b3 does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.2mm.

Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
<b>A1</b>	0.254	—	—	10	—	—
<b>A2</b>	3.683	3.810	3.937	145	150	155
<b>b</b>	0.356	0.500	0.660	14	20	26
<b>b1</b>	0.356	0.457	0.508	14	18	22
<b>b2</b>	1.016	1.270	1.524	40	50	60
<b>b3</b>	1.016	1.321	1.626	40	52	64
<b>c</b>	0.203	0.254	0.432	8	10	17
<b>c1</b>	0.203	0.254	0.356	8	10	14
<b>D</b>	52.07	52.2	52.32	2050	2055	2060
<b>E</b>	14.99	15.24	15.49	590	600	610
<b>E1</b>	13.69	13.87	13.94	539	546	549
<b>e</b>	—	2.540	—	—	100	—
<b>eB</b>	15.75	16.26	16.76	620	640	660
<b>L</b>	2.921	3.302	3.683	115	130	145
<b>S</b>	1.727	1.981	2.235	68	78	88
<b>Q1</b>	1.651	1.778	1.905	65	70	75
<b>θ</b>	0°	—	10°	0°	—	10°

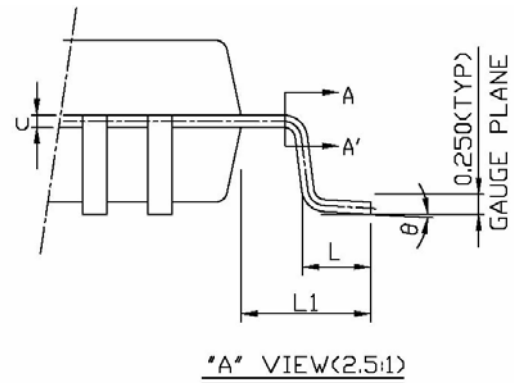
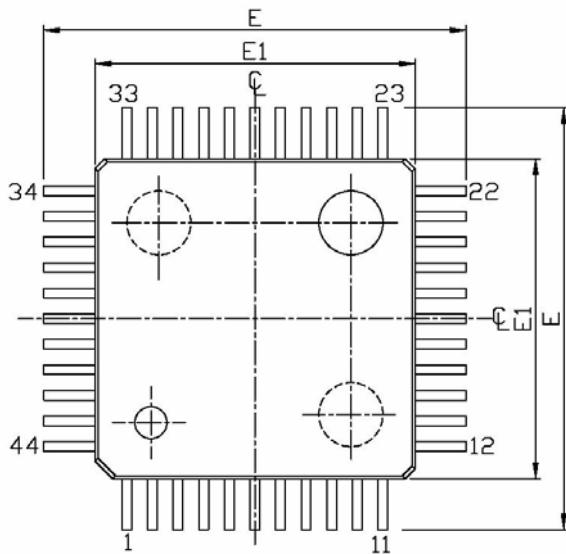
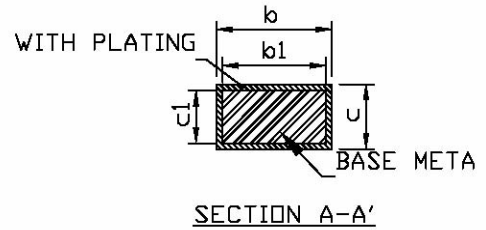
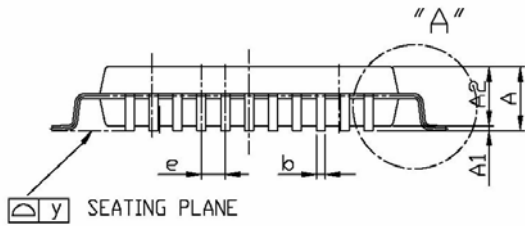
**PLCC 44L Package Information :**





UNIT SYMBOL	INCH(REF)	MM(BASE)
<b>A</b>	0.180(MAX)	4.572(MAX)
<b>A1</b>	0.024 ±0.005	0.52 ±0.14
<b>A2</b>	0.105 ±0.005	2.667 ±0.127
<b>B</b>	0.018 + 0.004 - 0.002	0.457 + 0.102 - 0.051
<b>B1</b>	0.028 + 0.004 - 0.002	0.711 + 0.102 - 0.051
<b>c</b>	0.010(TYP)	0.254(TYP)
<b>D</b>	0.690 ±0.010	17.526 ±0.254
<b>D1</b>	0.653 ±0.003	16.586 ±0.076
<b>D2</b>	0.610 ±0.020	15.494 ±0.508
<b>E</b>	0.690 ±0.010	17.526 ±0.254
<b>E1</b>	0.653 ±0.003	16.586 ±0.076
<b>E2</b>	0.610 ±0.010	15.494 ±0.254
<b>e</b>	0.050(TYP)	1.270(TYP)
<b>y</b>	0.003(MAX)	0.076(MAX)
<b>θ</b>	0~5°	0~5°

**QFP 44L(10x10x2.0mm) Package Information :**



Symbol	Dimension in mm			Dimension in MIL		
	Min	Nom	Max	Min	Nom	Max
<b>A</b>	—	—	2.45	—	—	964
<b>A1</b>	0.05	0.15	0.25	2.1	6.0	9.6
<b>A2</b>	1.90	2.00	2.10	74.8	78.7	82.7
<b>b</b>	0.29	0.32	0.45	11.4	12.6	17.7
<b>b1</b>	0.29	0.30	0.41	11.4	11.8	16.1
<b>c</b>	0.11	0.17	0.23	4.3	6.7	9.1
<b>c1</b>	0.11	0.15	0.19	4.3	5.9	7.5
<b>E</b>	13.00	13.20	13.40	512	520	528
<b>E1</b>	9.90	10.00	10.10	390	394	398
<b>[e]</b>	—	0.800	—	—	31.5	—
<b>L</b>	0.73	0.88	1.03	28.7	34.6	40.6
<b>L1</b>	1.50	1.60	1.70	59.1	63.0	66.9
<b>y</b>	—	—	0.076	—	—	3
<b>θ</b>	0°	—	7°	0°	—	7°

Note:

1. Refer to JEDC STD.MS-022(AB).
2. Dimension E1 do not include mold protrusion. Allowable protrusion is 0.25mm per side.E1 are maximum plastic body size dimension include mold mismatch .
3. Dimension b does not include dambar protrusion .Allowable dambar protrusion shall not cause the lead width to exceed the maximum b3 dimension by more than 0.1 mm.