Cyrod
Technologies Inc.

CRD89C51AB1TB

Data Sheet Rev 1.00

CRD89C51AB1TB

8 bit, fast, microcontroller with 16KB program/ISP Flash and 1KB RAM

Product List

CRD89C51AB1TB-25, 5V 25MHz Flash MCU
CRD89L51AB1TB-25, 3V 25MHz Flash MCU

Description

The CRD89C51AB1TB series product is an 8-bit single chip microcontroller with 16K bytes Flash and 1K byte RAM. It is a high speed derivative of the 8052 micro-controller family, offering an 8 times improvement over the standard 8052. Its instruction set is fully compatible to the 8052 instruction set. It can be programmed either through the ISP bootloader, or through an external programmer. The unused part of the flash area, can be used as EEPROM. After programming, the code can be protected to prevent illegal read, or write. It provides peripherals that can make many applications more efficient, such as dual DPTR, UART, watchdog timer, Low Voltage Reset, PWM module, capture and compare Timers, PCA, ADC, MDU and EEI. These are functionally compatible with peripherals available in all popular 8052 derivatives. Power saving modes (Idle, Stop) and low EMI characteristics combine to the above characteristics to form a powerful microcontroller.

Ordering Information

CRD89C51AB1TB-25-PG	25MHz, PDIP, 4.5V~5.5V
CRD89C51AB1TB-25-LG	25MHz, PLCC, 4.5V~5.5V
CRD89C51AB1TB-25-QG	25MHz, PQFP, 4.5V~5.5V
CRD89C51AB1TB-25-VG	25MHz, LQFP, 4.5V~5.5V
CRD89L51AB1TB-25-PG	25MHz, PDIP, 2.7V~3.6V
CRD89L51AB1TB-25-LG	25MHz, PLCC, 2.7V~3.6V
CRD89L51AB1TB-25-QG	25MHz, PQFP, 2.7V~3.6V
CRD89L51AB1TB-25-VG	25MHz, LQFP, 2.7V~3.6V

Features

- Operating Voltage: 2.7V ~ 3.6V or 4.5V ~ 5.5V
- General 8052 family compatibility
- 1 clock per machine cycle
- Frequency runs up to 25MHz
- 16K bytes on chip flash memory with In-System Programming and EEPROM capability
- 1K Bytes on-chip expanded RAM
- 256 Bytes for standard 8052 RAM
- Fully compatible instruction set
- External RAM address up to 64KB
- Dual 16-bit Data Pointers
- One full duplex, UART
- Three 16 bit Timers/Counters
- 36GPIOs (PDIP40),40GPIOs (PLCC44/QFP44), 44GPIOs (LQFP48)
- GPIO modes: quasi bidirectional, push-pull, open-drain
- External Interrupt 0,1 with two priority levels
- Programmable Watchdog Timer (WDT)
- One IIC (master/slave) interface
- One SPI (master/slave) interface
- 4-channel PWM
- 4-channel 16-bit compare/capture/load functions
- 8-channel 10-bit ADC
- Fast multiplication-division unit (MDU): 16*16, 32/16, 16/16, 32bit L/R shifting and 32bit normalization
- ISP/IAP/ICP functions
- ISP service program space configurable in N*512 byte (N=0 to 8) size for IAP application
- on chip ICE & OCD
- ALE output select for low EMI
- Expanded External Interrupt (EEI) interface for eight more external interrupts.
- LVI/LVR (LVR deglitch 500ns)
- Power Management (IDLE & STOP mode)
- Enhanced Code protection function

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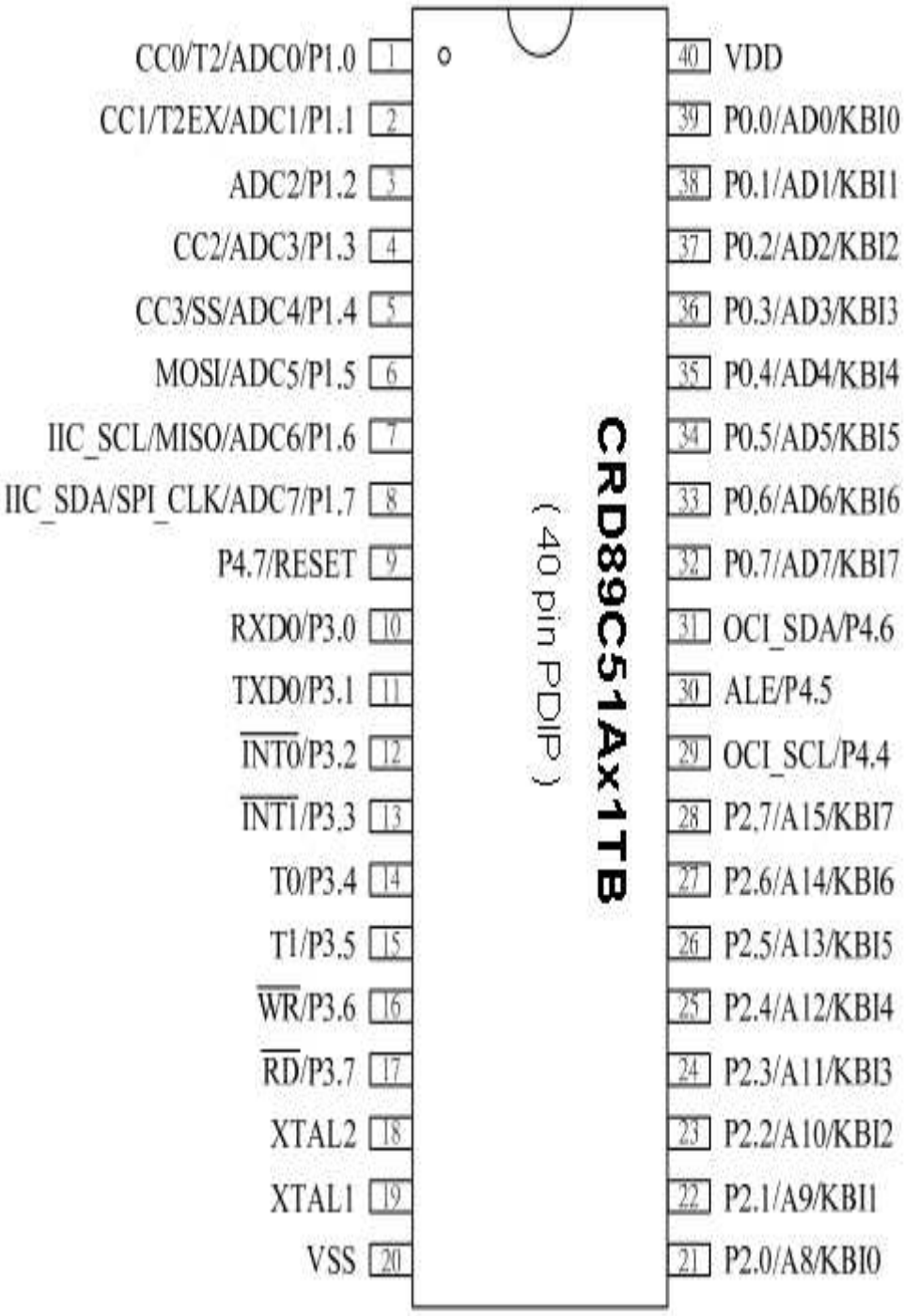
Pin Assignment



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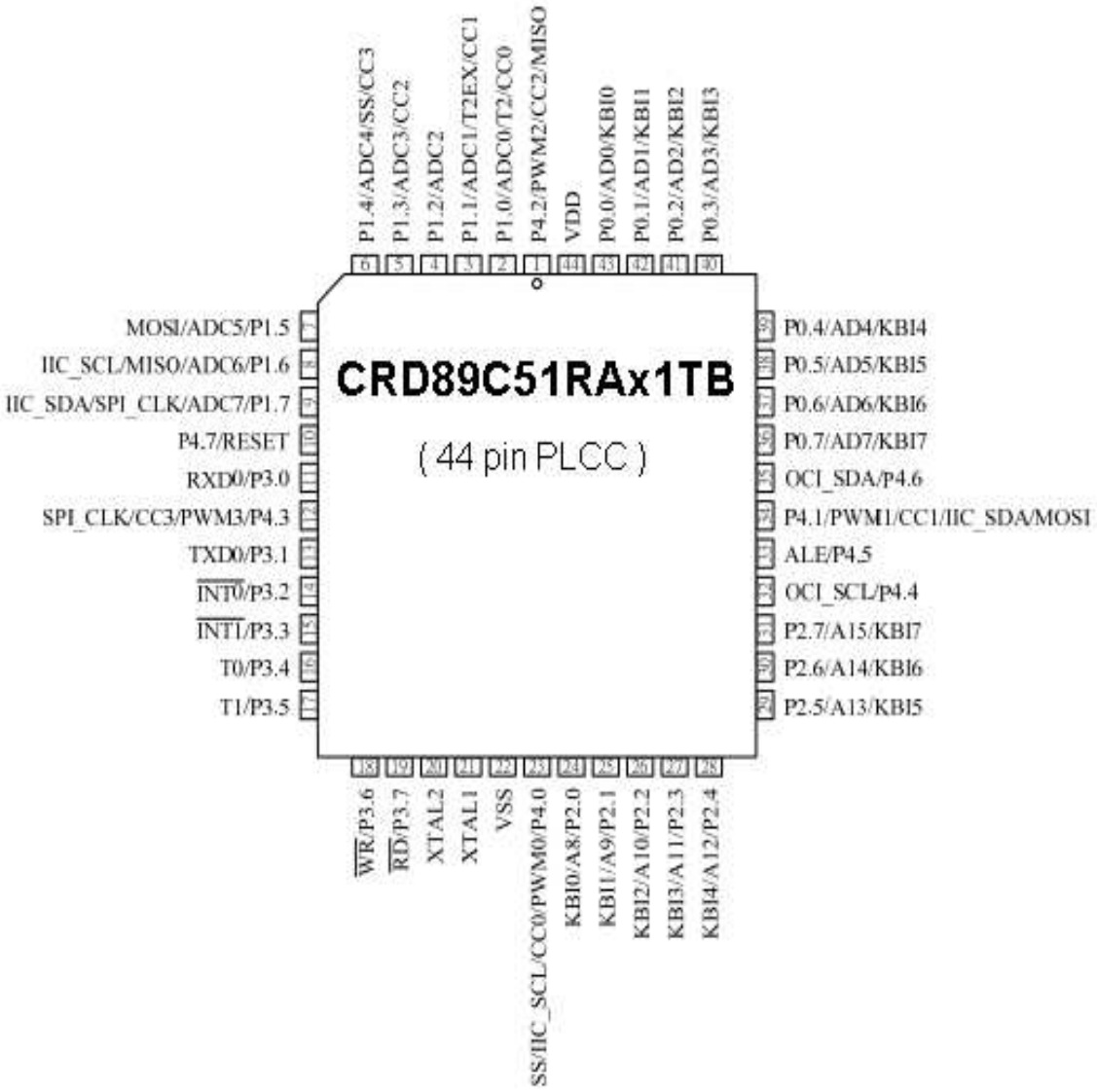
Pin Assignment



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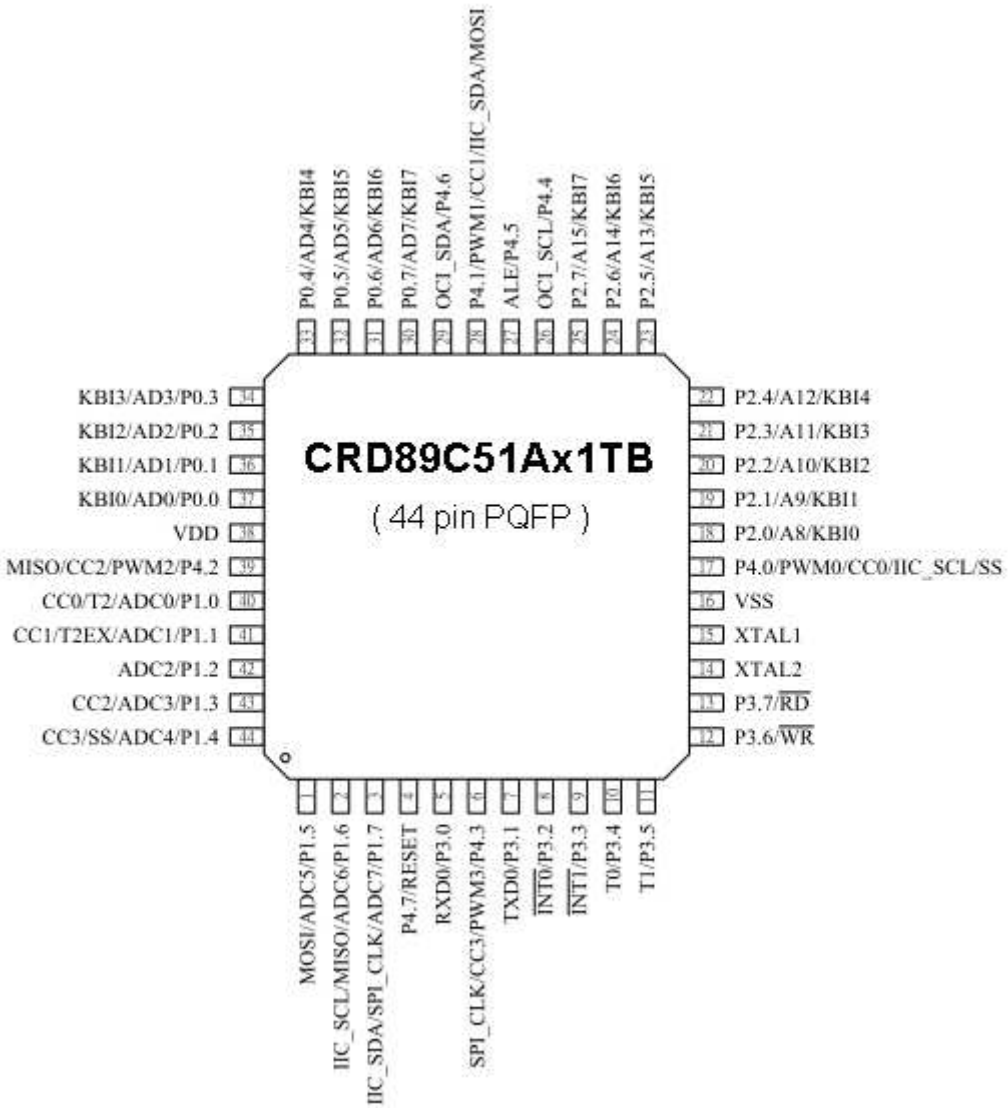

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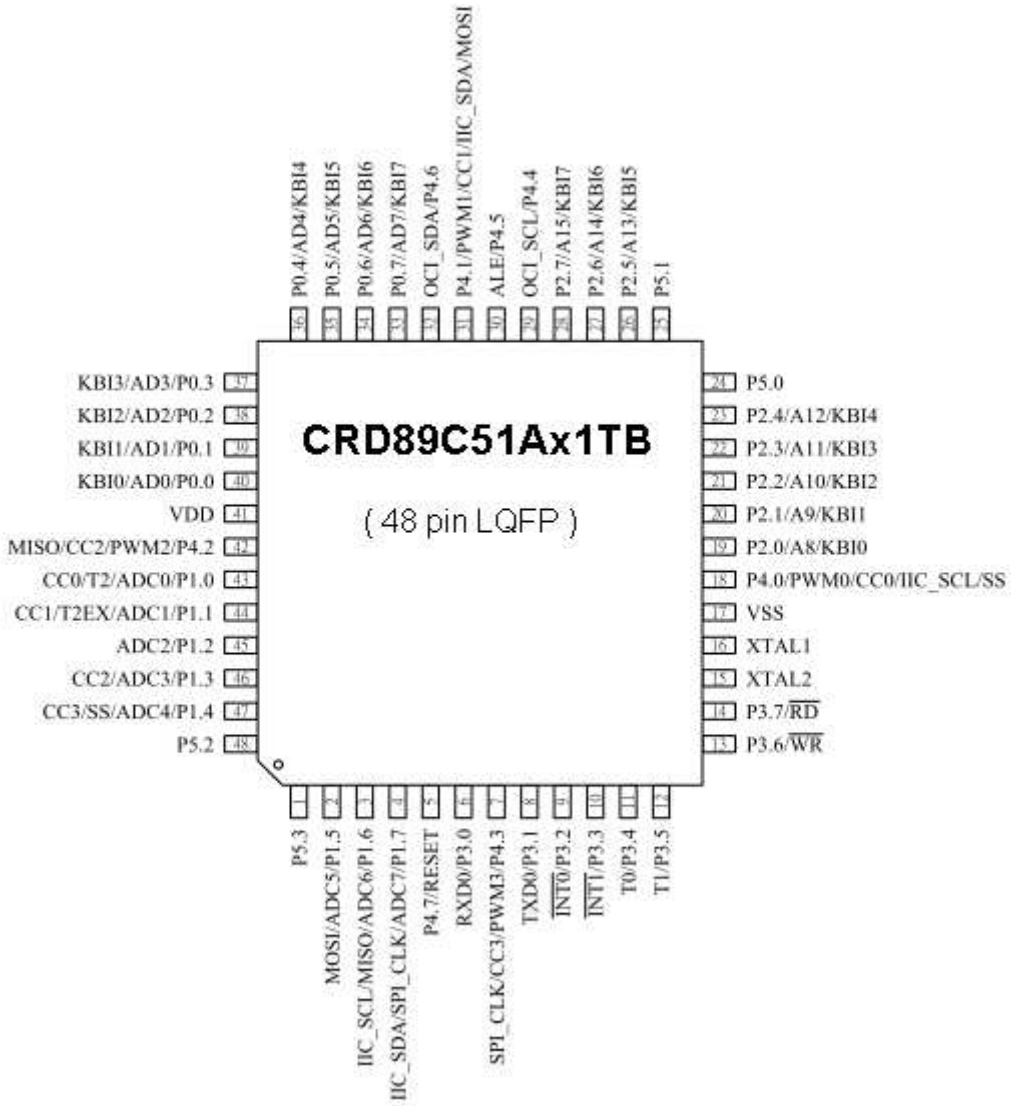
Pin Assignment



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Block Diagram

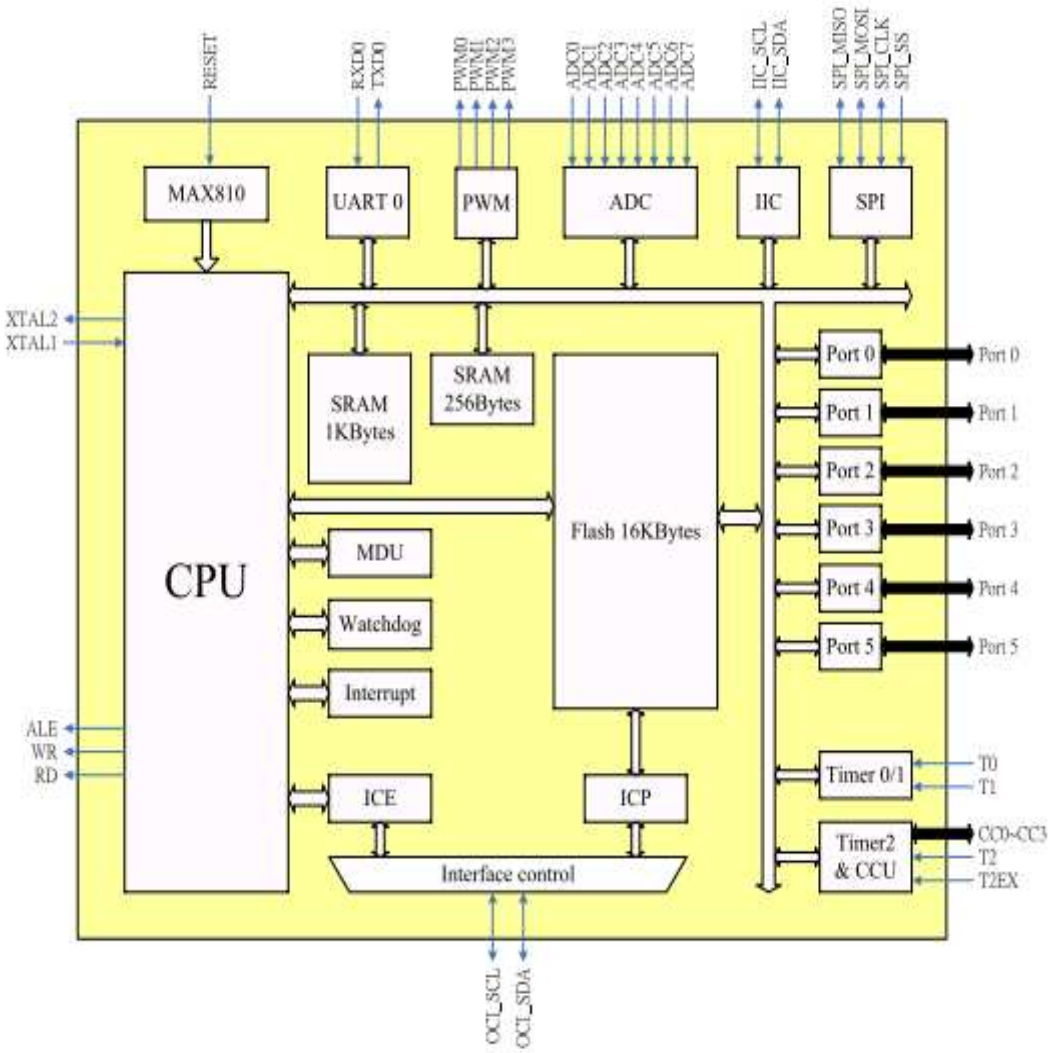

Fig. 1-1. Device Block Diagram

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40L PDIP	44L PLCC	44L PQFP	48L LQFP	Symbol	I/O	Description
	1	39	42	P4.2/PWM2/CC 2/MISO	I/O	Bit 2 of port 4 & PWM Channel 2 & Timer 2 compare/capture Channel 2 & SPIinterface Serial Data Master Input or Slave Output pin
1	2	40	43	P1.0/ADC0/T2/ CC0	I/O	Bit 0 of port 1 & ADC input channel 0 & Timer 2 external input clock & Timer 2 compare/capture Channel 0
2	3	41	44	P1.1/ADC1/ T2EX/CC1	I/O	Bit 1 of port 1 & ADC input channel 1 & Timer 2 capture trigger & Timer 2 compare/capture Channel 1
3	4	42	45	P1.2/ADC2	I/O	Bit 2 of port 1 & ADC input channel 2
4	5	43	46	P1.3/ADC3/CC2	I/O	Bit 3 of port 1 & ADC input channel 3 & Timer 2 compare/capture Channel 2
5	6	44	47	P1.4/ADC4/SS/ CC3	I/O	Bit 4 of port 1 & ADC input channel 4 & SPI interface Slave Select pin & Timer 2 compare/capture Channel 3
			48	P5.2	I/O	Bit 2 of port 5
			1	P5.3	I/O	Bit 3 of port 5
6	7	1	2	P1.5/ADC5/ MOSI	I/O	Bit 5 of port 1 & ADC input channel 5 & SPI interface SerialData Master Output or Slave Input pin
7	8	2	3	P1.6/ADC6/ MISO/ IIC_SCL	I/O	Bit 6 of port 1 & ADC input channel 6 & SPI interface SerialData Master Input or Slave Output pin & IIC SCL pin
8	9	3	4	P1.7/ADC7/ SPI_CLK/ IIC_SDA	I/O	Bit 7 of port 1 & ADC input channel 7 & SPI interface Clockpin & IIC SDA pin
9	10	4	5	RESET/ P4.7	I/O	Reset pin & Bit 7 of port 4
10	11	5	6	P3.0/RXD0	I/O	Bit 0 of port 3 & Serial interface channel 0 Rx data
	12	6	7	P4.3/PWM3/ CC3/TXD1/ SPI_CLK	I/O	Bit 3 of port 4 & PWM Channel 3 & Timer 2 compare/capture Channel 3 & Serial interface channel 1 Tx data or Rx clock in mode 0 & SPI interface Clock pin

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40L PDIP	44L PLCC	44L PQFP	48L LQFP	Symbol	I/O	Description
11	13	7	8	P3.1/TXD0	I/O	Bit 1 of port 3 & Serial interface channel 0 Tx data or Rx clock in mode 0
12	14	8	9	P3.2/#INT0	I/O	Bit 2 of port 3 & External interrupt 0
13	15	9	10	P3.3/#INT1	I/O	Bit 3 of port 3 & External interrupt 1
14	16	10	11	P3.4/T0	I/O	Bit 4 of port 3 & Timer 0 external input
15	17	11	12	P3.5/T1	I/O	Bit 5 of port 3 & Timer 1 external input
16	18	12	13	P3.6/#WR	I/O	Bit 6 of port 3 & external memory write signal
17	19	13	14	P3.7/#RD	I/O	Bit 7 of port 3 & external memory read signal
18	20	14	15	XTAL2	O	Crystal output
19	21	15	16	XTAL1	I	Crystal input
20	22	16	17	VSS	I	Power supply
	23	17	18	P4.0/PWM0/ CC0/IIC_SCL/ SS	I/O	Bit 0 of port 4 & PWM Channel 0 & Timer 2 compare/capture Channel 0 & IIC SCL pin & SPI interface Slave Select pin
21	24	18	19	P2.0/A8/ KBI0	I/O	Bit 0 of port 2 & Bit 8 of external memory address & KBI interrupt 0
22	25	19	20	P2.1/A9/ KBI1	I/O	Bit 1 of port 2 & Bit 9 of external memory address & KBI interrupt 1
23	26	20	21	P2.2/A10/KBI2	I/O	Bit 2 of port 2 & Bit 10 of external memory address & KBI interrupt 2
24	27	21	22	P2.3/A11/KBI3	I/O	Bit 3 of port 2 & Bit 11 of external memory address & KBI interrupt 3
25	28	22	23	P2.4/A12/KBI4	I/O	Bit 4 of port 2 & Bit 12 of external memory address & KBIinterrupt 4
			24	P5.0	I/O	Bit 0 of port 5
			25	P5.1	I/O	Bit 1 of port 5

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40L PDIP	44L PLCC	44L PQFP	48L LQFP	Symbol	I/O	Description
26	29	23	26	P2.5/A13/KBI5	I/O	Bit 5 of port 2 & Bit 13 of external memory address & KBIinterrupt 5
27	30	24	27	P2.6/A14/KBI6	I/O	Bit 6 of port 2 & Bit 14 of external memory address & KBI interrupt 6
28	31	25	28	P2.7/A15/KBI7	I/O	Bit 7 of port 2 & Bit 15 of external memory address & KBIinterrupt 7
29	32	26	29	OCI_SCL/P4.4	I/O	Clock I/O pin of ICE and ICP& Bit 4 of port 4
30	33	27	30	ALE/P4.5	I/O	Address latch enable & Bit 5 of port 4
	34	28	31	P4.1/PWM1/ CC1/IIC_SDA/ MOSI	I/O	Bit 1 of port 4 & PWM Channel 1 & Timer 2 compare/capture Channel 1 & IIC SDA pin & SPI Data Master Output/Slave Input pin
31	35	29	32	OCI_SDA/P4.6	I/O	Data I/O pin of ICE and ICP & Bit 6 of port 4
32	36	30	33	P0.7/AD7/KBI7	I/O	Bit 7 of port 0 & Bit 7 of external memory address/ data & KBI interrupt 7
33	37	31	34	P0.6/AD6/KBI6	I/O	Bit 6 of port 0 & Bit 6 of external memory address/ data & KBI interrupt 6
34	38	32	35	P0.5/AD5/KBI5	I/O	Bit 5 of port 0 & Bit 5 of external memory address/ data & KBI interrupt 5
35	39	33	36	P0.4/AD4/KBI4	I/O	Bit 4 of port 0 & Bit 4 of external memory address/ data & KBI interrupt 4
36	40	34	37	P0.3/AD3/KBI3	I/O	Bit 3 of port 0 & Bit 3 of external memory address/ data & KBI interrupt 3
37	41	35	38	P0.2/AD2/KBI2	I/O	Bit 2 of port 0 & Bit 2 of external memory address/ data & KBI interrupt 2
38	42	36	39	P0.1/AD1/KBI1	I/O	Bit 1 of port 0 & Bit 1 of external memory address/ data & KBI interrupt 1
39	43	37	40	P0.0/AD0/KBI0	I/O	Bit 0 of port 0 & Bit 0 of external memory address/ data & KBI interrupt 0
40	44	38	41	VDD	I	Power supply

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Special Function Registers (SFRs)

Table 1.1: CRD89C51AB1TB SFR location

Hex\Bin	X000	X001	X010	X011	X100	X101	X110	X111	Bin/Hex
F8	IICS	IICCTL	IICA1	IICA2	IICRWD	IICS2			**FF**
F0	B	SPIC1	SPIC2	SPITXD	SPIRXD	SPIS		TAKEY	**F7**
E8	P4	MD0	MD1	MD2	MD3	MD4	MD5	ARCON	**EF**
E0	ACC	ISPFAH	ISPFAL	ISPFD	ISPFC		LVC	SWRES	**E7**
D8	P5		P3M0	P3M1	P4M0	P4M1	P5M0	P5M1	**DF**
D0	PSW		P0M0	P0M1	P1M0	P1M1	P2M0	P2M1	**D7**
C8	T2CON	CCCON	CRCL	CRCH	TL2	TH2	PWM MDH	PWM MDL	**CF**
C0	IRCON	CCEN	CCL1	CCH1	CCL2	CCH2	CCL3	CCH3	**C7**
B8	IEN1	IP1	S0RELH		PWMD 0H	PWMD 0L	PWMD 1H	PWMD 1L	**BF**
B0	P3	PWMD 2H	PWMD 2L	PWMD 3H	PWMD 3L	PWMC	WDTC	WDTK	**B7**
A8	IEN0	IP0	S0RELL	ADCC1	ADCC2	ADCDH	ADCDL	ADCCS	**AF**
A0	P2								**A7**
98	S0CON	S0BUF							**9F**
90	P1	AUX		KBLS	KBE	KBF	KBD		**97**
88	TCON	TMOD	TL0	TL1	TH0	TH1		IFCON	**8F**
80	P0	SP	DPL	DPH	DPL1	DPH1	RCON	PCON	**87**
Hex\Bin	**X000**	**X001**	**X010**	**X011**	**X100**	**X101**	**X110**	**X111**	**Bin/Hex**

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Table 1.2 SFR description and initial value

Register	Location	Reset value	Description
P0	80h	FFh	Port 0
SP	81h	07h	Stack Pointer
DPL	82h	00h	Data Pointer 0 low byte
DPH	83h	00h	Data Pointer 0 high byte
DPL1	84h	00h	Data Pointer 1 low byte
DPH1	85h	00h	Data Pointer 1 high byte
RCON	86h	00h	Internal RAM control register
PCON	87h	40h	Power Control
TCON	88h	00h	Timer/Counter Control
TMOD	89h	00h	Timer Mode Control
TL0	8Ah	00h	Timer 0, low byte
TL1	8Bh	00h	Timer 1, low byte
TH0	8Ch	00h	Timer 0, high byte
TH1	8Dh	00h	Timer 1, high byte
IFCON	8Fh	00h	Interface control register
P1	90h	FFh	Port 1
AUX	91h	00h	AUX
KBLS	93h	00h	Keyboard level selector Register
KBE	94h	00h	Keyboard input enable Register
KBF	95h	00h	Keyboard interrupt flag Register
KBD	96h	00h	Keyboard interface De-bounce control register
S0CON	98h	00h	Serial Port 0, Control Register
S0BUF	99h	00h	Serial Port 0, Data Buffer
P2	A0h	FFh	Port 2
IEN0	A8h	00h	Interrupt Enable Register 0
IP0	A9h	00h	Interrupt Priority Register 0
S0RELL	AAh	00h	Serial Port 0, Reload Register, low byte
ADCC1	ABh	00h	ADC Control 1 Register
ADCC2	ACh	00h	ADC Control 2 Register
ADCDH	ADh	00h	ADC data high byte
ADCDL	AEh	00h	ADC data low byte
ADCCS	AFh	00h	ADC clock select
P3	B0h	FFh	Port 3

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Register	Location	Reset value	Description
PWMD2H	B1h	00h	PWM channel 2 data high byte
PWMD2L	B2h	00h	PWM channel 2 data low byte
PWMD3H	B3h	00h	PWM channel 3 data high byte
PWMD3L	B4h	00h	PWM channel 3 data low byte
PWMC	B5h	00h	PWM control register
WDTC	B6h	04h	Watchdog timer control register
WDTK	B7h	00h	Watchdog timer refresh key.
IEN1	B8h	00h	Interrupt Enable Register 1
IP1	B9h	00h	Interrupt Priority Register 1
S0RELH	BAh	00h	Serial Port 0, Reload Register, high byte
S1RELH	BBh	00h	Serial Port 1, Reload Register, high byte
PWMD0H	BCh	00h	PWM channel 0 data high byte
PWMD0L	BDh	00h	PWM channel 0 data low byte
PWMD1H	BEh	00h	PWM channel 1 data high byte
PWMD1L	BFh	00h	PWM channel 1 data low byte
IRCON	C0h	00h	Interrupt Request Control Register
CCEN	C1h	00h	Compare/Capture Enable Register
CCL1	C2h	00h	Compare/Capture Register 1, low byte
CCH1	C3h	00h	Compare/Capture Register 1, high byte
CCL2	C4h	00h	Compare/Capture Register 2, low byte
CCH2	C5h	00h	Compare/Capture Register 2, high byte
CCL3	C6h	00h	Compare/Capture Register 3, low byte
CCH3	C7h	00h	Compare/Capture Register 3, high byte
T2CON	C8h	00h	Timer 2 Control
CCCON	C9h	00h	Compare/Capture Control
CRCL	CAh	00h	Compare/Reload/Capture Register, low byte
CRCH	CBh	00h	Compare/Reload/Capture Register, high byte
TL2	CCh	00h	Timer 2, low byte
TH2	CDh	00h	Timer 2, high byte
PWMMDH	CEh	00h	PWM Max Data Register, high byte.
PWMMDL	CFh	FFh	PWM Max Data Register, low byte.
PSW	D0h	00h	Program Status Word
P0M0	D2h	00h	Port 0 output mode 0
P0M1	D3h	00h	Port 0 output mode 1
P1M0	D4h	00h	Port 1 output mode 0
P1M1	D5h	00h	Port 1 output mode 1
P2M0	D6h	00h	Port 2 output mode 0

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Register	Location	Reset value	Description
P2M1	D7h	00h	Port 2 output mode 1
P5	D8h	3Fh	Port 5
P3M0	DAh	00h	Port 3 output mode 0
P3M1	DBh	00h	Port 3 output mode 1
P4M0	DCh	00h	Port 4 output mode 0
P4M1	DDh	00h	Port 4 output mode 1
P5M0	DEh	00h	Port 5 output mode 0
P5M1	DFh	00h	Port 5 output mode 1
ACC	E0h	00h	Accumulator
ISPFAH	E1h	FFh	ISP Flash Address-High register
ISPFAL	E2h	FFh	ISP Flash Address-Low register
ISPFD	E3h	FFh	ISP Flash Data register
ISPFC	E4h	00h	ISP Flash control register
LVC	E6h	00h	Low voltage control register
SWRES	E7h	00h	Software Reset register
P4	E8h	FFh	Port 4
MD0	E9h	00h	Multiplication/Division Register 0
MD1	EAh	00h	Multiplication/Division Register 1
MD2	EBh	00h	Multiplication/Division Register 2
MD3	ECh	00h	Multiplication/Division Register 3
MD4	EDh	00h	Multiplication/Division Register 4
MD5	EEh	00h	Multiplication/Division Register 5
ARCON	EFh	00h	Arithmetic Control Register
B	F0h	00h	B Register
SPIC1	F1h	08h	SPI control register 1
SPIC2	F2h	00h	SPI control register 2
SPITXD	F3h	00h	SPI transmit data buffer
SPIRXD	F4h	00h	SPI receive data buffer
SPIS	F5h	40h	SPI status register
TAKEY	F7h	00h	Time Access Key register
IICS	F8h	00h	IIC status register
IICCTL	F9h	04h	IIC control register
IICA1	FAh	A0h	IIC channel 1 Address 1 register
IICA2	FBh	60h	IIC channel 1 Address 2 register
IICRWD	FCh	00h	IIC channel 1 Read / Write Data buffer
IICS2	FDh	00h	IIC status2 register

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Functional Description

1. General Features

CRD89C51AB1TB is an 8-bit micro-controller. All of its functions and the detailed meanings of the SFRs will be given in the following sections.

1.1. Embedded Flash

The program can be loaded into the embedded flash memory via an external writer, an ICP (In-Circuit Programming) device, or the ISP (In-System Programming) software. The high-quality Flash has a 100K-write cycle life and is suitable for program reloading, data recording, or EEPROM functionallity.

1.2. IO Pads

Six I/O ports are provided: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 3, 4 are 8-bit ports and Port 5 is a 4-bit port. They can operate in the following modes: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. These modes are further discussed in section 5.
Pins OCI_SCL,ALE,OCI_SDA and RESET can be redefined as P4.4,P4.5,P4.6 and P4.7 during reprogramming.
All the pads for P0 ~ P5 are slew rate controlled to reduce EMI. Another way to reduce EMI is to disable the ALE output if unused. This is selected by its SFR. The IO pads can withstand 4KV ESD (human body model) guaranteeing the mcu's performance in high ESD environments.

1.3. 2T/1T Selection

The conventional 8052 series MCUs are 12T, i.e., 12 oscillator clocks are needed for each machine cycle. CRD89C51AB1TB is a 2T or 1T MCU, it can execute one instruction within two clocks, or only one clock. The difference between 2T mode and 1T mode is illustrated in Fig. 1-2.

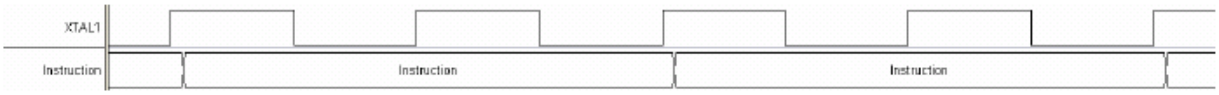

Fig. 1-2(a): The waveform of internal instruction signal in 2T mode

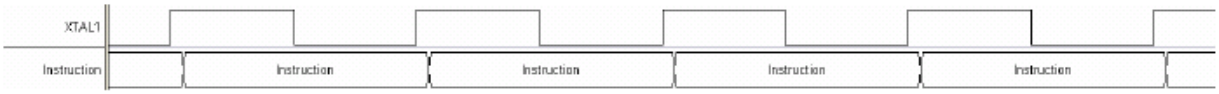

Fig. 1-2(b): The waveform of internal instruction signal in 1T mode

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The device defaults to 2T mode, and it can be changed to 1T mode if IFCON [7] (at address 8Fh) is set high. Not every instruction can be executed within one machine cycle. The exact number of machine cycles required for each instruction is given in the next section.

1.4. Reset

1.4.1 Hardware RESET function

The mcu provides an Internal reset circuit. The internal reset time is set during reprogramming. The following options are available:

Internal Reset time
25ms (default)
200ms
100ms
50ms
16ms
8ms
4ms

1.4.2 Software RESET function

A Software reset mechanism is provided, that resets the whole device. To perform a software reset, the firmware must write FFh to the SWRES register. This is possible only after the TAKEY register is written to by the values 55h, AAh and 5Ah in that order. The resulting software reset signal is ORed with the hardware reset signal. The SWRES register is self-reset at the end of the software reset procedure.

Mnemonic	Description	Address	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Reset
Software Reset Function											
TAKEY	Time Access Key reg.	F7h	TAKEY[7:0]								OOH
SWRES	Software Reset register	E7h	SWRES[7:0]								00H

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1.4.3 Time Access Key register

Mnemonic: TAKEY				Address: F7h				
7	6	5	4	3	2	1	0	Reset
TAKEY[7:0]								00h

The software reset register (SWRES) is read-only by default. To enable the SWRES register write attribute, the firmware must write to the TAKEY register three specific values 55h, AAh and 5Ah in this order.

1.4.4 Software Reset register (SWRES)

Mnemonic: SWRES					Address: E7h			
7	6	5	4	3	2	1	0	Reset
SWRES[7:0]								00h

SWRES [7:0]: Software reset register. These 8-bit is self-reset at the end of the software reset procedure.
SWRES [7:0] = FFh, software reset.
SWRES [7:0] = 00h ~ FEh, MCU no action.

1.4.5 Example of software reset

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah ; enable SWRES write attribute
MOV SWRES, #FFh ; software reset MCU
```

1.5. Clock sources

The clock source of the device may be either external, or internal. The external clock source may be either a crystal connected to pins XTAL1 and XTAL2, or an external oscillator connected to pin XTAL1 only. The internal clock source is the internal oscillator that may be set to run at frequencies ranging from 1MHz to 24MHz. This frequency can be set when programming the device from an external writer. The choice of internal, or external, clock source is also made during this programming phase. The settings are stored within the device in a dedicated area of the flash memory, the information block. This is a 128 byte flash memory, separate from the program memory and accessible only by the device core and only to retrieve its settings.

After a reset, the mcu defaults to the use of the external oscillator. It then reads the settings stored at the information block and selects the clock source required by the user.

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The possible clock source selections are provided in table 1-1:

Clock source
external crystal or OSC
24MHz from the internal OSC
20MHz from the internal OSC
16MHz from the internal OSC
12MHz from the internal OSC
8MHz from the internal OSC
4MHz from the internal OSC
2MHz from the internal OSC
1MHz from the internal OSC (default selection during the device initialization process)

Table 1.3 : Selection of clock source

Please, note that there may be a 20% variance in the frequency of the internal oscillator. Its use is not recommended in applications requiring an accurate clock source.

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2. Instruction Set

All CRD89C51AB1TB instructions are binary code compatible and perform the same functions as they do with the industry standard 8051. The following tables provide a summary of this instruction set. The corresponding mnemonics, descriptions, op codes, program memory bytes and required machine cycles are provided. Each machine cycle, might need one, or two, oscillator clocks, depending on the setting of bit IFCON[7].

Table 2-1 : Arithmetic operations

Mnemonic	Description	Code	Bytes	Cycles
ADD A,Rn	Add register to accumulator	28-2F	1	1
ADD A,direct	Add direct byte to accumulator	25	2	2
ADD A,@Ri	Add indirect RAM to accumulator	26-27	1	2
ADD A,#data	Add immediate data to accumulator	24	2	2
ADDC A,Rn	Add register to accumulator with carry flag	38-3F	1	1
ADDC A,direct	Add direct byte to A with carry flag	35	2	2
ADDC A,@Ri	Add indirect RAM to A with carry flag	36-37	1	2
ADDC A,#data	Add immediate data to A with carry flag	34	2	2
SUBB A,Rn	Subtract register from A with borrow	98-9F	1	1
SUBB A,direct	Subtract direct byte from A with borrow	95	2	2
SUBB A,@Ri	Subtract indirect RAM from A with borrow	96-97	1	2
SUBB A,#data	Subtract immediate data from A with borrow	94	2	2
INC A	Increment accumulator	04	1	1
INC Rn	Increment register	08-0F	1	2
INC direct	Increment direct byte	05	2	3
INC @Ri	Increment indirect RAM	06-07	1	3
INC DPTR	Increment data pointer	A3	1	1
DEC A	Decrement accumulator	14	1	1
DEC Rn	Decrement register	18-1F	1	2
DEC direct	Decrement direct byte	15	2	3
DEC @Ri	Decrement indirect RAM	16-17	1	3
MUL AB	Multiply A and B	A4	1	5
DIV	Divide A by B	84	1	5
DA A	Decimal adjust accumulator	D4	1	1

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Table 2-2 : Logic operations

Mnemonic	Description	Code	Bytes	Cycles
ANL A,Rn	AND register to accumulator	58-5F	1	1
ANL A,direct	AND direct byte to accumulator	55	2	2
ANL A,@Ri	AND indirect RAM to accumulator	56-57	1	2
ANL A,#data	AND immediate data to accumulator	54	2	2
ANL direct,A	AND accumulator to direct byte	52	2	3
ANL direct,#data	AND immediate data to direct byte	53	3	4
ORL A,Rn	OR register to accumulator	48-4F	1	1
ORL A,direct	OR direct byte to accumulator	45	2	2
ORL A,@Ri	OR indirect RAM to accumulator	46-47	1	2
ORL A,#data	OR immediate data to accumulator	44	2	2
ORL direct,A	OR accumulator to direct byte	42	2	3
ORL direct,#data	OR immediate data to direct byte	43	3	4
XRL A,Rn	Exclusive OR register to accumulator	68-6F	1	1
XRL A,direct	Exclusive OR direct byte to accumulator	65	2	2
XRL A,@Ri	Exclusive OR indirect RAM to accumulator	66-67	1	2
XRL A,#data	Exclusive OR immediate data to accumulator	64	2	2
XRL direct,A	Exclusive OR accumulator to direct byte	62	2	3
XRL direct,#data	Exclusive OR immediate data to direct byte	63	3	4
CLR A	Clear accumulator	E4	1	1
CPL A	Complement accumulator	F4	1	1
RL A	Rotate accumulator left	23	1	1
RLC A	Rotate accumulator left through carry	33	1	1
RR A	Rotate accumulator right	03	1	1
RRC A	Rotate accumulator right through carry	13	1	1
SWAP A	Swap nibbles within the accumulator	C4	1	1

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Table 2-3 : Data transfer

Mnemonic	Description	Code	Bytes	Cycles
MOV A,Rn	Move register to accumulator	E8-EF	1	1
MOV A,direct	Move direct byte to accumulator	E5	2	2
MOV A,@Ri	Move indirect RAM to accumulator	E6-E7	1	2
MOV A,#data	Move immediate data to accumulator	74	2	2
MOV Rn,A	Move accumulator to register	F8-FF	1	2
MOV Rn,direct	Move direct byte to register	A8-AF	2	4
MOV Rn,#data	Move immediate data to register	78-7F	2	2
MOV direct,A	Move accumulator to direct byte	F5	2	3
MOV direct,Rn	Move register to direct byte	88-8F	2	3
MOV direct1,direct2	Move direct byte to direct byte	85	3	4
MOV direct,@Ri	Move indirect RAM to direct byte	86-87	2	4
MOV direct,#data	Move immediate data to direct byte	75	3	3
MOV @Ri,A	Move accumulator to indirect RAM	F6-F7	1	3
MOV @Ri,direct	Move direct byte to indirect RAM	A6-A7	2	5
MOV @Ri,#data	Move immediate data to indirect RAM	76-77	2	3
MOV DPTR,#data16	Load data pointer with a 16-bit constant	90	3	3
MOVC A,@A+DPTR	Move code byte relative to DPTR to accumulator	93	1	3
MOVC A,@A+PC	Move code byte relative to PC to accumulator	83	1	3
MOVX A,@Ri	Move external RAM (8-bit addr.) to A	E2-E3	1	3
MOVX A,@DPTR	Move external RAM (16-bit addr.) to A	E0	1	3
MOVX @Ri,A	Move A to external RAM (8-bit addr.)	F2-F3	1	4
MOVX @DPTR,A	Move A to external RAM (16-bit addr.)	F0	1	4
PUSH direct	Push direct byte onto stack	C0	2	4
POP direct	Pop direct byte from stack	D0	2	3
XCH A,Rn	Exchange register with accumulator	C8-CF	1	2
XCH A,direct	Exchange direct byte with accumulator	C5	2	3
XCH A,@Ri	Exchange indirect RAM with accumulator	C6-C7	1	3
XCHD A,@Ri	Exchange low-order nibble indir. RAM with A	D6-D7	1	3

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Table 2-4 : Program branches

Mnemonic	Description	Code	Bytes	Cycles
ACALL addr11	Absolute subroutine call	xxx11	2	6
LCALL addr16	Long subroutine call	12	3	6
RET	from subroutine	22	1	4
RETI	from interrupt	32	1	4
AJMP addr11	Absolute jump	xxx01	2	3
LJMP addr16	Long jump	02	3	4
SJMP rel	Short jump (relative addr.)	80	2	3
JMP @A+DPTR	Jump indirect relative to the DPTR	73	1	2
JZ rel	Jump if accumulator is zero	60	2	3
JNZ rel	Jump if accumulator is not zero	70	2	3
JC rel	Jump if carry flag is set	40	2	3
JNC	Jump if carry flag is not set	50	2	3
JB bit,rel	Jump if direct bit is set	20	3	4
JNB bit,rel	Jump if direct bit is not set	30	3	4
JBC bit,direct rel	Jump if direct bit is set and clear bit	10	3	4
CJNE A,direct rel	Compare direct byte to A and jump if not equal	B5	3	4
CJNE A,#data rel	Compare immediate to A and jump if not equal	B4	3	4
CJNE Rn,#data rel	Compare immed. to reg. and jump if not equal	B8-BF	3	4
CJNE @Ri,#data rel	Compare immediate to indirect and jump if not equal	B6-B7	3	4
DJNZ Rn,rel	Decrement register and jump if not zero	D8-DF	2	3
DJNZ direct,rel	Decrement direct byte and jump if not zero	D5	3	4
NOP	No operation	00	1	1

Table 2-5 : Boolean manipulation

Mnemonic	Description	Code	Bytes	Cycles
CLR C	Clear carry flag	C3	1	1
CLR bit	Clear direct bit	C2	2	3
SETB C	Set carry flag	D3	1	1
SETB bit	Set direct bit	D2	2	3
CPL C	Complement carry flag	B3	1	1
CPL bit	Complement direct bit	B2	2	3
ANL C,bit	AND direct bit to carry flag	82	2	2
ANL C,/bit	AND complement of direct bit to carry	B0	2	2
ORL C,bit	OR direct bit to carry flag	72	2	2
ORL C,/bit	OR complement of direct bit to carry	A0	2	2
MOV C,bit	Move direct bit to carry flag	A2	2	2
MOV bit,C	Move carry flag to direct bit	92	2	3

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3. Memory Structure

The CRD89C51AB1TB memory structure follows the general 8052 structure. It manipulates operands in three memory spaces. They are (1) 256 bytes standard RAM, (2) 1K bytes auxiliary RAM, and (3) 16K bytes embedded flash as program memory.

3.1. Program Memory

The CRD89C51AB1TB has 16KB on-chip flash memory which can be used as general program memory. It is located in addresses $0000 to $3FFF. If there is any byte not used as program memory, it can be used to record data as EEPROM. Guidance on how to do this is provided in section 19. At the top of this address range, up to 4k bytes may be used to host an ISP service program. The ISP service program size can be set in N multiples of 256 byte blocks, where N=0 to 16. When N=0, no memory is allocated to the ISP service program. When N=1 addresses $3F00 to $3FFF are reserved for the ISP service program. When N=2 addresses $3E00 to $3FFF are reserved for the ISP service program…etc. The value of N is set by the external writer, or ICP.

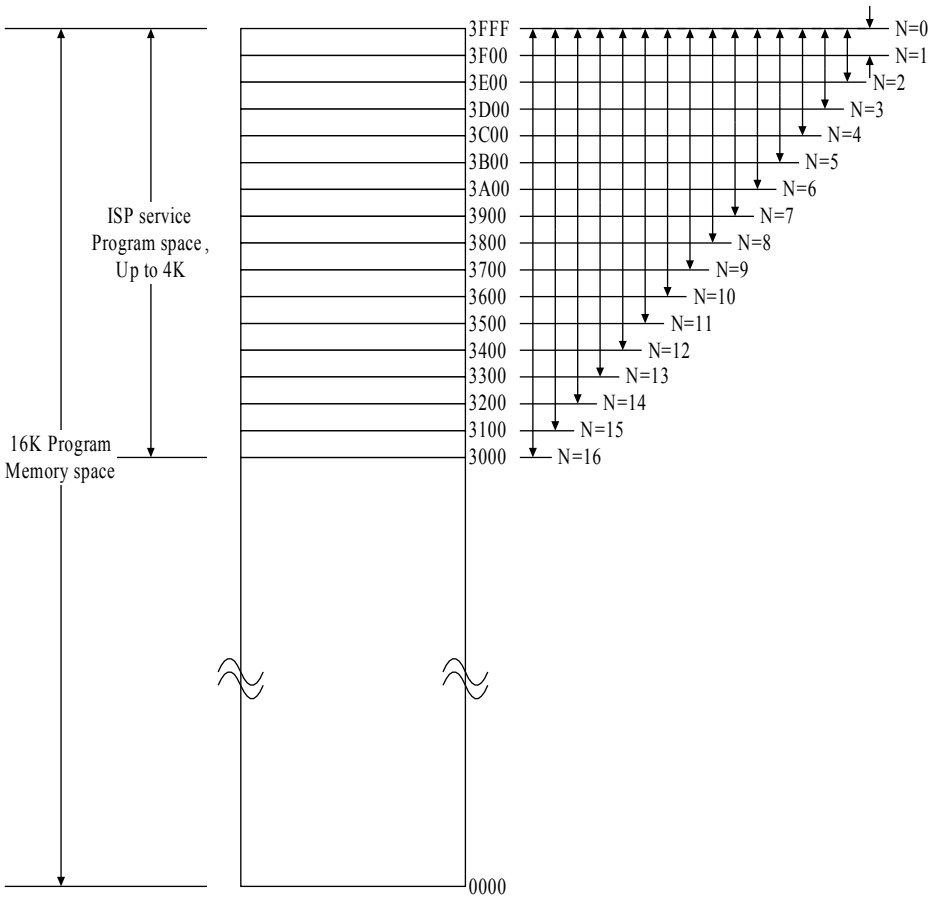

Fig.3.1: Flash Memory Structure

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3.2. Data Memory

The mcu provides 1024 plus 256 Bytes of on-chip SRAM. The 256 bytes are the same as the general 8052 internal memory structure. If bit IFCON[1] = 0, the 1KB on-chip SRAM is enabled and accessed through MOVX instructions. Address range from 0400h to FFFFh is accessed by a standard external memory interface using P2 and P0 for the address/data bus, and P3[7:6] for the read/write signals. If bit IFCON[1] = 1, the internal 1k bytes of RAM are disabled and the whole range of RAM addresses is accessed via the external memory interface.
Please note that the external memory interface complies with the standard 12T timing. Figure 3-2 illustrates its operation:

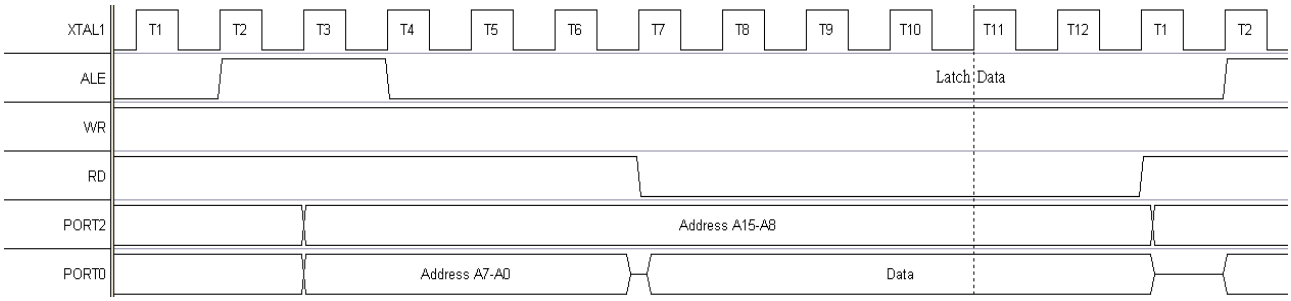

Fig. 3-2(a): External memory access - read

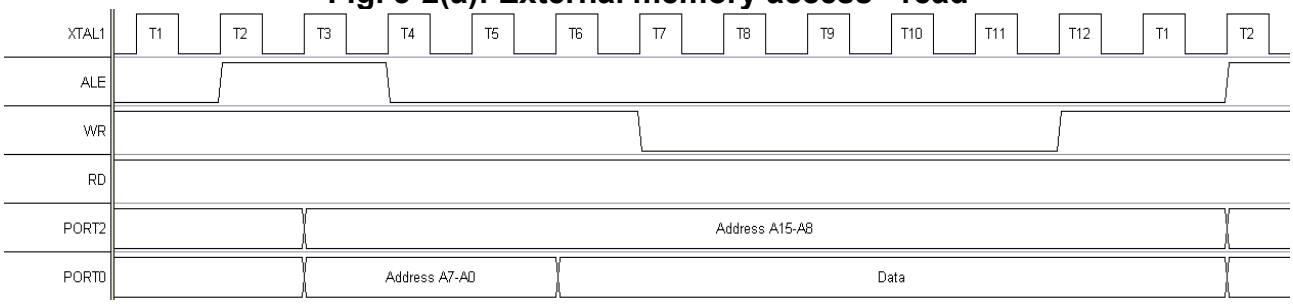

Fig. 3-2(b): External memory access – write

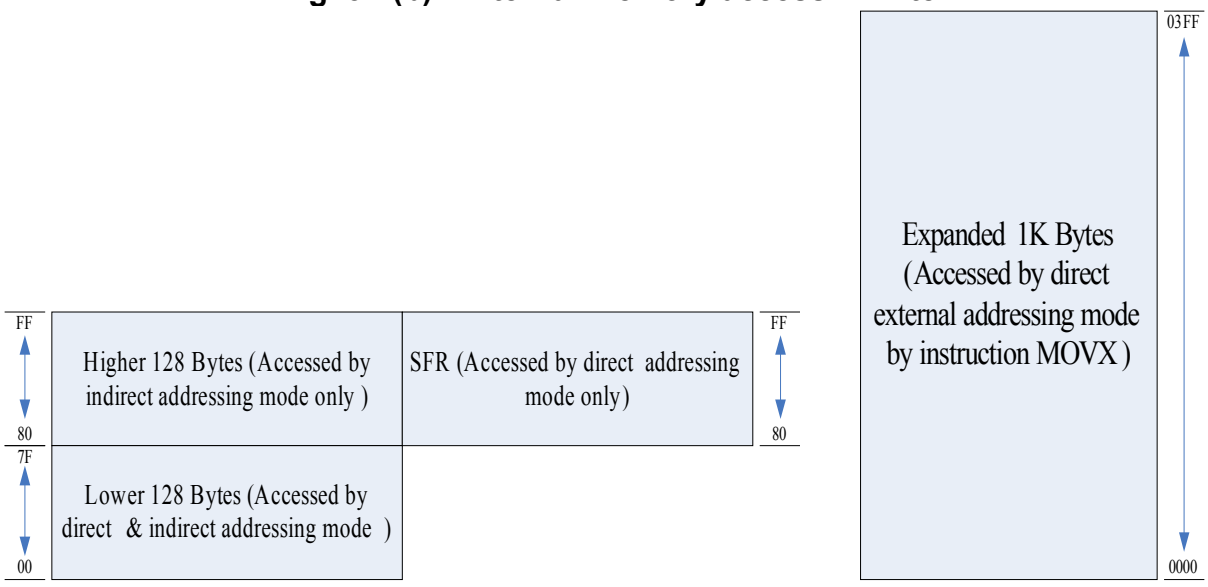

Fig. 3-3: RAM architecture

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3.2.1. Data memory - lower 128 byte (00h to 7Fh)

Data Memory 00h to FFh is the same as defined in 8052. Addresses 00h to 7Fh are accessed by both direct and indirect addressing. Addresses 00h to 1Fh is register area. Addresses 20h to 2Fh is memory bit area, and address 30h to 7Fh is for general memory area.

3.2.2. Data memory - higher 128 byte (80h to FFh)

Addresses 80h to FFh are accessed by indirect addressing. It is data area.

3.2.3. Data memory - Expanded 1024 bytes ($0000 to $03FF)

External addresses 0000h to 03FFh contain the on-chip expanded SRAM, a total of 1024 Bytes. This memory can be accessed via external direct addressing mode (with MOVX instructions). Accessing addresses outside this range will generate the external memory control signal automatically. Bit EMEN in IFCON[1] controls the availability of this memory section. When EMEN = 0, the 1KB on-chip SRAM is enabled. The default value for EMEN is 0.
The address space of instruction MOVX @Ri,A (i=0,1) is determined by RCON [7:0] of SFR $86 RCON (internal RAM control register). The default setting of RCON [7:0] is 00h (page0). One page of data RAM is 256 bytes.

MOVX @Ri, A MOVX A,@Ri	0 <= RCON[7:0] <= 3	4 <= RCON [7:0] <= 255
EMEN = 0	Addr [15:8] <= RCON[7:0]	Port2 [7:0] <= RCON[7:0]
EMEN = 1	Port2 [7:0] <= P2 [7:0]	Port2 [7:0] <= P2 [7:0]

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4. CPU Engine

The mcu engine is composed of four components:

a. Control unit
b. Arithmetic – logic unit
c. Memory control unit
d. RAM and SFR control unit

The mcu engine fetches instructions from program memory and executes them using RAM or SFR. The following paragraphs describe its registers.

Name	Description	Loc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
CPU Core											
ACC	Accumulator	E0h	ACC.7	ACC.6	ACC.5	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H
B	B register	F0h	B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H
PSW	Program status word	D0h	CY	AC	F0	RS[1:0]		OV	F1	P	00H
SP	Stack Pointer	81h	SP[7:0]								07H
DPL	Data pointer 0 low	82h	DPL[7:0]								00H
DPH	Data pointer 0 high	83h	DPH[7:0]								00H
DPL1	Data pointer 1 low	84h	DPL1[7:0]								00H
DPH1	Data pointer 1 high	85h	DPH1[7:0]								00H
AUX	Auxiliary register	91h	BRS	P4 CC	P4 SPI	--	P4 IIC	P0 KBI	--	DPS	00H
RCON	Internal RAM control register	86h	RCON[7:0]								00H
IFCON	Interface control register	8Fh	ITS	CDPR	--	--	ALEC[1:0]		EMEN	ISPE	00H

4.1. Accumulator

The Accumulator register. Most instructions use the Acc to store the operand.

Mnemonic: ACC Address: E0h

7	6	5	4	3	2	1	0	Reset
ACC.7	ACC.6	ACC05	ACC.4	ACC.3	ACC.2	ACC.1	ACC.0	00H

ACC[7:0]: The A (or ACC) register is the standard 8052 accumulator.

4.2. B Register

The B register is used during multiply and divide instructions. It can also be used as a scratch pad register to store temporary data.

Mnemonic: B Address: F0h

7	6	5	4	3	2	1	0	Reset
B.7	B.6	B.5	B.4	B.3	B.2	B.1	B.0	00H

B[7:0]: The B register serves as a second accumulator.

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4.3. Program Status Word

Mnemonic: PSW Address: D0h

7	6	5	4	3	2	1	0	Reset
CY	AC	F0	RS[1:0]		OV	F1	P	00H

CY: Carry flag.
AC: Auxiliary Carry flag for BCD operations.
F0: General purpose Flag 0 available for user.
RS[1:0]: Register bank select, used to select working register bank.

RS[1:0]	Bank Selected	Location
00	Bank 0	00H – 07H
01	Bank 1	08H – 0FH
10	Bank 2	10H – 17H
11	Bank 3	18H – 1FH

OV: Overflow flag.
F1: General purpose Flag 1 available for user.
P: Parity flag, affected by hardware to indicate odd/even number of “one” bits in the Accumulator, i.e. even parity.

4.4. Stack Pointer

The stack pointer is a 1-byte register initialized to 07H after reset. This register is incremented before PUSH and CALL instructions, causing the stack to start from location 08H.

Mnemonic: SP Address: 81h

7	6	5	4	3	2	1	0	Reset
SP[7:0]								07H

SP[7:0]: The Stack Pointer stores the scratchpad RAM address where the stack begins. It points to the top of the stack.

4.5. Data Pointer

The data pointer (DPTR) is 2-bytes wide. The lower part is DPL, and the highest is DPH. It can be loaded as a 2-byte register (e.g. MOV DPTR,#data16) or as two separate registers (e.g. MOV DPL,#data8). It is generally used to access the external code or data space (e.g. MOVC A,@A+DPTR or MOV A, @DPTR respectively).

Mnemonic: DPL Address: 82h

7	6	5	4	3	2	1	0	Reset
DPL[7:0]								00H

DPL[7:0]: Data pointer Low 0

Mnemonic: DPH Address: 83h

7	6	5	4	3	2	1	0	Reset
DPH[7:0]								00H

DPH[7:0]: Data pointer High 0

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4.6. Data Pointer 1

The dual data pointer accelerates the movement of block data. The standard DPTR is a 16-bit register that is used to address external memory, or peripherals. The standard data pointer is called DPTR and the second data pointer is called DPTR1. The data pointer select bit chooses the active pointer. The data pointer select bit (DPS) is located in the LSB of AUX register (AUX.0).

The user switches between DPTR and DPTR1 by toggling the DPS bit. All DPTR-related instructions use the currently selected DPTR for any activity.

Mnemonic: DPL1 Address: 84h

7	6	5	4	3	2	1	0	Reset
DPL1[7:0]								00H

DPL1[7:0]: Data pointer Low 1

Mnemonic: DPH1 Address: 85h

7	6	5	4	3	2	1	0	Reset
DPH1[7:0]								00H

DPH1[7:0]: Data pointer High 1

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

DPS: Data Pointer select bit.
DPS = 1 is selects DPTR1.

4.7. Internal RAM control register

Mnemonic: RCON Address: 86h

7	6	5	4	3	2	1	0	Reset
RCON[7:0]								00H

1K bytes of on-chip expanded RAM are provided and can be accessed by external memory addressing method only (instruction MOVX). The address space of instruction MOVX @Ri,A (i= 0,1) is determined by RCON [7:0] of RCON. The default setting of RCON [7:0] is 00h (page0).

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4.8. Interface control register

Mnemonic: IFCON Address: 8Fh

7	6	5	4	3	2	1	0	Reset
ITS	CDPR	--	--	ALEC[1:0]		EMEN	ISPE	00H

ITS: Instruction timing select.
ITS = 0, 2T instruction mode (default).
ITS = 1, 1T instruction mode.
CDPR: Code protect (read only).

ALEC[1:0]: ALE output control register.

ALEC[1:0]	ALE Output
00	Always output
01	No ALE output
10	Only Read or Write have ALE output
11	reserved

EMEN: Internal 1K SRAM disable.
EMEN = 0, Enable internal 1K RAM (default).
EMEN = 1, Disable internal 1K RAM.

ISPE: ISP function enable bit.
ISPE = 0, Disable ISP function (default).
ISPE = 1, Enable ISP function.

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5. GPIO

Six I/O ports are available: Port 0, Port 1, Port 2, Port 3, Port 4, and Port 5. Ports 0, 1, 2, 3, 4 are 8-bit ports and Port 5 is a 4-bit port. They can operate in four modes: quasi-bidirectional (standard 8051 port outputs), push-pull, open drain, and input-only. Two configuration registers for each port select the output mode for each port pin. All I/O port pins may be configured by software to one of four modes on a pin-by-pin basis, as shown below:

Mnemonic	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
P0M0	Port 0 output mode 0	D2h	P0M0[7:0]								00h
P0M1	Port 0 output mode 1	D3h	P0M1[7:0]								00h
P1M0	Port 1 output mode 0	D4h	P1M0[7:0]								00h
P1M1	Port 1 output mode 1	D5h	P1M1[7:0]								00h
P2M0	Port 2 output mode 0	D6h	P2M0[7:0]								00h
P2M1	Port 2 output mode 1	D7h	P2M1[7:0]								00h
P3M0	Port 3 output mode 0	DAh	P3M0[7:0]								00h
P3M1	Port 3 output mode 1	DBh	P3M1[7:0]								00h
P4M0	Port 4 output mode 0	DCh	P4M0[7:0]								00h
P4M1	Port 4 output mode 1	DDh	P4M1[7:0]								00h
P5M0	Port 5 output mode 0	DEh	--	--	P5M0[3:0]						00h
P5M1	Port 5 output mode 1	DFh	--	--	P5M1[3:0]						00h

PxM1.y	PxM0.y	Port output mode
0	0	Quasi-bidirectional (standard 8051 port outputs) (pull-up)
0	1	Push-pull
1	0	Input only (high-impedance)
1	1	Open drain

Pins OCI_SCL,ALE,OCI_SDA and RESET can be defined as P4.4,P4.5,P4.6 and P4.7 by the external writer, or the ISP, during device reprogramming.

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Every pin can be set either high, or low, independently as described below:

Mnemonic	Description	Address	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	Reset
Ports											
Port 5	Port 5	D8h	--	--	--	--	P5.3	P5.2	P5.1	P5.0	FFh
Port 4	Port 4	E8h	P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh
Port 3	Port 3	B0h	P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh
Port 2	Port 2	A0h	P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh
Port 1	Port 1	90h	P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh
Port 0	Port 0	80h	P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

Mnemonic: P0								Address: 80h
7	6	5	4	3	2	1	0	Reset
P0.7	P0.6	P0.5	P0.4	P0.3	P0.2	P0.1	P0.0	FFh

P0.7~0: Port0 [7] ~ Port0 [0]

Mnemonic: P1								Address: 90h
7	6	5	4	3	2	1	0	Reset
P1.7	P1.6	P1.5	P1.4	P1.3	P1.2	P1.1	P1.0	FFh

P1.7~0: Port1 [7] ~ Port1 [0]

Mnemonic: P2								Address: A0h
7	6	5	4	3	2	1	0	Reset
P2.7	P2.6	P2.5	P2.4	P2.3	P2.2	P2.1	P2.0	FFh

P2.7~0: Port2 [7] ~ Port2 [0]

Mnemonic: P3								Address: B0h
7	6	5	4	3	2	1	0	Reset
P3.7	P3.6	P3.5	P3.4	P3.3	P3.2	P3.1	P3.0	FFh

P3.7~0: Port3 [7] ~ Port3 [0]

Mnemonic: P4								Address: E8h
7	6	5	4	3	2	1	0	Reset
P4.7	P4.6	P4.5	P4.4	P4.3	P4.2	P4.1	P4.0	FFh

P4.7~0: Port4 [7] ~ Port4 [0]

Mnemonic: P5								Address: D8h
7	6	5	4	3	2	1	0	Reset
--	--	--	--	P5.3	P5.2	P5.1	P5.0	FFh

P5.3~0: Port5 [3] ~ Port5 [0]

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6. Multiplication Division Unit (MDU)

This on-chip arithmetic unit provides 32-bit division, 16-bit multiplication, shift and normalize features. All operations are unsigned integer operations.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Multiplication Division Unit										
PCON	Power control	87H	SMOD	MDUF	-	-	-	-	STOP	IDLE
ARCON	Arithmetic Control register	EFh	MDEF	MDOV	SLR	SC[4:0]				
MD0	Multiplication/Division Register 0	E9h	MD0[7:0]							
MD1	Multiplication/Division Register 1	EAh	MD1[7:0]							
MD2	Multiplication/Division Register 2	EBh	MD2[7:0]							
MD3	Multiplication/Division Register 3	ECh	MD3[7:0]							
MD4	Multiplication/Division Register 4	EDh	MD4[7:0]							
MD5	Multiplication/Division Register 5	EEh	MD5[7:0]							

6.1. Operating registers

The MDU is controlled by seven registers, which are memory mapped as special function registers. The arithmetic unit allows operations concurrently to, and independent of, the CPU's activity.

Operands and results registers are MD0 to MD5, and the control register is ARCON. Any calculation of the MDU overwrites its operands.

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Mnemonic: ARCON Address: EFh

7	6	5	4	3	2	1	0	Reset
MDEF	MDOV	SLR	SC[4:0]					00H

MDEF: Multiplication Division Error Flag.
The MDEF is a read-only error flag. It indicates an improperly performed operation (when one of the arithmetic operations has been restarted or interrupted by a new operation). The error flag mechanism is automatically enabled with the first write to MD0 and disabled with the final read instruction from MD3 (multiplication or shift/normalizing) or MD5 (division) in the third phase.

The error flag is set when:
1. A calculation is in progress and a write access to MDx registers occurs restarting, or interrupting, the calculation.
2. The Error flag mechanism is enabled and a read access to MDx registers occurs (don't cause interrupt calculations)

The error flag is reset only if:
The second phase is finished and a read access to the Mdx registers occurs (arithmetic operation successfully completed).

MDOV: Multiplication Division Overflow flag. The overflow flag is read only.
The overflow flag is set when:
Division by zero was requested
Multiplication with a result greater then 0000FFFFh
Start of normalizing if the most significant bit of MD3 is set (MD3.7=1)
The overflow flag is reset when:
Write access to MD0 register (start of the first phase)

SLR: Shift direction bit.
SLR = 0 – shift left operation.
SLR = 1 – shift right operation.

SC[4:0]: Shift counter.
When preset with 00000b, normalizing is selected. After normalized, SC[4:0] contains the number of normalizing shifts performed. When SC[4:0] ≠ 0, shift operation is started. The number of shifts performed is determined by the count written to SC[4:0]. SC[4] is MSB and SC[0] is LSB.

6.2. Operation of the MDU

The operation of the MDU consists of three phases:

6.2.1 First phase : loading the MDx registers, x = 0~5 :

The type of calculation the MDU has to perform is selected by the order in which the MDx registers are written to. A write to MD0 is the first transfer to be done in any case. Next writes must be done as shown in the table below to determine the MDU operation. The last write will start the selected operation.

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Operation	32bit/16bit	16bit/16bit	16bit x 16bit	shift/normalizing
First write	MD0 Dividend Low MD1 Dividend MD2 Dividend MD3 Dividend High MD4 Divisor Low	MD0 Dividend Low MD1 Dividend High MD4 Divisor Low	MD0 Multiplicand Low MD4 Multiplicator Low MD1 Multiplicand High	MD0 LSB MD1 MD2 MD3 MSB
Last write	MD5 Divisor High	MD5 Divisor High	MD5 Multiplicator High	ARCON start conversion

Table 6-1 : MDU registers write sequence

A write to MD0 is the first transfer to be done in any case. Next writes must be done as shown in table 6.1 to determine the MDU operation. The selected operation starts after the last write.

6.2.2. Second phase: calculation.

During the calculation period, the MDU works in parallel to the CPU. When the calculation is complete, the hardware will set the MDUF bit to one. The flag will be cleared at the next calculation.

Mnemonic: PCON Address: 87h

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF	-	PMW	-	-	STOP	IDLE	40H

MDUF: MDU finish flag.
When the MDU calculation is completed, the MDUF will be set by the hardware. It will be cleared by the hardware at the next calculation.

The following table provides the execution time for each mathematical operation.

Table 6-2 MDU execution times

Operation	**Number of Tclk**
Division 32bit/16bit	17 clock cycles
Division 16bit/16bit	9 clock cycles
Multiplication	11 clock cycles
Shift	min 3 clock cycles, max 18 clock cycles
Normalize	min 4 clock cycles, max 19 clock cycles

6.2.3. Third phase: reading the result from the MDx registers.

The sequence of reading out the MDx registers is not critical. The last read (from MD5 in division operation, or MD3 in multiplication, shift and normalizing) signals the end of the whole calculation.

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Table 6-3 : MDU registers read sequence

Operation	32Bit/16Bit	16Bit/16Bit	16Bit x 16Bit	shift/normalizing
First read	MD0	MD0	MD0	MD0
	Quotient Low	Quotient Low	Product Low	LSB
	MD1	MD1	MD1	MD1
	Quotient	Quotient High	Product	
	MD2		MD2	MD2
	Quotient		Product	
	MD3			
	Quotient High			
	MD4	MD4		
	Remainder Low	Remainder Low		
Last read	MD5	MD5	MD3	MD3
	Remainder High	Remainder High	Product High	MSB

Further explanations of the normalization and shift operations.
In a normalization operation, all leading zeroes in registers MD0 to MD3 are removed with a series of shift left operations. The whole operation is completed when the MSB (most significant bit) of MD3 register contains a '1'. After normalization, bits ARCON.4 (MSB) to ARCON.0 (LSB) contain the number of shift left operations.
In a shift operation, SLR bit (ARCON.5) has to contain the shift direction, and ARCON.4 to ARCON.0 represent the shift count (which must not be 0). During shift, zeroes come into the left, or right, end of the registers MD0, or MD3, respectively.

6.3 Normalizing

All leading zeroes of integers variables in registers MD0 to MD3 are removed by shift left operations. The whole operation is completed when the MSB (most significant bit) of MD3 register contains a '1'.
After normalizing, bits ARCON.4 (MSB) to ARCON.0 (LSB) contain the number of shift left operations, which were done.

6.4 Shifting

SLR bit (ARCON.5) has to contain the shift direction, and ARCON.4 to ARCON.0 the shift count which must not be 0). During shift, zeroes come into the left or right end of the registers MD0 or MD3, respectively.

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7. Timer 0 and Timer 1

The mcu has three 16-bit timer/counter registers: Timer 0, Timer 1 and Timer 2. All can be configured for counter, or timer, operations.

In timer mode, the Timer 0 register, or Timer 1 register, is incremented every 12 machine cycles, which means that it is incremented every 12 periods of the clk signal.

In counter mode, the Timer 0 register, or Timer 1 register, is incremented when a falling edge is detected at the corresponding input pin T0, or T1. Since it takes 2 machine cycles to recognize a 1-to-0 event, the maximum input count rate is 1/2 of the oscillator frequency. There are no restrictions on the duty cycle, however to ensure proper recognition of 0 or 1 state, an input should be stable for at least 1 machine cycle.

Four operating modes can be selected for Timer 0 and Timer 1. Two Special Function registers (TMOD and TCON) are used to select the appropriate mode.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	RESET
Timer 0 and 1											
TL0	Timer 0 , low byte	8Ah	TL0[7:0]								00h
TH0	Timer 0 , high byte	8Ch	TH0[7:0]								00h
TL1	Timer 1 , low byte	8Bh	TL1[7:0]								00h
TH1	Timer 1 , high byte	8Dh	TH1[7:0]								00h
TMOD	Timer Mode Control	89h	GATE	C/T	M1	M0	GATE	C/T	M1	M0	00h
TCON	Timer/Counter Control	88h	TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00h

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7.1 Timer/counter mode control register (TMOD)

Mnemonic: TMOD — Address: 89h

7	6	5	4	3	2	1	0	Reset
GATE	C/T	M1	M0	GATE	C/T	M1	M0	00H
Timer 1				Timer 0				

GATE: If set, it enables the external gate control (pin INT0 or INT1 for Counter 0 or 1, respectively). When INT0 or INT1 is high, and TRx bit is set (see TCON register), a counter is incremented at every falling edge on T0 or T1 input pin.

C/T: Selects Timer or Counter operation. When set to 1, a counter operation is performed, when cleared to 0, the corresponding register will function as a timer.

M[1:0]: Selects mode for Timer/Counter 0 or Timer/Counter 1.

M1	M0	MODE	Function
0	0	Mode 0	13-bit counter/timer, with 5 lower bits in TL0 or TL1 register and 8 bits in TH0 or TH1 register (for Timer 0 and Timer 1, respectively). The 3 high order bits of TL0 and TL1 are hold at zero.
0	1	Mode 1	16-bit counter/timer.
1	0	Mode 2	8 -bit auto-reload counter/timer. The reload value is kept in TH0 or TH1, while TL0 or TL1 is incremented every machine cycle. When TLx overflows, a value from THx is copied to TLx.
1	1	Mode 3	If Timer 1 M1 and M0 bits are set to 1, Timer 1 stops. If Timer 0 M1 and M0 bits are set to 1, Timer 0 acts as two independent 8 bit timers / counters.

7.2 Timer/counter control register (TCON)

Mnemonic: TCON — Address: 88h

7	6	5	4	3	2	1	0	Reset
TF1	TR1	TF0	TR0	IE1	IT1	IE0	IT0	00H

TF1: Timer 1 overflow flag set by hardware when Timer 1 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR1: Timer 1 Run control bit. If cleared, Timer 1 stops.

TF0: Timer 0 overflow flag set by hardware when Timer 0 overflows. This flag can be cleared by software and is automatically cleared when interrupt is processed.

TR0: Timer 0 Run control bit. If cleared, Timer 0 stops.

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IE1: Interrupt 1 edge flag. Set by hardware, when falling edge on external pin INT1 is observed. Cleared when interrupt is processed.

IT1: Interrupt 1 type control bit. Selects falling edge or low level on input pin to cause interrupt.

IE0: Interrupt 0 edge flag. Set by hardware, when falling edge on external pin INT0 is observed. Cleared when interrupt is processed.

IT0: Interrupt 0 type control bit. Selects falling edge or low level on input pin to cause interrupt.

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8 Timer 2 and Capture/Compare Unit

Timer 2 is not only a 16-bit timer, but also a 4-channel unit with compare, capture and reload functions. It is very similar to the programmable counter array (PCA) in other MCUs except for the pulse width modulation (PWM) function.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	
Timer 2 and Capture Compare Unit											
AUX	Auxiliary register	91H	BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	
T2CON	Timer 2 control	C8h	T2PS	CC0 FR	--	T2R[1:0]		T2CM	T2I[1:0]		
CCCON	Compare/Capture Control	C9h	CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	
CCEN	Compare/Capture Enable register	C1h	COC AH3	COC AL3	COC AH2	COC AL2	COC AH1	COC AL1	COC AH0	COC AL0	
TL2	Timer 2, low byte	CCh	TL2[7:0]								
TH2	Timer 2, high byte	CDh	TH2[7:0]								
CRCL	Compare/Reload/ Capture register, low byte	CAh	CRCL[7:0]								
CRCH	Compare/Reload/ Capture register, high byte	CBh	CRCH[7:0]								
CCL1	Compare/Capture register 1, low byte	C2h	CCL1[7:0]								
CCH1	Compare/Capture register 1, high byte	C3h	CCH1[7:0]								
CCL2	Compare/Capture register 1, low byte	C4h	CCL2[7:0]								
CCH2	Compare/Capture register 2, high byte	C5h	CCH2[7:0]								
CCL3	Compare/Capture register 3, low byte	C6h	CCL3[7:0]								
CCH3	Compare/Capture register 3, high byte	C7h	CCH3[7:0]								

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

P4CC: P4CC = 0 – Capture/Compare function on P1.
P4CC = 1 – Capture/Compare function on P4.

Mnemonic: T2CON Address: C8h

7	6	5	4	3	2	1	0	Reset
T2PS	CC0FR	–	T2R[1:0]		T2CM	T2I[1:0]		00H

T2PS: Prescaler select bit:
T2PS = 0 – timer 2 is clocked with 1/12 of the oscillator frequency.
T2PS = 1 – timer 2 is clocked with 1/24 of the oscillator frequency.

CC0FR: Select active edge:
CC0FR = 0 – falling edge
CC0FR = 1 – rising edge

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T2R[1:0]: Timer 2 reload mode selection
T2R[1:0] = 0X – Reload disabled
T2R[1:0] = 10 – Mode 0
T2R[1:0] = 11 – Mode 1

T2CM: Timer 2 Compare mode selection
T2CM = 0 – Mode 0
T2CM = 1 – Mode 1

T2I[1:0]: Timer 2 input selection
T2I[1:0] = 00 – Timer 2 stop
T2I[1:0] = 01 – Input frequency f/12 or f/24
T2I[1:0] = 10 – Timer 2 is incremented by external signal at pin T2
T2I[1:0] = 11 – internal clock input is gated to Timer 2

Mnemonic: CCCON Address: C9h

7	6	5	4	3	2	1	0	Reset
CCI3	CCI2	CCI1	CCI0	CCF3	CCF2	CCF1	CCF0	00H

CCI3: Compare/Capture 3 interrupt control bit. Enabled if equal to 1.
CCI2: Compare/Capture 2 interrupt control bit. Enabled if equal to 1.
CCI1: Compare/Capture 1 interrupt control bit. Enabled if equal to 1.
CCI0: Compare/Capture 0 interrupt control bit. Enabled if equal to 1.

CCF3: Compare/Capture 3 flag set by hardware. This flag can be cleared by software.
CCF2: Compare/Capture 2 flag set by hardware. This flag can be cleared by software.
CCF1: Compare/Capture 1 flag set by hardware. This flag can be cleared by software.
CCF0: Compare/Capture 0 flag set by hardware. This flag can be cleared by software.

Note: Compare/Capture interrupt shares T2 interrupt vector.

Mnemonic: CCEN Address: C1h

7	6	5	4	3	2	1	0	Reset
COCAH3	COCAL3	COCAH2	COCAL2	COCAH1	COCAL1	COCAH0	COCAL0	00H

COCAH3,COCAL3: Compare/Capture mode for Channel 3.

COCAH3	COCAL3	Function
0	0	Compare/capture disable
0	1	Capture on rising edge at pin CC3
1	0	Compare enable
1	1	Capture on write operation into register CCL3

COCAH2,COCAL2: Compare/Capture mode for Channel 2.

COCAH2	COCAL2	Function
0	0	Compare/capture disable
0	1	Capture on rising edge at pin CC2
1	0	Compare enable
1	1	Capture on write operation into register CCL2

COCAH1,COCAL1: Compare/Capture mode for Channel 1.

COCAH1	COCAL1	Function
0	0	Compare/capture disable
0	1	Capture on rising edge at pin CC1
1	0	Compare enable
1	1	Capture on write operation into register CCL1

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COCAH0,COCAL0: Compare/Capture mode for Channel 0.

COCAH0	COCAL0	Function
0	0	Compare/capture disable
0	1	Capture on rising edge at pin CC0
1	0	Compare enable
1	1	Capture on write operation into register CCL0

8.1 Timer 2 function

Timer 2 can operate as timer, event counter, or gated timer as explained below.

8.1.1 Timer mode

In this mode Timer 2 can be incremented every 12 clocks (Fosc/12), or every 24 clocks (Fosc/24), depending on the 2:1 prescaler. The prescaler is selected by bit T2PS in register T2CON.

8.1.2 Event counter mode

In this mode, the timer is incremented when the state of signal T2 changes from 1 to 0. Signal T2 is sampled in every cycle. Timer 2 is incremented in the cycle following the one in which the transition was detected.

8.1.3 Gated timer mode

In this mode, the internal clock which increments timer 2 is gated by external signal T2.

8.1.4 Reload of Timer 2

Reload (16-bit reload from the CRC register) can be executed in the following two modes:

Mode 0: Reload signal is generated by a Timer 2 overflow - auto reload
Mode 1: Reload signal is generated by a negative transition at the corresponding input pin T2EX.

8.2 Compare function

In the four independent comparators, the value stored in any compare/capture register is compared to the contents of the timer register. Compare modes 0 and 1 are selected by bit T2CM. In both compare modes, the results of comparison arrive at Port 1 within the same machine cycle in which the internal compare signal is activated.

8.2.1 Compare Mode 0

In mode 0, when the value in Timer 2 equals the value of the compare register, the output signal changes from low to high. It goes back to a low level on timer overflow. In this mode, writing to the port will have no effect, because the input line from the internal bus and the write-to-latch line are disconnected. The following figure illustrates the function of compare mode 0.

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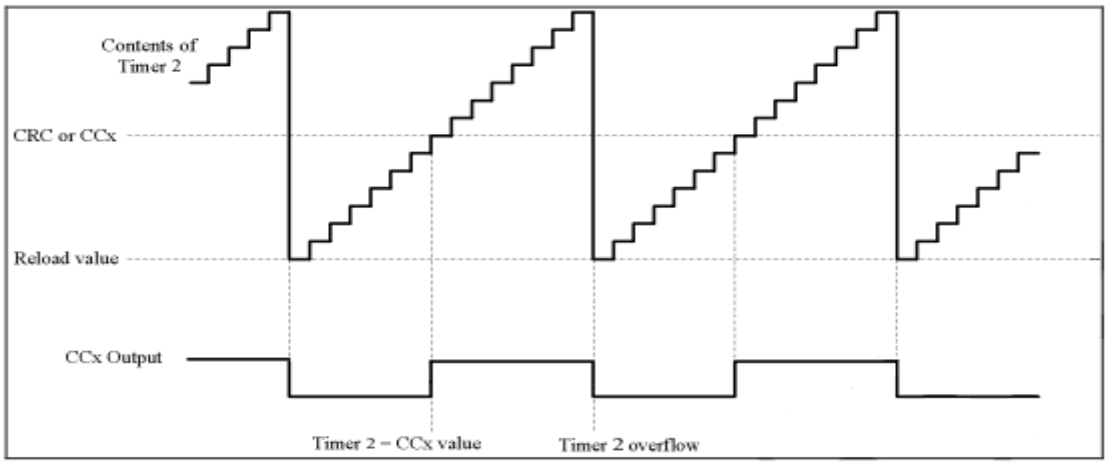

Fig. 8-1: Compare mode 0 function

8.2.2 Compare Mode 1

In compare mode 1, the transition of the output signal can be determined by software. A timer 2 overflow causes no output change. In this mode, both transitions of a signal can be controlled. Fig. 8-2 shows a functional diagram of a register/port configuration in compare Mode 1. In compare Mode 1, the value is written first to the “Shadow Register”, when compare signal is active, this value is transferred to the output register.

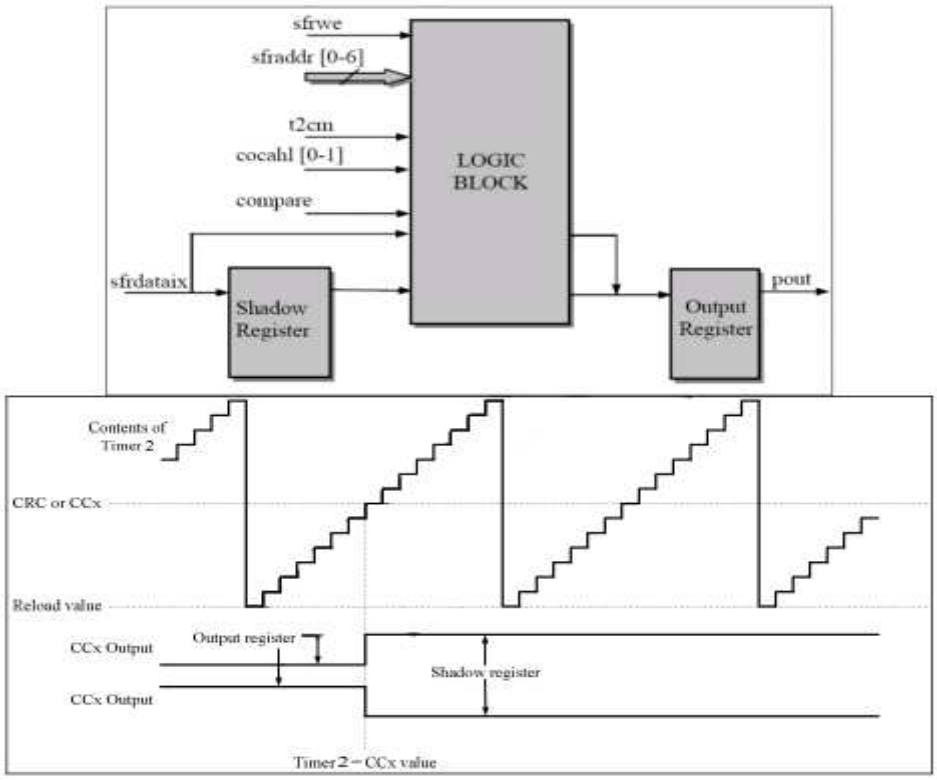

Fig. 8-2: Compare mode 1 function

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8.3 Capture function

Actual timer/counter contents can be saved into registers CCx, or CRC, upon an external event (mode 0), or a software write operation (mode 1).

8.3.1 Capture Mode 0

In mode 0, value capture of Timer 2 is executed when:

(a) Rising edge on input CC1-CC3
(b) Rising, or Falling, edge on input CC0 (depending on bit CC0FR)

The contents of Timer 2 will be latched into the appropriate capture register.

8.3.2 Capture Mode 1

In mode 1, value capture of timer 2 is caused by writing any value into the low-order byte of the dedicated capture register. The value written to the capture register is irrelevant to this function. The contents of Timer 2 will be latched into the appropriate capture register.

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9 Serial interface 0

The mcu contains one serial interface for data communication, called UART0. The communication rate can be set by configuring the baud rate in SFRs.

The two serial buffers consist of two separate registers, a transmit buffer and a receive buffer.

Writing data to the SFR S0BUF transfers the data to the serial output buffer and starts the transmission. Reading from the S0BUF reads data from the serial receive buffer. The serial port can simultaneously transmit and receive data. It can also buffer 1 byte at receive, which prevents the receive data from being lost if the CPU reads the second byte before the transmission of the first byte is completed.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Serial interface 0										
PCON	Power control	87h	SMOD	MDUF	--	--	--	--	STOP	IDLE
AUX	Auxiliary register	91h	BRS	P4CC	P4SPI	--	P4 IIC	P0 KBI	--	DPS
S0CON	Serial Port 0 control register	98h	SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0
S0RELL	Serial Port 0 reload register low byte	AAh	S0 REL.7	S0 REL.6	S0 REL.5	S0 REL.4	S0 REL.3	S0 REL.2	S0 REL.1	S0 REL.0
S0RELH	Serial Port 0 reload register high byte	BAh	--	--	--	--	--	--	S0 REL.9	S0 REL.8
S0BUF	Serial Port 0 data buffer	99h	S0BUF[7:0]							

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

Mnemonic: S0CON Address: 98h

7	6	5	4	3	2	1	0	Reset
SM0	SM1	SM20	REN0	TB80	RB80	TI0	RI0	00H

SM0,SM1: Serial Port 0 mode selection.

SM0	SM1	Mode
0	0	0
0	1	1
1	0	2
1	1	3

The 4 modes of UART0, Mode 0 ~ 3, will be explained later.

SM20: Enables multiprocessor communication feature
REN0: If set, enables serial reception. Cleared by software to disable reception.
TB80: The 9th transmitted data bit in modes 2 and 3. Set or cleared by the CPU,depending on the function it performs such as parity check, multiprocessor communication etc.
RB80: In modes 2 and 3, it is the 9th data bit received. In mode 1, if SM20 is 0, RB80 is the stop bit. In mode 0, this bit is not used. Must be cleared by software.
TI0: Transmit interrupt flag, set by hardware after completion of a serial transfer. Must be cleared by software.
RI0: Receive interrupt flag, set by hardware after completion of a serial reception.Must be cleared by software.

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9.1 Serial interface 0

The Serial Interface 0 can operate in the following 4 modes:

SM0	SM1	Mode	Description	Baud Rate
0	0	0	Shift register	Fosc/12
0	1	1	8-bit UART	Variable
1	0	2	9-bit UART	Fosc/32 or Fosc/64
1	1	3	9-bit UART	Variable

Fosc is the crystal, or oscillator, frequency.

9.1.1 Mode 0

Pin RXD0 serves as input and output. TXD0 outputs the shift clock. 8 bits are transmitted with LSB first. The baud rate is fixed at 1/12 of the crystal frequency. Reception is initialized in Mode 0 by setting the flags in S0CON as follows: RI0 = 0 and REN0 = 1. In the other modes, a start bit when REN0 = 1 starts receiving serial data.

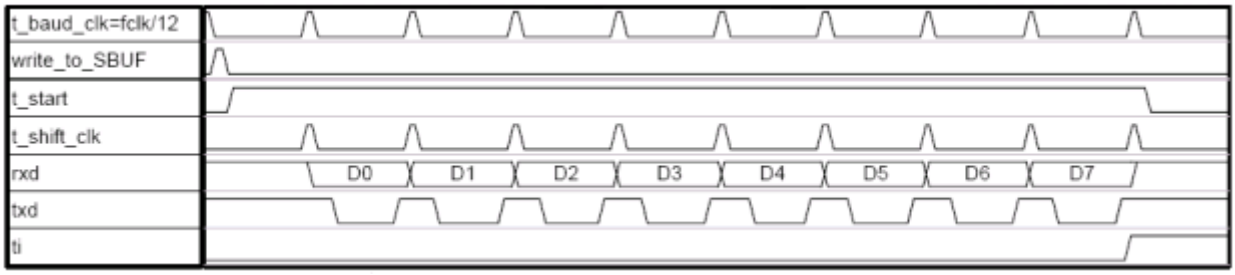

Fig. 9-1: Transmit mode 0 for Serial 0

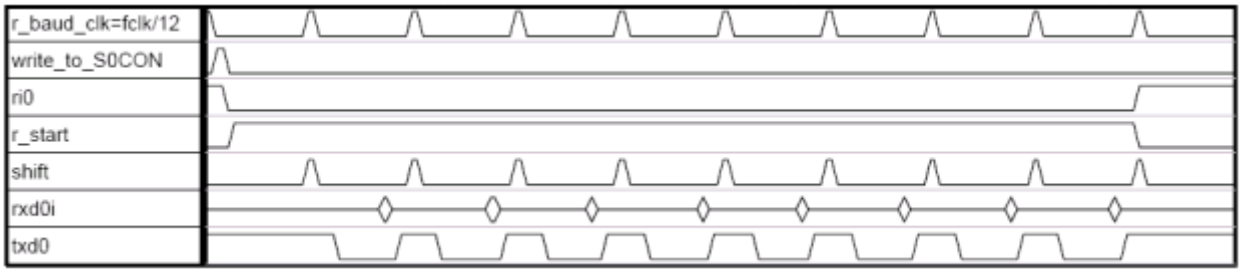

Fig. 9-2: Receive mode 0 for Serial 0

9.1.2 Mode 1

Here Pin RXD0 serves as input, and TXD0 serves as serial output. No external shift clock is used, 10 bits are transmitted: a start bit (always 0), 8 data bits (LSB first), and a stop bit (always 1). On receive, a start bit synchronizes the transmission, 8 data bits are available by reading S0BUF, and a stop bit sets the flag RB80 in the SFR S0CON. In mode 1, either the internal baud rate generator, or timer 1, can be used to specify the desired baud rate.

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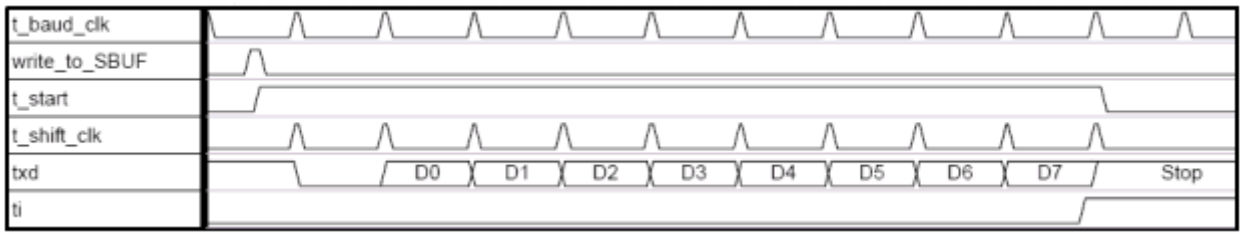

Fig. 9-3: Transmit mode 0 for Serial 0

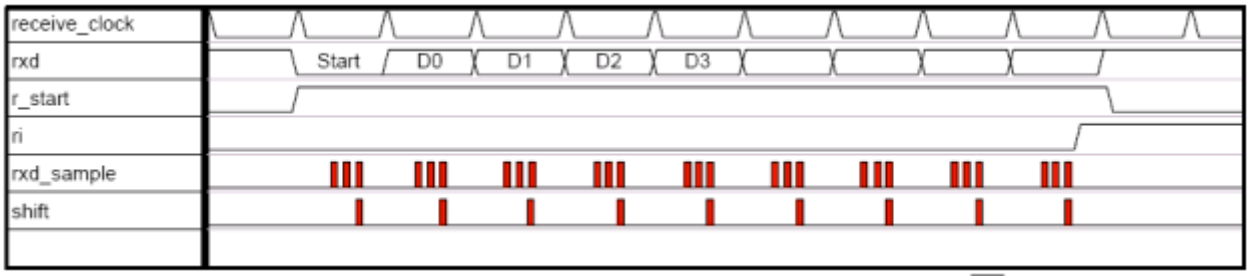

Fig. 9-4: Receive mode 1 for Serial 0

9.1.3 Mode 2

This mode is similar to Mode 1, but with two differences. The baud rate is fixed at 1/32 (SMOD=1) or 1/64(SMOD=0) of oscillator frequency, and 11 bits are transmitted or received: a start bit (0), 8 data bits (LSB first), a programmable Bit 9, and a stop bit (1). Bit 9 can be used to control the parity of the serial interface: at transmission, bit TB80 in S0CON is output as Bit 9, and at receive, Bit 9 affects RB80 in SFR S0CON.

9.1.4 Mode 3

In Mode 3, either the internal baud rate generator, or timer 1, can be used to specify the baud rate. It is otherwise the same to mode 2.

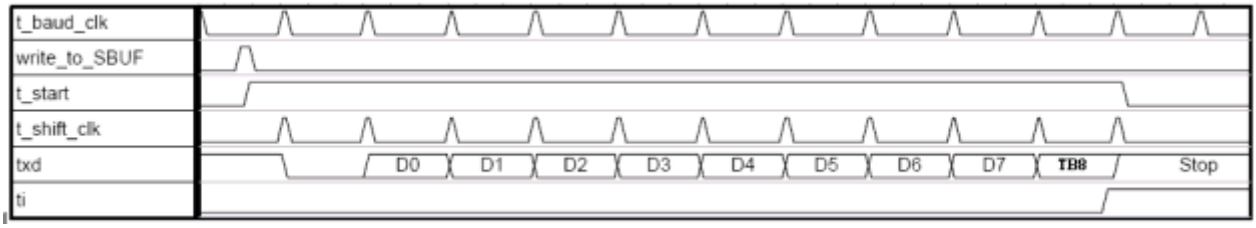

Fig. 9-5: Transmit modes 2 and 3 for Serial 0

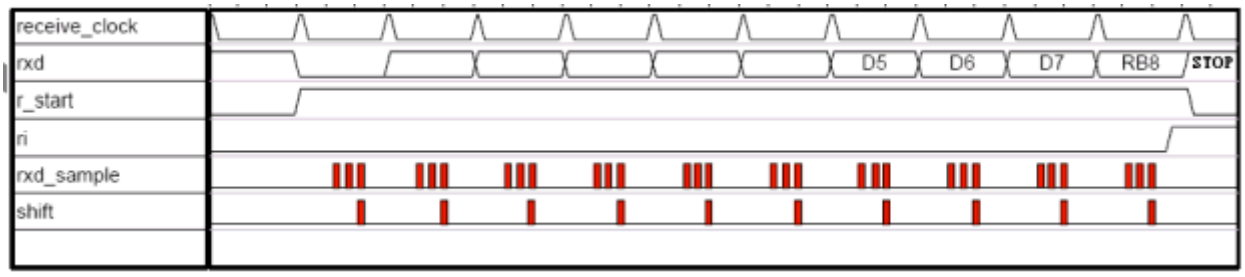

Fig. 9-6: Receive modes 2 and 3 for Serial 0

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9.2 Multiprocessor communication of Serial Interface 0

The feature of receiving 9 bits in Modes 2 and 3 of Serial Interface 0, can be used for multiprocessor communication. In this case, the slave processors have bit SM20 in S0CON set to 1. When the master processor outputs slave's address, it sets the Bit 9 to 1, causing a serial port receive interrupt in all the slaves. The slave processors compare the received byte with their network address. If matched, the addressed slave will clear SM20 and receive the rest of the message, while other slaves will leave SM20 bit unaffected and ignore this message. After addressing the slave, the host will output the rest of the message with the Bit 9 set to 0, so no serial port receive interrupt will be generated in unselected slaves.

9.3 Baud rate generator

9.3.1 Serial interface 0 modes 1 and 3

(a) When BRS = 0 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{SMOD} \times F_{OSC}}{32 \times 12 \times (256 - TH1)}$$

(b) When BRS = 1 (in SFR AUX):

$$\text{Baud Rate} = \frac{2^{SMOD} \times F_{OSC}}{64 \times (2^{10} - S0REL)}$$

9.4 Clock source for the baud rate generator

Because serial communications require an accurate clock source, it is not recommended to use the internal OSC as the system clock source when the serial interface functions are used. There may be a 20% variance in the frequency of the internal oscillator. The user should choose a clock source from either the external crystal or an external oscillator.

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10 Watchdog timer

The Watch Dog Timer (WDT) is an 8-bit free-running counter that generates a reset signal if it overflows. The WDT is useful for systems which are susceptible to noise, power glitches, or electrostatic discharge that might cause a software dead loop or runaway. It can help the application software to recover from an abnormal condition.

The WDT is independent from Timer0, Timer1, or Timer2. It is driven by a free running on-chip RC oscillator (250KHz). It will keep on running even after the system clock has been turned off (for example, in sleep mode). During normal operation, or sleep mode, a WDT time-out will cause the MCU to reset.

Following a reset, the application must check the WDTF bit of the WDTC register, to determine the source of the reset. After an external reset the watchdog timer is disabled and all its registers are cleared to zero. The WDT can be enabled at any time through bit WDTE of the WDTC register.

To prevent a WDT reset, the application software must periodically clear the WDT counter before its time-out period expires. The default WDT time-out period is approximately 16.38ms (WDTM [3:0] = 0100b). In order to select another time-out period, the WDT has a selectable divider input for the time base source clock. To select the required divider input, bits 3 ~ 0 (WDTM [3:0]) of Watch Dog Timer Control Register (WDTC) must be set accordingly.

$$WDTCLK = \frac{250\ KHz}{2^{WDTM}}$$

$$\text{Watchdog Reset Time} = \frac{256}{WDTCLK}$$

WDTM [3:0]	Divider (250 KHz RC oscillator in)	Time period @ 250KHz
0000	1	1.02ms
0001	2	2.05ms
0010	4	4.10ms
0011	8	8.19ms
0100	16	16.38ms (default)
0101	32	32.77ms
0110	64	65.54ms
0111	128	131.07ms
1000	256	262.14ms
1001	512	524.29ms
1010	1024	1.05s
1011	2048	2.10s
1100	4096	4.19s
1101	8192	8.39s
1110	16384	16.78s
1111	32768	33.55s

Table 10-1 : WDT clock source divider selection and time-out period.

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When WDTEN bit is set to 1, the watchdog function will be disabled no matter what the WDTE bit status is. When WDTEN bit is cleared to 0, the watchdog function will be enabled, provided that bit WDTE is set to 1 by the application. Bit WDTEN is set during device programming either via the external writer, or the ISP.

When the MCU is reset, the application should read the WDTEN control bit status, before setting bit WDTE. After bit WDTE set to 1, the 8 bit-counter starts counting, based on the selected time base source clock, as set by bits WDTM [3:0]. If allowed to overflow, it will set the WDTF flag and will automatically reset the MCU. Flag WDTF can be cleared by software, or a reset caused by an external source, or power on.

After the MCU has been reset by any source, bit WDTE will be cleared to 0 automatically.

Once the watchdog is started it cannot be stopped. It must be refreshed in order to avoid an MCU reset. It can be refreshed by writing 0x55 to the Watch Dog Timer refresh Key (WDTK) register. This will clear the content of the 8-bit counter and let the counter re-start.

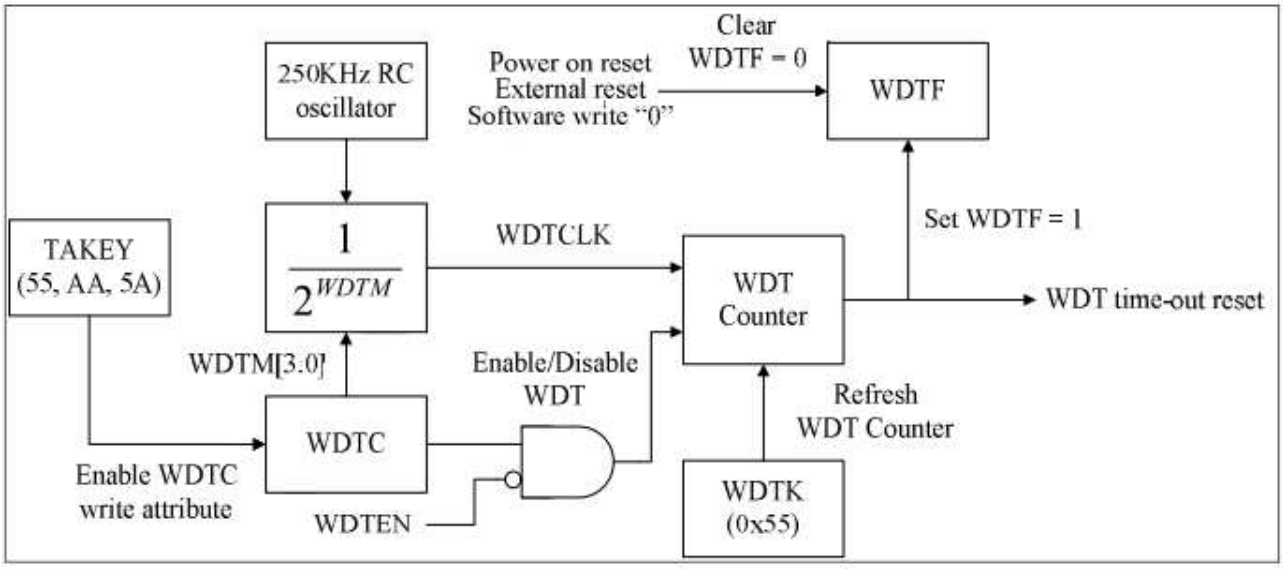

Fig. 10-1: Watchdog timer block diagram

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Watchdog Timer										
TAKEY	Time Access Key register	F7h	TAKEY [7:0]							
WDTC	Watchdog timer control register	B6h	WDTF	--	WDTE	--	WDTM [3:0]			
WDTK	Watchdog timer refresh key	B7h	WDTK[7:0]							

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Mnemonic: TAKEY Address: F7h

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

Watchdog timer control register (WDTC) is read-only by default; software must write three specific values 55h, AAh and 5Ah sequentially to the TAKEY register in order to enable the WDTC write attribute.

The sequence of writes that must occur is:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```

Mnemonic: WDTC Address: B6h

7	6	5	4	3	2	1	0	Reset
WDTF	--	WDTE	--	WDTM [3:0]				04H

WDTF: Watchdog timer reset flag.
When the MCU is reset by the watchdog, the WDTF flag will be set to one by hardware. This flag is cleared by software, or by an external, or power-on, reset.

WDTE: Control bit used to enable Watchdog timer.
The WDTE bit can be used only if WDTEN is "0". If the WDTEN bit is "0", then WDT can be disabled / enabled by the WDTE bit.
0: Disable WDT.
1: Enable WDT.

The WDTE bit cannot be used if WDTEN is "1". That is, if the WDTEN bit is "1", WDT is always disabled no matter what the WDTE bit status is. The WDTE bit can be read and written.

WDTM [3:0]: WDT clock source divider bit. Please see table 10-1 to reference the WDT time-out period.

Mnemonic: WDTK Address: B7h

7	6	5	4	3	2	1	0	Reset
WDTK[7:0]								00H

WDTK: Watchdog timer refresh key.
The application must write 0x55 into the WDTK register, for the watchdog timer to be cleared.
For example, enable the watchdog with a time-out reset period of 327.68ms.

a. Clear WDTEN to “0” (bit 7 of OP3 in the information block – refer to the ISP section for details).
b. Perform the following write sequence:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah ; WDTC write attribute is now enabled.
MOV WDTC, #28h ; Set WDTM [3:0] = 1000b. Set WDTE =1 to enable the WDT.
MOV WDTK, #55h ; Clear WDT timer to 0.
```


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11 Interrupts

The MCU provides 12 interrupt sources with four priority levels. Each source has its own request flag(s), located in a special function register. Each interrupt requested by the corresponding flag may be individually enabled, or disabled, by the interrupt enable bits in SFR's IEN0, IEN1, and IEN2.

When an interrupt occurs, the MCU will vector to the predetermined address as shown in Table 11-1. Once an interrupt service has begun, it can be interrupted only by a higher priority interrupt. The interrupt service is terminated by a return from instruction RETI. When a RETI is executed, the MCU will return to the instruction that would have been executed next when the interrupt occurred.

When the interrupt condition occurs, the MCU will also indicate this by setting a flag bit. This bit is set regardless of whether the interrupt is enabled or disabled. Each interrupt flag is sampled by the hardware once every machine cycle. If the sampling process indicates that an enabled interrupt is pending, then the corresponding interrupt request flag is set. The interrupt will be acknowledged by the hardware during the next instruction cycle, forcing an LCALL to the appropriate vector address.

The time required for an interrupt to be serviced varies depending on the state of the MCU when the interrupt occurs. If the MCU is servicing an interrupt with equal or greater priority, the new interrupt will not be serviced until the current interrupt service is complete. In other cases, the response time depends on the instruction that is currently being executed. The fastest possible response to an interrupt is 7 machine cycles. This includes one machine cycle to detect the interrupt and six cycles to perform the LCALL.

Interrupt Request Flags	Interrupt Vector Address	Interrupt Number *(use Keil C Tool)
IE0 – External interrupt 0	0003h	0
TF0 – Timer 0 interrupt	000Bh	1
IE1 – External interrupt 1	0013h	2
TF1 – Timer 1 interrupt	001Bh	3
RI0/TI0 – Serial channel 0 interrupt	0023h	4
TF2/EXF2 – Timer 2 interrupt	002Bh	5
PWMIF – PWM interrupt	0043h	8
SPIIF – SPI interrupt	004Bh	9
ADCIF – A/D converter interrupt	0053h	10
KBIIF – keyboard Interface interrupt	005Bh	11
LVIIF – Low Voltage Interrupt	0063h	12
IICIF – IIC interrupt	006Bh	13

Table 11-1: Interrupt vectors

*See Keil C about C51 User's Guide about Interrupt Function description

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Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
Interrupt										
IEN0	Interrupt Enable 0 register	A8h	EA	--	ET2	ES0	ET1	EX1	ET0	EX0
IEN1	Interrupt Enable 1 register	B8h	EXEN2	--	IEIIC	IELVI	IEKBI	IEADC	IESPI	IE PWM
IRCON	Interrupt request register	C0h	EXF2	TF2	IICIF	LVIIF	KBIIF	ADCIF	SPIIF	PWM IF
IP0	Interrupt priority level 0	A9h	--	--	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0
IP1	Interrupt priority level 1	B9h	--	--	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0

Mnemonic: IEN0 Address: A8h

7	6	5	4	3	2	1	0	Reset
EA	–	ET2	ES0	ET1	EX1	ET0	EX0	00h

EA: EA=0 – Disable all interrupt.
EA=1 – Enable all interrupt.
ET2: ET2=0 – Disable Timer 2 overflow or external reload interrupt.
ET2=1 – Enable Timer 2 overflow or external reload interrupt.
ES0: ES0=0 – Disable Serial channel 0 interrupt.
ES0=1 – Enable Serial channel 0 interrupt.
ET1: ET1=0 – Disable Timer 1 overflow interrupt.
ET1=1 – Enable Timer 1 overflow interrupt.
EX1: EX1=0 – Disable external interrupt 1.
EX1=1 – Enable external interrupt 1.
ET0: ET0=0 – Disable Timer 0 overflow interrupt.
ET0=1 – Enable Timer 0 overflow interrupt.
EX0: EX0=0 – Disable external interrupt 0.
EX0=1 – Enable external interrupt 0.

Mnemonic: IEN1 Address: B8h

7	6	5	4	3	2	1	0	Reset
EXEN2	--	IEIIC	IELVI	IEKBI	IEADC	IESPI	IEPWM	00H

EXEN2: Timer 2 reload interrupt enable.
EXEN2 = 0 – Disable Timer 2 external reload interrupt.
EXEN2 = 1 – Enable Timer 2 external reload interrupt.
IEIIC: IIC interrupt enable.
IEIICS = 0 – Disable IIC interrupt.
IEIICS = 1 – Enable IIC interrupt.
IELVI: LVI interrupt enable.
IELVI = 0 – Disable LVI interrupt.
IELVI = 1 – Enable LVI interrupt.
IEKBI: KBI interrupt enable.
IEKBI = 0 – Disable KBI interrupt.
IEKBI = 1 – Enable KBI interrupt.
IEADC: A/D converter interrupt enable
IEADC = 0 – Disable ADC interrupt.
IEADC = 1 – Enable ADC interrupt.
IESPI: SPI interrupt enable.
IESPI = 0 – Disable SPI interrupt.
IESPI = 1 – Enable SPI interrupt.
IEPWM: PWM interrupt enable.

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IEPWM = 0 – Disable PWM interrupt.
IEPWM = 1 – Enable PWM interrupt

Mnemonic: IRCON Address: C0h

7	6	5	4	3	2	1	0	Reset
EXF2	TF2	IICIF	LVIIF	KBIIF	ADCIF	SPIIF	PWMIF	00H

EXF2: Timer 2 external reloads flag. Must be cleared by software.
TF2: Timer 2 overflows flag. Must be cleared by software.
IICIF: IIC interrupt flag.
LVIIF: LVI interrupt flag.
KBIIF: KBI interrupt flag.
ADCIF: A/D converter end interrupt flag.
SPIIF: SPI interrupt flag.
PWMIF: PWM interrupt flag. Must be cleared by software.

11.1 Priority level structure

All interrupt sources are combined in groups:

Groups	
External interrupt 0	PWM interrupt
Timer 0 interrupt	SPI interrupt
External interrupt 1	ADC interrupt
Timer 1 interrupt	KBI interrupt
Serial channel 0 interrupt	LVI interrupt
Timer 2 interrupt	IIC interrupt

Table 11-2: Priority level groups

Each group of interrupt sources can be programmed individually to one of four priority levels by setting, or clearing, one bit in the special function register IP0 and one in IP1. If requests of the same priority level will be received simultaneously, an internal polling sequence determines which request is serviced first.

Mnemonic: IP0 Address: A9h

7	6	5	4	3	2	1	0	Reset
--	--	IP0.5	IP0.4	IP0.3	IP0.2	IP0.1	IP0.0	00H

Mnemonic: IP1 Address: B9h

7	6	5	4	3	2	1	0	Reset
--	--	IP1.5	IP1.4	IP1.3	IP1.2	IP1.1	IP1.0	00H

IP1.x	IP0.x	Priority Level
0	0	Level0 (lowest)
0	1	Level1
1	0	Level2
1	1	Level3 (highest)

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Table 11-3: Priority levels

Bit	Groups	
IP1.0, IP0.0	External interrupt 0	PWM interrupt
IP1.1, IP0.1	Timer 0 interrupt	SPI interrupt
IP1.2, IP0.2	External interrupt 1	ADC interrupt
IP1.3, IP0.3	Timer 1 interrupt	KBI interrupt
IP1.4, IP0.4	Serial channel 0	LVI interrupt
IP1.5, IP0.5	Timer 2 interrupt	IIC interrupt

Table 11-4: Priority Groups

Interrupt source	Sequence
External interrupt 0	Polling sequence
PWM interrupt	
Timer 0 interrupt	
SPI interrupt	
External interrupt 1	
ADC interrupt	
Timer 1 interrupt	
KBI interrupt	
Serial channel 0 interrupt	
LVI interrupt	
Timer 2 interrupt	
IIC interrupt	

Table 11-5: Polling sequence

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12 Power Management Unit

In order to save power, the power management unit provides two power management modes, IDLE and STOP.

Mnemonic: PCON Address: 87h

7	6	5	4	3	2	1	0	Reset
SMOD	MDUF	--	--	--	--	STOP	IDLE	40H

STOP: Stop mode control bit. Setting this bit invokes the Stop Mode. It always reads 0.
IDLE: Idle mode control bit. Setting this bit invokes the Idle Mode. It always reads 0.

12.1 Idle mode

Setting the IDLE bit of PCON register invokes the IDLE mode. The IDLE mode leaves internal clocks and peripherals running. Power consumption drops because the CPU is not active. The CPU can exit the IDLE state with any one of the interrupts or a reset.

12.2 Stop mode

Setting the STOP bit of PCON register invokes the STOP mode. All internal clocking in this mode is turned off. The CPU will exit this state from a no-clocked external interrupt or a reset condition. Internally generated interrupts (timer, serial port ...) are not useful since they require clocking activity.

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13 Pulse Width Modulation (PWM)

The MCU provides four PWM channel outputs. The interrupt vector for the unit is 43h.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
PWM										
PWMC	PWM Control register	B5h	PWMCS[2:0]			--	PWM 3EN	PWM 2EN	PWM 1EN	PWM 0EN
PWMD0H	PWM 0 Data register high byte	BCh	PWM P0	--	--	--	--	--	PWMD0[9:8]	
PWMD0L	PWM 0 Data register low byte	BDh	PWMD0[7:0]							
PWMD1H	PWM 0 Data register high byte	BEh	PWM P1	--	--	--	--	--	PWMD1[9:8]	
PWMD1L	PWM 1 Data register low byte	BFh	PWMD1[7:0]							
PWMD2H	PWM 1 Data register high byte	B1h	PWM P2	--	--	--	--	--	PWMD2[9:8]	
PWMD2L	PWM 2 Data register low byte	B2h	PWMD2[7:0]							
PWMD3H	PWM 2 Data register high byte	B3h	PWM P3	--	--	--	--	--	PWMD3[9:8]	
PWMD3L	PWM 3 Data register low byte	B4h	PWMD3[7:0]							
PWMMDH	PWM Max Data register high byte	CEh	--	--	--	--	--	--	PWMMD0[9:8]	
PWMMDL	PWM Max Data register low byte	CFh	PWMMD[7:0]							

Mnemonic: PWMC Address: B5h

7	6	5	4	3	2	1	0	Reset
PWMCS[2:0]			--	PWM 3EN	PWM 2EN	PWM 1EN	PWM 0EN	00H

PWMCS[2:0]: PWM clock select.

PWMCS [2:0]	Mode
000	Fosc
001	Fosc/2
010	Fosc/4
011	Fosc/6
100	Fosc/8
101	Fosc/12
110	Timer 0 overflow
111	Timer 0 external input (P3.4/T0)

PWM3EN: PWM channel 3 enable control bit.
PWM3EN = 1 – PWM channel 3 enabled.
PWM3EN = 0 – PWM channel 3 disabled.

PWM2EN: PWM channel 2 enable control bit.
PWM2EN = 1 – PWM channel 2 enabled.
PWM2EN = 0 – PWM channel 2 disabled.

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PWM1EN: PWM channel 1 enable control bit.
PWM1EN = 1 – PWM channel 1 enabled.
PWM1EN = 0 – PWM channel 1 disabled.
PWM0EN: PWM 0 enable control bit.
PWM0EN = 1 – PWM channel 0 enabled.
PWM0EN = 0 – PWM channel 0 disabled.

Mnemonic: PWMD0H Address: BCh

7	6	5	4	3	2	1	0	Reset
PWMP0	--	--	--	--	--	PWMD0[9:8]		00H

Mnemonic: PWMD0L Address: BDh

7	6	5	4	3	2	1	0	Reset
PWMD0[7:0]								00H

PWMP0: PWM channel 0 idle polarity select.
"0" – PWM channel 0 will idle low.
"1" – PWM channel 0 will idle high.
PWMD0[9:0]: PWM channel 0 data register.

Mnemonic: PWMD1H Address: BEh

7	6	5	4	3	2	1	0	Reset
PWMP1	--	--	--	--	--	PWMD1[9:8]		00H

Mnemonic: PWMD1L Address: BFh

7	6	5	4	3	2	1	0	Reset
PWMD1[7:0]								00H

PWMP1: PWM channel 1 idle polarity select.
"0" – PWM channel 1 will idle low.
"1" – PWM channel 1 will idle high.
PWMD1[9:0]: PWM channel 1 data register.

Mnemonic: PWMD2H Address: B1h

7	6	5	4	3	2	1	0	Reset
PWMP2	--	--	--	--	--	PWMD2[9:8]		00H

Mnemonic: PWMD2L Address: B2h

7	6	5	4	3	2	1	0	Reset
PWMD2[7:0]								00H

PWMP2: PWM channel 2 idle polarity select.
"0" – PWM channel 2 will idle low.
"1" – PWM channel 2 will idle high.
PWMD2[9:0]: PWM channel 2 data register.

Mnemonic: PWMD3H Address: B3h

7	6	5	4	3	2	1	0	Reset
PWMP3	--	--	--	--	--	PWMD3[9:8]		00H

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Mnemonic: PWMD3L Address: B4h

7	6	5	4	3	2	1	0	Reset
PWMD3[7:0]								00H

PWMP3: PWM channel 3 idle polarity select.
"0" – PWM channel 3 will idle low.
"1" – PWM channel 3 will idle high.
PWMD3[9:0]: PWM channel 3 data register.

Mnemonic: PWMMDH Address: CEh

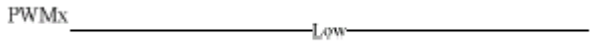
7	6	5	4	3	2	1	0	Reset
--	--	--	--	--	--	PWMMD[9:8]		00H

Mnemonic: PWMMDL Address: CFh

7	6	5	4	3	2	1	0	Reset
PWMMD[7:0]								00H

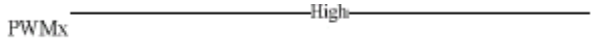
PWMMD[9:0]: PWM Max Data register.
PWM counts from 0000h to PWMMD[9:0]. When the contents of the PWM counter data equal those of PWMMD[9:0], an overflow occurs.

PWMPx = 0 & PWMDx = 00h



PWMPx = 0 & PWMDx ≠ 00h

PWMPx = 1 & PWMDx = 00h



PWMPx = 1 & PWMDx ≠ 00h

$$\text{PWM period} = \frac{\text{PWMMD} + 1}{\text{PWMclock}}$$

$$\text{Leading pulse} = \frac{\text{PWMDx}}{\text{PWMclock}}$$

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14 IIC function

The IIC module uses the SCL (clock) and the SDA (data) line to communicate with the external IIC interface. It can operate up to a speed of 400Kbps (maximum), as set by the IICBR [2:0] control bits. The IIC module provides 2 interrupts (RXIF, TXIF) at interrupt vector 6Bh. It generates START, repeated START and STOP signals automatically in master mode and can detect START, repeated START and STOP signals in slave mode. The maximum communication length and the number of devices that can be connected are limited by a maximum bus capacitance of 400pF.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
IIC Function										
AUX	Auxiliary register	91h	BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS
IICCTL	IIC control register	F9h	IICEN	--	MSS	MAS	RStart	IICBR[2:0]		
IICS	IIC Status register	F8h	MStart	RXIF	TXIF	RDR	TDR	RXAK	TXAK	RW
IICA1	IIC Address 1 register	FAh	IICA1[7:1]							MATCH1 or RW1
IICA2	IIC Address 2 register	FBh	IICA2[7:1]							MATCH2 or RW2
IICRWD	IIC Read/Write register	FCh	IICRWD[7:0]							
IICS2	IIC status2 register	FDh	--	--	--	--	AB_EN	BF_EN	AB_F	BF

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

P4IIC: P4IIC = 0 – IIC function on P1.
P4IIC = 1 – IIC function on P4.

Mnemonic: IICCTL Address: F9h

7	6	5	4	3	2	1	0	Reset
IICEN	--	MSS	MAS	RStart	IICBR[2:0]			04h

IICEN: Enable IIC module
IICEN = 1 is Enable
IICEN = 0 is Disable.
MSS: Master or slave mode select.
MSS = 1 is master mode.
MSS = 0 is slave mode.

NOTE: The MSS bit must be set first, before any other IIC module bit is set

MAS: Master address select (master mode only)
MAS = 0 is to use IICA1.
MAS = 1 is to use IICA2.
RStart: Re-start control bit (master mode only)

When this bit is set, the module will generate a start condition to the SDA and SCL lines (after the current ACK is sent) and then will send out the calling address which is stored in IICA1, or IICA2, as selected by the MAS control bit. The bit will be cleared automatically as soon as the address byte is transmitted.

IICBR[2:0]: Baud rate selection (master mode only). Fosc is the frequency of the external crystal, or oscillator. This value defaults to Fosc/512.

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IICBR[2:0]	Baud Rate
000	Fosc/32
001	Fosc/64
010	Fosc/128
011	Fosc/256
100	Fosc/512
101	Fosc/1024
110	Fosc/2048
111	Fosc/4096

Mnemonic: IICS Address: F8h

7	6	5	4	3	2	1	0	Reset
MStart	RxIF	TxIF	RDR	TDR	RxAK	TxAK	RW	00h

MStart: Master Start control bit. (Master mode only)
When the MStart bit is set, the module will generate a start condition on the SDA and SCL lines and will send out the calling address which is stored in IICA1, or IICA2, as selected by the MAS control bit. When the MStart bit is cleared, the module will generate a stop condition on the SDA and SCL lines.

RxIF: The data Receive Interrupt Flag (RXIF) is set after the IICRWD (IIC Read Write Data Buffer) is loaded with a newly received data byte.

TxIF: The data Transmit Interrupt Flag (TXIF) is set when the data of the IICRWD (IIC Read Write Data Buffer) is loaded on the output shift register.

RDR: The MCU must clear this bit after reading the data from the IICRWD. The IIC module is able to write new data into the IICRWD only when this bit is cleared.

TDR: After writing data to the IICRWD, the MCU must set this bit to '1' for the IIC module to transmit the data written in the IICRWD. The bit is cleared automatically after the byte in IICRWD, is transmitted.

RxAK: Acknowledge Received indicator bit. This bit is cleared after receiving an ACK following the transmission of 8 data bits on the bus.

TxAK: Acknowledge status transmit bit. After receiving 8 data bits, a NACK will be transmitted to the master if this bit is set, while an ACK will be transmitted to the master if this bit is cleared. It is the 9th bit in a one byte transmission as shown in Fig. 14-1. This bit must be written first, before the beginning of the reception of the byte.

RW: While in slave mode, the device will read (receive) data from the bus if this bit is cleared. When set, the device will write (transmit) data to the bus.

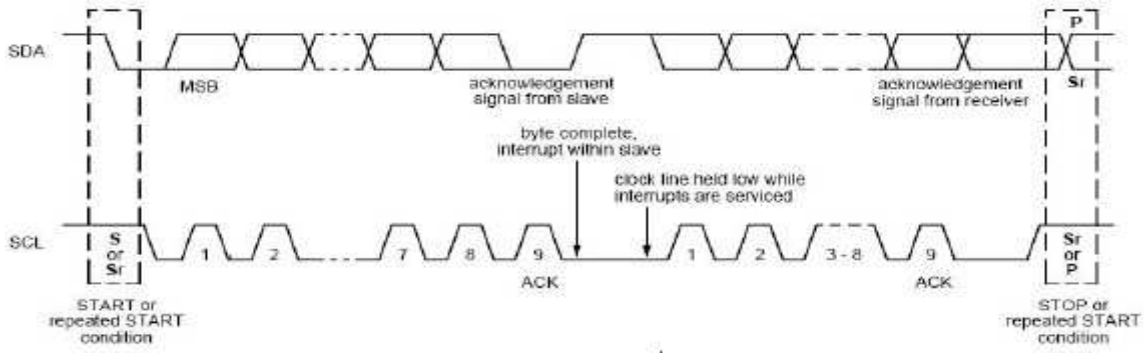

Fig. 14-1: Acknowledgement bit in the 9th bit of a byte transmission

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Mnemonic: IICA1 Address: FAh

7	6	5	4	3	2	1	0	Reset
IICA1[7:1]							Match1 or RW1	A0H
R/W							R or R/W	

Slave mode:

IICA1[7:1]: IIC Address registers

These bits set the 7-bit address of the slave module. When an address byte is received from the master, it will be compared to these bits. If there is a match, bit Match1 (IICA1.0) will be set. When the IIC bus is stopped, bit Match1 will be cleared automatically.

Master mode:

IICA1[7:1]: IIC Address registers

These bits set the 7-bit address of the slave device to be addressed.

RW1: This bit will be sent out to the slave device as the RW bit, when either bit Mstart, or bit Rstart, is set. It is sent as the 8th bit of the IIC address byte, as shown in Fig. 14-2, and is used to indicate to the slave device the direction of the communication. If set to 1, the module is in master receive mode. If cleared to 0, the module is in master transmit mode.

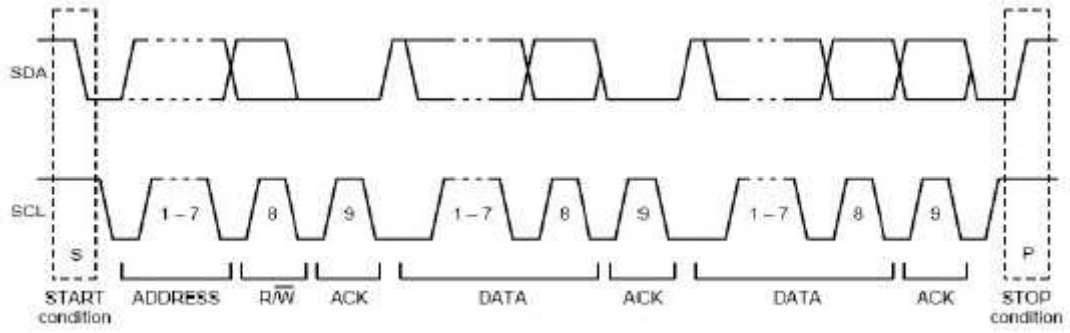

Fig. 14-2: RW bit in the 8th bit of the IIC address byte

Mnemonic: IICA2 Address: FBh

7	6	5	4	3	2	1	0	Reset
IICA2[7:1]							Match2 or RW2	60H
R/W							R or R/W	

Slave mode:

IICA2[7:1]: IIC Address registers

These bits set the second 7-bit address of the slave module. When an address byte is received from the master, it will be compared to these bits. If there is a match, bit Match2 (IICA2.0) will be set. When the IIC bus is stopped, bit Match2 will be cleared automatically.

Master mode:

IICA2[7:1]: IIC Address registers

These bits set the 7-bit address of the slave device to be addressed.

RW2: This bit will be sent out to the slave device as the RW bit, when either bit Mstart, or bit Rstart, is set. It is used to indicate to the slave device the direction of the communication. If set to 1, the module is in master receive mode. If cleared to 0, the module is in master transmit mode.

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Mnemonic: IICRW Address: FCh

7	6	5	4	3	2	1	0	Reset
IICRW[7:0]								00H

IICRWD[7:0]: IIC read/write data buffer.
When receiving, the received byte is stored here. When transmitting, the byte to be sent is written here.

Mnemonic: IICS2 Address: FDh

7	6	5	4	3	2	1	0	Reset
–	–	–	–	AB_EN	BF_EN	AB_F	BF	00H

AB_EN: Arbitration lost enable bit. (Master mode only)
If bit AB_EN is set, the hardware will check whether bus arbitration is lost. If bus arbitration is lost, the mcu will return to IDLE state. If bit AB_EN is cleared, hardware will not check whether bus arbitration is lost. It is advised to set this bit in a multi-master and slave bus. Clear this bit in a single master bus.

BF_EN: Bus busy enable bit. (Master mode only)
If bit BF_EN is set, hardware will not generate a start condition to the bus until BF=0. If this bit is cleared, the mcu will always generate a start condition when MStart is set. Set this bit in a multi-master and slave bus. Clear this bit in a single master bus.

AB_F: Arbitration lost bit. (Master mode only)
In a multi-master bus, an arbitration lost condition occurs, when a data bit “1” is sent but a “0” is returned. This bit is set in such condition. The application software needs to clear this bit and then check until BF=0 before sending data again.

BF: Bus busy bit. (Master mode only)
This bit is set if one of the following is detected: scl=0, sda=0, bus start. It is cleared if a bus stop is detected, or a quiet period of about 4.7μsec elapses. This bit can be cleared by software to return to the ready state.

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15 SPI function

Serial Peripheral Interface (SPI) is a synchronous serial protocol that allows a master device to initiate communication with slave devices.

The interrupt vector for this module is 4Bh. There is only one SPI interface channel.

There are 4 signals used in SPI:
SPI_MOSI: data output in the master mode, data input in the slave mode,
SPI_MISO: data input in the master mode, data output in the slave mode,
SPI_SCK: clock output form the master, the above data are synchronous to this signal,
SPI_SS: slave select input in the slave mode. In master mode, it is used to select a device when cleared to 0. The slave device is selected when it detects a 0 in this pin.
Fig. 15-1 demonstrates the relation of the 4 signals between master and slave devices.

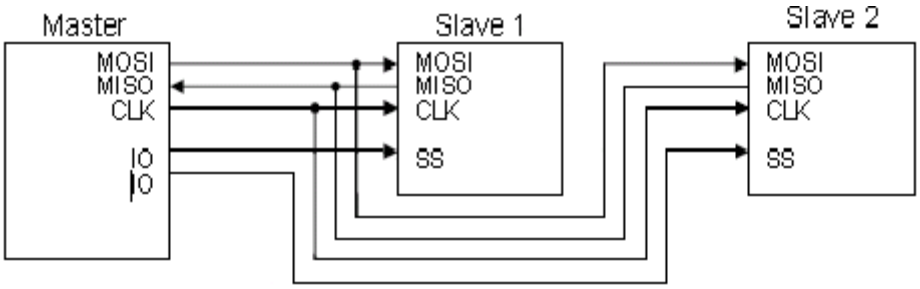

Fig. 15-1: SPI signals between master and slave devices

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
SPI Function										
AUX	Auxiliary register	91h	BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS
SPIC1	SPI control register 1	F1h	SPIEN	SPI MSS	SPI SSP	SPI CKP	SPI CKE	SPIBR[2:0]		
SPIC2	SPI Control register 2	F2h	SPIFD	TBC[2:0]			--	RBC[2:0]		
SPIS	SPI status register	F5h	--	SPI MLS	SPIOV	SPI TXIF	SPI TDR	SPI RXIF	SPI RDR	SPIRS
SPITXD	SPI transmit data buffer	F3h	SPITXD[7:0]							
SPIRXD	SPI receive data buffer	F4h	SPIRXD[7:0]							

Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

P4SPI: P4SPI = 0 – SPI function on P1.
P4SPI = 1 – SPI function on P4.

Mnemonic: SPIC1 Address: F1h

7	6	5	4	3	2	1	0	Reset
SPIEN	SPIMSS	SPISSP	SPICKP	SPICKE	SPIBR[2:0]			08H

SPIEN: Enable SPI module. “1” is Enable. “0” is Disable.

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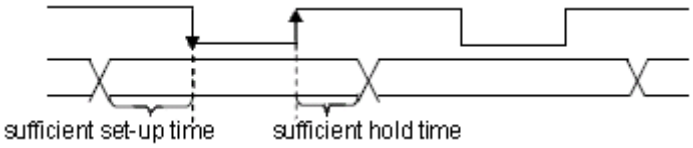
SPIMSS: Master or Slave mode Select
"1" = Master mode.
"0" = Slave mode.
SPISSP: Slave Select (SS) active polarity (used in slave mode only)
"1" -> active high.
"0" -> active low.
SPICKP: Clock idle polarity (used in master mode only)
"1" – SCK high during idle. Ex :

"0" - SCK low during idle. Ex :

SPICKE: Clock sample edge select.
"1" -> data latch in rising edge
"0" -> data latch in falling edge.

* To ensure data latch stability, the mcu generates the output data as illustrated in the following example, the other side can latch the stable data either in rising or falling edge.



SPIBR[2:0]: SPI baud rate select (master mode only), Fosc is the external crystal or oscillator frequency :

SPIBR[2:0]	Baud Rate
000	Fosc/4
001	Fosc/8
010	Fosc/16
011	Fosc/32
100	Fosc/64
101	Fosc/128
110	Fosc/256
111	Fosc/512

Mnemonic: SPIC2 Address: F2h

7	6	5	4	3	2	1	0	Reset
SPIFD	TBC[2:0]			--	RBC[2:0]			08H

SPIFD: Full-duplex mode enable.
"1" : enable full-duplex mode.
"0" : disable full-duplex mode.

When set, only 8-bit communication is allowed and both TBC[2:0] and RBC[2:0] will be cleared and kept to zero. When the master device transmits data to the slave device via the MOSI line, the slave device responds by sending data back to the master device via the MISO line. This implies that full-duplex transmission with both out-data and in-data are synchronized with the same clock SCK as shown below.

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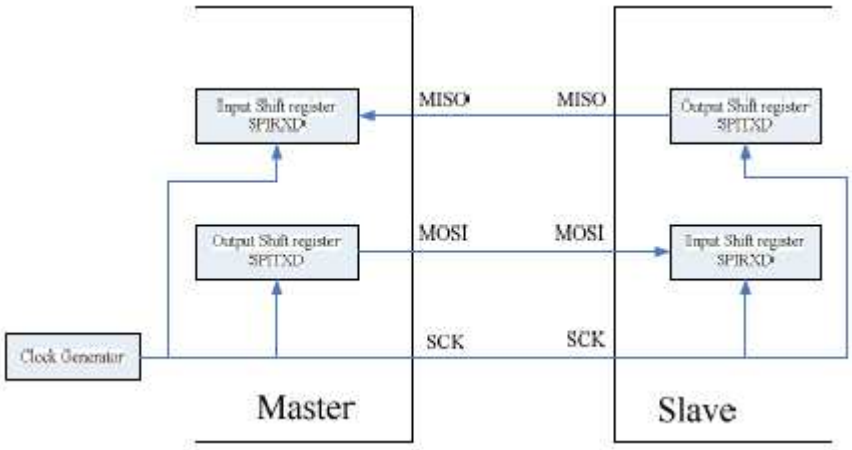

TBC[2:0]: SPI transmitter bit counter, here 1-8 bits are allowed except for the full-duplex mode

TBC[2:0]	Bit Counter
000	8 bits output
001	1 bit output
010	2 bits output
011	3 bits output
100	4 bits output
101	5 bits output
110	6 bits output
111	7 bits output

RBC[2:0]: SPI receiver bit counter, here 1-8 bits are allowed except for the full-duplex mode

RBC[2:0]	Bit Counter
000	8 bits output
001	1 bit output
010	2 bits output
011	3 bits output
100	4 bits output
101	5 bits output
110	6 bits output
111	7 bits output

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Mnemonic: SPIS Address: F5h

7	6	5	4	3	2	1	0	Reset
--	SPIMLS	SPIOV	SPITXIF	SPITDR	SPIRXIF	SPIRDR	SPIRS	40h

SPIMLS: MSB or LSB output /input first
"1" : MSB output/input first
"0" : LSB output/input first
SPIOV: Overflow flag.
SPIOV is set when there is data available in SPIRXD (SPIRDR is set), but has not been read, and the next data is also received (there is no preventing mechanism against such situation). SPIRXD is damaged by this overflow. The flag will be cleared by hardware when SPIRDR is cleared.
SPITXIF: Transmit Interrupt Flag.
SPITXIF is set when the data held in the SPITXD register is moved to the output shift register.
SPITDR: Transmit Data Ready.
When a byte is loaded onto the SPITXD register, the application software must set this flag for the SPI module to transmit the byte. The flag is cleared automatically when the data byte is moved to the output shift register.
SPIRXIF: Receive Interrupt Flag.
SPIRXIF is set after the SPIRXD register is loaded with a newly received byte.
SPIRDR: Receive Data Ready.
SPIRDR is set when a byte is received. The MCU must clear this bit after it reads the data from the SPIRXD register. If the SPI module on the transmit side writes new data into the SPIRXD before this bit is cleared, then the data will be overwritten.
SPIRS: Receive Start.
This bit is set to enable data reception into the SPIRXD register.

Mnemonic: SPITXD Address: F3h

7	6	5	4	3	2	1	0	Reset
SPITXD[7:0]								00h

SPITXD[7:0]: Transmit data buffer.

Mnemonic: SPIRXD Address: F4h

7	6	5	4	3	2	1	0	Reset
SPIRXD[7:0]								00h

SPIRXD[7:0]: Receive data buffer.

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16 KBI – Keyboard Interface

The keyboard interface (KBI) can be connected to an 8 x n matrix keyboard, or any similar device. It has 8 inputs with programmable interrupt capability on either high, or low, level. These 8 inputs are available on either P2, or P0. The related interrupt can be used to exit from the idle and stop modes. The 8 inputs are independent from each other but share the same interrupt vector at 5Bh.

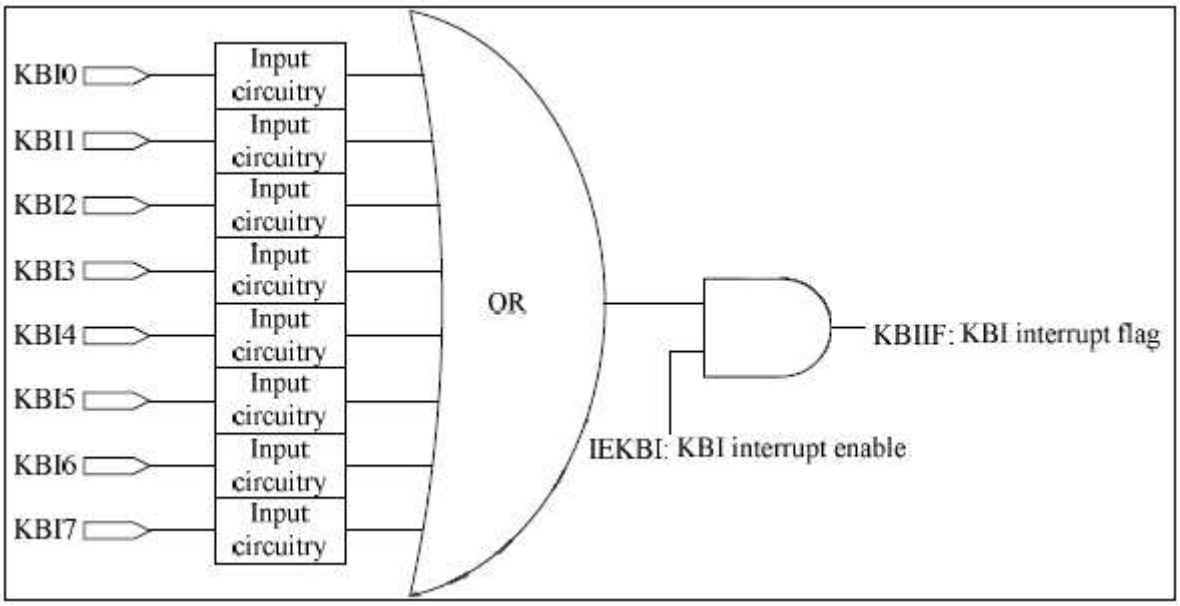

Figure 16.1 keyboard interface block diagram

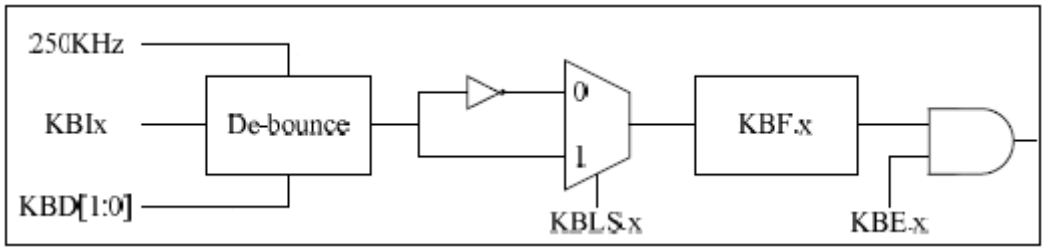

Figure 16.2 keyboard input circuitry

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
KBI function										
AUX	Auxiliary register	91h	BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS
KBLS	KBI level selection	93h	KBLS7	KBLS6	KBLS5	KBLS4	KBLS3	KBLS2	KBLS 1	KBLS0
KBE	KBI input enable	94h	KBE7	KBE6	KBE5	KBE4	KBE3	KBE2	KBE1	KBE0
KBF	KBI flag	95h	KBF7	KBF6	KBF5	KBF4	KBF3	KBF2	KBF1	KBF0
KBD	KBI De-bounce control register	96h	KBDEN	--	--	--	--	--	KBD1	KBD0

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Mnemonic: AUX Address: 91h

7	6	5	4	3	2	1	0	Reset
BRS	P4CC	P4SPI	--	P4IIC	P0KBI	--	DPS	00H

P0KBI: P0KBI = 0 – KBI function on P2.
P0KBI = 1 – KBI function on P0.

Mnemonic: KBLS Address: 93h

7	6	5	4	3	2	1	0	Reset
KBLS.7	KBLS.6	KBLS.5	KBLS.4	KBLS.3	KBLS.2	KBLS.1	KBLS.0	00H

KBLS.7: Keyboard Line 7 level selection bit
0 : enable a low level detection on KBI7.
1 : enable a high level detection on KBI7.
KBLS.6: Keyboard Line 6 level selection bit
0 : enable a low level detection on KBI6.
1 : enable a high level detection on KBI6.
KBLS.5: Keyboard Line 5 level selection bit
0 : enable a low level detection on KBI5.
1 : enable a high level detection on KBI5.
KBLS.4: Keyboard Line 4 level selection bit
0 : enable a low level detection on KBI4.
1 : enable a high level detection on KBI4.
KBLS.3: Keyboard Line 3 level selection bit
0 : enable a low level detection on KBI3.
1 : enable a high level detection on KBI3.
KBLS.2: Keyboard Line 2 level selection bit
0 : enable a low level detection on KBI2.
1 : enable a high level detection on KBI2.
KBLS.1: Keyboard Line 1 level selection bit
0 : enable a low level detection on KBI1.
1 : enable a high level detection on KBI1.
KBLS.0: Keyboard Line 0 level selection bit
0 : enable a low level detection on KBI0.
1 : enable a high level detection on KBI0.

Mnemonic: KBE Address: 94h

7	6	5	4	3	2	1	0	Reset
KBE.7	KBE.6	KBE.5	KBE.4	KBE.3	KBE.2	KBE.1	KBE.0	00H

KBE.7: Keyboard Line 7 enable bit
0 : enable standard I/O pin.
1 : enable KBF.7 bit in KBF register to generate an interrupt request.
KBE.6: Keyboard Line 6 enable bit
0 : enable standard I/O pin.
1 : enable KBF.6 bit in KBF register to generate an interrupt request.
KBE.5: Keyboard Line 5 enable bit
0 : enable standard I/O pin.
1 : enable KBF.5 bit in KBF register to generate an interrupt request.
KBE.4: Keyboard Line 4 enable bit
0 : enable standard I/O pin.
1 : enable KBF.4 bit in KBF register to generate an interrupt request.

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KBE.3: Keyboard Line 3 enable bit
0 : enable standard I/O pin.
1 : enable KBF.3 bit in KBF register to generate an interrupt request.
KBE.2: Keyboard Line 2 enable bit
0 : enable standard I/O pin.
1 : enable KBF.2 bit in KBF register to generate an interrupt request.
KBE.1: Keyboard Line 1 enable bit
0 : enable standard I/O pin.
1 : enable KBF.1 bit in KBF register to generate an interrupt request.
KBE.0: Keyboard Line 0 enable bit
0 : enable standard I/O pin.
1 : enable KBF.0 bit in KBF register to generate an interrupt request.

Mnemonic: KBF Address: 95h

7	6	5	4	3	2	1	0	Reset
KBF.7	KBF.6	KBF.5	KBF.4	KBF.3	KBF.2	KBF.1	KBF.0	00H

KBF.7: Keyboard Line 7 flag
This is set by hardware when KBI7 detects a programmed level. It generates a Keyboard interrupt request if KBE.7 is also set. It must be cleared by software.
KBF.6: Keyboard Line 6 flag
This is set by hardware when KBI6 detects a programmed level. It generates a Keyboard interrupt request if KBE.6 is also set. It must be cleared by software.
KBF.5: Keyboard Line 5 flag
This is set by hardware when KBI5 detects a programmed level. It generates a Keyboard interrupt request if KBE.5 is also set. It must be cleared by software.
KBF.4: Keyboard Line 4 flag
This is set by hardware when KBI4 detects a programmed level. It generates a Keyboard interrupt request if KBE.4 is also set. It must be cleared by software.
KBF.3: Keyboard Line 3 flag
This is set by hardware when KBI3 detects a programmed level. It generates a Keyboard interrupt request if KBE.3 is also set. It must be cleared by software.
KBF.2: Keyboard Line 2 flag
This is set by hardware when KBI2 detects a programmed level. It generates a Keyboard interrupt request if KBE.2 is also set. It must be cleared by software.
KBF.1: Keyboard Line 1 flag
This is set by hardware when KBI1 detects a programmed level. It generates a Keyboard interrupt request if KBE.1 is also set. It must be cleared by software.
KBF.0: Keyboard Line 0 flag
This is set by hardware when KBI0 detects a programmed level. It generates a Keyboard interrupt request if KBE.0 is also set. It must be cleared by software.

Mnemonic: KBD Address: 96h

7	6	5	4	3	2	1	0	Reset
KBDEN	--	--	--	--	--	KBD.1	KBD.0	00H

KBDEN: Enable KBI de-bounce function. The default KBI function is enabled.
KBDEN = 0, enable KBI de-bounce function. The de-bounce time is selected by KBD [1:0].
KBDEN = 1, disable KBI de-bounce function. The KBI input pin without de-bounce mechanism.
KBD[1:0]: Select KBI de-bounce time.
KBD[1:0] = 00, the de-bounce time is 320 ms (default).
KBD[1:0] = 01, the de-bounce time is 160 ms.
KBD[1:0] = 10, the de-bounce time is 80 ms.
KBD[1:0] = 11, the de-bounce time is 40 ms.

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17 LVI – Low Voltage Interrupt

The interrupt vector for this function is 63h.

Mnemonic: LVC Address: E6h

7	6	5	4	3	2	1	0	Reset
LVI_EN	--	LVRXE	--	--	--	--	--	00H

LVI_EN: Low voltage interrupt function enable bit.
LVI_EN = 0 : disable low voltage detect function.
LVI_EN = 1 : enable low voltage detect function.

LVRXE: External low voltage reset function enable bit.
LVRXE = 0 : disable external low voltage reset function.
LVRXE = 1 : enable external low voltage reset function.

Low Voltage Detect Level		
	LVI	LVRX
CRD89C51AB1TB	3.5V	3.1V
CRD89L51AB1TB	2.3V	2.1V

Note: The device is guaranteed to operate normally within the operating voltage described in the DC operating conditions section. In practice, the device is capable of operating under a VDD supply down to the LVR voltage and then a low voltage reset is triggered. Normal operation is not tested for VDD supplies below the valid operating voltage of the device.

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18 10-bit Analog-to-Digital Converter (ADC)

The mcu provides an eight channel 10-bit ADC. The result of the conversion is provided at ADCD [9:0]. The ADC interrupt vector is 53h.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ADC										
ADCC1	ADC Control register 1	ABh	ADC7 EN	ADC6 EN	ADC5 EN	ADC4 EN	ADC3 EN	ADC2 EN	ADC1 EN	ADC0 EN
ADCC2	ADC Control register 2	ACh	Start	ADJUST	--	--	--	ADCCH[2:0]		
ADCDH	ADC data high byte	ADh	ADCDH [7:0]							
ADCDL	ADC data low byte	AEh	ADCDL [7:0]							
ADCCS	ADC clock select	AFh	--	--	--	ADCCS[4:0]				

Mnemonic: ADCC1 Address: ABh

7	6	5	4	3	2	1	0	Reset
ADC7EN	ADC6EN	ADC5EN	ADC4EN	ADC3EN	ADC2EN	ADC1EN	ADC0EN	00H

ADC7EN: ADC channels 7 enable.
ADC7EN = 1 – Enable ADC channel 7
ADC6EN: ADC channels 6 enable.
ADC6EN = 1 – Enable ADC channel 6
ADC5EN: ADC channels 5 enable.
ADC5EN = 1 – Enable ADC channel 5
ADC4EN: ADC channels 4 enable.
ADC4EN = 1 – Enable ADC channel 4
ADC3EN: ADC channels 3 enable.
ADC3EN = 1 – Enable ADC channel 3
ADC2EN: ADC channels 2 enable.
ADC2EN = 1 – Enable ADC channel 2
ADC1EN: ADC channels 1 enable.
ADC1EN = 1 – Enable ADC channel 1
ADC0EN: ADC channels 0 enable.
ADC0EN = 1 – Enable ADC channel 0

Mnemonic: ADCC2 Address: ACh

7	6	5	4	3	2	1	0	Reset
START	ADJUST	–	–	–	ADCCH[2:0]			00H

Start: When this bit is set, the ADC will start a conversion.

ADJUST: Adjust the format of ADC conversion DATA.
ADJUST = 0: (default value)
ADC data high byte ADCD [9:2] = ADCDH [7:0].
ADC data low byte ADCD [1:0] = ADCDL [1:0].
ADJUST = 1:
ADC data high byte ADCD [9:8] = ADCDH [1:0].
ADC data low byte ADCD [7:0] = ADCDL [7:0].

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ADCCH[2:0]: ADC channel select.

ADCCH [2:0]	Channel
000	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

ADJUST = 0:

Mnemonic: ADCDH — Address: ADh

7	6	5	4	3	2	1	0	Reset
ADCD[9]	ADCD[8]	ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	00H

Mnemonic: ADCDL — Address: AEh

7	6	5	4	3	2	1	0	Reset
--	--	--	--	--	--	ADCD[1]	ADCD[0]	00H

ADJUST = 1:

Mnemonic: ADCDH — Address: ADh

7	6	5	4	3	2	1	0	Reset
--	--	--	--	--	--	ADCD[9]	ADCD[8]	00H

Mnemonic: ADCDL — Address: AEh

7	6	5	4	3	2	1	0	Reset
ADCD[7]	ADCD[6]	ADCD[5]	ADCD[4]	ADCD[3]	ADCD[2]	ADCD[1]	ADCD[0]	00H

Mnemonic: ADCCS — Address: AFh

7	6	5	4	3	2	1	0	Reset
–	–	--	ADCCS[4]	ADCCS[3]	ADCCS[2]	ADCCS[1]	ADCCS[0]	00H

ADCCS[4:0]: ADC clock select.

NOTE: maximum ADC clock is 12.5MHz.
NOTE: maximum ADC Conversion rate is 500KHz.

$$ADC\_Clock = \frac{Fclk}{2x(ADCCS+1)}$$

$$ADC\_Conversion\_Rate = \frac{ADC\_Clock}{23}$$

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ADCCS[4:0]	ADC Clock(Hz)	Clocks for ADC Conversion
00000	Fclk/2	46
00001	Fclk/4	92
00010	Fclk/6	138
00011	Fclk/8	184
00100	Fclk/10	230
00101	Fclk/12	276
00110	Fclk/14	322
00111	Fclk/16	368
01000	Fclk/18	414
01001	Fclk/20	460
01010	Fclk/22	506
01011	Fclk/24	552
01100	Fclk/26	598
01101	Fclk/28	644
01110	Fclk/30	690
01111	Fclk/32	736
10000	Fclk/34	782
10001	Fclk/36	828
10010	Fclk/38	874
10011	Fclk/40	920
10100	Fclk/42	966
10101	Fclk/44	1012
10110	Fclk/46	1058
10111	Fclk/48	1104
11000	Fclk/50	1150
11001	Fclk/52	1196
11010	Fclk/54	1242
11011	Fclk/56	1288
11100	Fclk/58	1334
11101	Fclk/60	1380
11110	Fclk/62	1426
11111	Fclk/64	1472

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19 In-System Programming (Internal ISP)

A user may update the application software found in the mcu if an ISP service code is preloaded in the ISP code area as shown in Table 19-1. One page of Flash memory is 256 bytes. The mcu provides the necessary internal flash control signals required for flash program/chip erase/page erase/protect functions.

19.1 ISP service program

The ISP service program resides in the ISP service program area. It is loaded onto the mcu via an external writer. It communicates with the host by using a communication protocol that ensures the integrity of the data to be programmed and then performs the related flash memory programming functions. It can be initiated when the mcu is either active, or idle. It cannot be initiated while in power-down mode.

19.2 Lock Bit (N)

The Lock Bit N has two functions:

- configure the size of the service program area
- lock the ISP service program area and protect it during the flash erase function.

The ISP service program area is located in region $3000 to $3FFF. It is divided in blocks of N*256 bytes. (N=0 to 16). When N=1 the ISP service program occupies 256 bytes, while when N=16 the ISP service program occupies 4K bytes. This is the maximum ISP service program allowed. When N=0 there is no ISP function and all flash memory can be used as program memory. When N <> 0, any flash memory not used for ISP service program, may be used for the user application and data. The ISP service program area is reserved from address $3FFF downwards. As shown in Table 19-1, its start address is located at $3x00 where x is an even number, depending on the lock bit N.

The lock bit N function is different from the flash protect function. The flash erase function erases all of the flash memory apart from the locked ISP service program area. If the flash is not protected, the content of ISP service program can be read. If the flash is protected, the overall content of the flash program memory, including the ISP service program area can not be read.

N	ISP service program address
0	No ISP service program
1	256 bytes ($3F00h ~ $3FFFh)
2	512 bytes ($3E00h ~ $3FFFh)
3	768 bytes ($3D00h ~ $3FFFh)
4	1.0 K bytes ($3C00h ~ $3FFFh)
5	1.25 K bytes ($3B00h ~ $3FFFh)
6	1.5 K bytes ($3A00h ~ $3FFFh)
7	1.75 K bytes ($3900h ~ $3FFFh)
8	2.0 K bytes ($3800h ~ $3FFFh)
9	2.25 K bytes ($3700h ~ $3FFFh)
10	2.5 K bytes ($3600h ~ $3FFFh)
11	2.75 K bytes ($3500h ~ $3FFFh)
12	3.0 K bytes ($3400h ~ $3FFFh)
13	3.25 K bytes ($3300h ~ $3FFFh)
14	3.5 K bytes ($3200h ~ $3FFFh)
15	3.75 K bytes ($3100h ~ $3FFFh)
16	4.0 K bytes ($3000h ~ $3FFFh)

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19.3 Programming the ISP Service Program

After the ISP service program is programmed and the Lock Bit N is set, the ISP service program area will be protected (locked) automatically. The lock bit N has its own program/erase timing, separate from the flash memory program/erase timing. The locked ISP service program can not be erased by the flash erase function. The ISP service program can only be updated via an external writer. It cannot be updated in system.

19.4 Initiating the ISP Service Program

There are a number of ways to invoke the code located at the ISP code area. These are:

(1) Blank reset. If the mcu is reset and the first flash address is blank ($0000=0xFF), then the PC will be loaded with the start address of the ISP service program. The hardware reset includes both the internal (power on reset) and external pad reset.
(2) The application program executes a long jump instruction to the ISP service program entry point.
(3) The ISP service program is invoked by setting P2.6, P2.7 low, or P4.3 low, during hardware reset. The hardware reset includes both internal (power on reset) and external pad reset. When designing the application circuit, the designer must take care of the handling of P2.6, P2.7 or P4.3 during the reset period to prevent the mcu from entering the ISP service program.
(4) The ISP service program is invoked if, while the RESET line is active, two negative edge pulses are applied on P3.0. The hardware reset includes both the internal (power on reset) and external pad reset.

During the reset period, the hardware will detect the status of P2.6/P2.7/P4.3/P3.0. If they meet one of above conditions, the ISP service program will be invoked. After completion of the ISP service, the mcu must be reset, either by hardware reset, or by WDT reset, or a long jump to address $0000.

The ISP entry method will be selected during mcu reprogramming either by the external writer, or the ISP.

Name	Description	Addr	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
ISP Function										
TAKEY	Time Access Key register	F7h	TAKEY [7:0]							
IFCON	Interface Control register	8Fh	ITS	CDPR	--	--	ALEC[1:0]		EMEN	ISPE
ISPFAH	ISP Flash Address - High register	E1h	ISPFAH [7:0]							
ISPFAL	ISP Flash Address - Low register	E2h	ISPFAL [7:0]							
ISPFD	ISP Flash Data register	E3h	ISPFD [7:0]							
ISPFC	ISP Flash Control register	E4h	EMF1	EMF2	EMF3	EMF4	--	ISPF.2	ISPF.1	ISPF.0

Mnemonic: TAKEY Address: F7h

7	6	5	4	3	2	1	0	Reset
TAKEY [7:0]								00H

By default, ISP enable bit (ISPE, IFCON.0) is read-only. It can be set only after the application writes to TAKEY three specific values 55h, AAh and 5Ah in this sequence. For example:

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah
```


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Mnemonic: IFCON Address: 8Fh

7	6	5	4	3	2	1	0	Reset
ITS	CDPR	--	--	ALEC[1:0]		EMEN	ISPE	00H

For the ISP function to be enabled, ISPE (IFCON.0) must be set to 1. When cleared to 0, the ISP function is disabled. It acts as security against accidental use of the ISP function which might lead to unintentional program erasure. After setting the ISPE bit, the user is granted write access to the ISP registers ISPFAH, ISPFAL, ISPFD and ISPFC, which are otherwise read-only.

Mnemonic: ISPFAH Address: E1h

7	6	5	4	3	2	1	0	Reset
ISPFAH [7:0]								00H

Mnemonic: ISPFAL Address: E2h

7	6	5	4	3	2	1	0	Reset
ISPFAL [7:0]								00H

ISPFAH : ISP Function Flash address MSB, ISPFAL : ISP Function Flash address LSB. These two bytes provide the 16-bit flash memory address of the selected ISP function. This address must not lie within the memory area of the ISP service program. If it does, then the selected flash program/page erase function will be ignored.

Mnemonic: ISPFD Address: E3h

7	6	5	4	3	2	1	0	Reset
ISPFD [7:0]								00H

ISPFD: provides the 8 bit data required for the selected ISP function.

Mnemonic: ISPFC Address: E4h

7	6	5	4	3	2	1	0	Reset
EMF1	EMF2	EMF3	EMF4	--	ISPF[2]	ISPF[1]	ISPF[0]	00H

EMF1: Entry mechanism (1) flag, clear by reset. (Read only)
EMF2: Entry mechanism (2) flag, clear by reset. (Read only)
EMF3: Entry mechanism (3) flag, clear by reset. (Read only)
EMF4: Entry mechanism (4) flag, clear by reset. (Read only)
ISPF [2:0]: ISP function select bit.

ISPF [2:0]	ISP Function
000	Byte program
001	Chip protect
010	Page erase
011	Chip Erase
100	Write option
101	Read option
110	Erase option
111	--

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One page of flash memory consists of 256 bytes.

The Option function can access the settings of the Internal reset time (see section 1.4.1), clock source (see section 1.5), P4[4:7] pins function select (see section 5), WDTEN control bit (see section 10) and ISP entry mechanisms select (see in section 19).

If the chip is protected, or there is no ISP service program, then the Option settings can only be read.

In order to perform either the byte program, or the page erase, ISP function, the user must specify the flash address concerned. If the page erase function is selected, the mcu will erase the contents of the entire page within which the address indicated by ISPFAH & ISPFAL, lies. For example, if ISPFAH & ISPFAL is loaded with $XYMN, then all addresses from $XY00 to $XYFF, will be erased. If the chip erase ISP function is selected, then the mcu will erase all the flash program memory apart from the ISP service program area. If the chip protection is activated, then all memory contents will read back #00H.

Example: using the ISP service program to load address $1005h with byte #22h.

```
MOV TAKEY, #55h
MOV TAKEY, #AAh
MOV TAKEY, #5Ah     ; enable ISPE write
MOV IFCON, #01H     ; enable the ISP function
MOV ISPFAH, #10H    ; set flash address-high, 10H
MOV ISPFAL, #05H    ; set flash address-low, 05H
MOV ISPFD, #22H     ; set flash data to be programmed, data = 22H
MOV ISPFC, #00H     ; start loading #22H to flash address $1005H
```


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Operating Conditions

Symbol	Description	Min.	Typ.	Max.	Unit.	Remarks
TA	Operating temperature	-40	25	85	℃	Ambient temperature under bias
VDD33	Supply voltage	2.7	3.3	3.6	V	
VDD5	Supply voltage	4.5	5.0	5.5	V	

DC Characteristics

TA = -40℃ to 85℃, VCC = 5.0V

Symbol	Parameter	Valid	Min	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3,4,5	-0.5	0.8	V	Vcc=5V
VIL2	Input Low-voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High-voltage	Port 0,1,2,3,4,5	2.0	Vcc + 0.5	V	
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	Vcc + 0.5	V	
VOL	Output Low-voltage	Port 0,1,2,3,4,5		0.4	V	IOL=4.9mA Vcc=5V
VOH1	Output High-voltage using Strong Pullup(1)	Port 0,1,2,3,4,5	90% Vcc		V	IOH= -4.6mA
VOH2	Output High-voltage using Weak Pullup(2)	Port 0,1,2,3,4,5	2.4		V	IOH= -250μA
			75% Vcc		V	IOH= -162μA
			90% Vcc		V	IOH= -73μA
IIL	Logic 0 Input Current	Port 0,1,2,3,4,5		-75	μA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3,4,5		-650	μA	Vin= 2.0V
ILI	Input Leakage Current	Port 0,1,2,3,4,5		±10	μA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	300	kΩ	
CIO	Pin Capacitance			10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		12	mA	Active mode, 12MHz
				11	mA	Idle mode, 12MHz
				30	μA	Power down mode

Notes: 1. Port in Push-Pull Output Mode
2. Port in Quasi-Bidirectional Mode

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TA = -40℃ to 85℃, VCC = 3.3V

Symbol	Parameter	Valid	Min	Max	Units	Conditions
VIL1	Input Low-voltage	Port 0,1,2,3,4,5	-0.5	0.8	V	Vcc=3.3V
VIL2	Input Low-voltage	RES, XTAL1	0	0.8	V	
VIH1	Input High-voltage	Port 0,1,2,3,4,5	2.0	Vcc + 0.5	V	
VIH2	Input High-voltage	RES, XTAL1	70%Vcc	Vcc + 0.5	V	
VOL	Output Low-voltage	Port 0,1,2,3,4,5		0.4	V	IOL=3.2mA Vcc=3.3V
VOH1	Output High-voltage using Strong Pullup(1)	Port 0,1,2,3,4,5	90% Vcc		V	IOH= -2.3mA
VOH2	Output High-voltage using Weak Pullup(2)	Port 0,1,2,3,4,5	2.4		V	IOH= -77μA
			90% Vcc		V	IOH= -33μA
IIL	Logic 0 Input Current	Port 0,1,2,3,4,5		-75	μA	Vin= 0.45V
ITL	Logical Transition Current	Port 0,1,2,3,4,5		-650	μA	Vin= 1.5V
ILI	Input Leakage Current	Port 0,1,2,3,4,5		±10	μA	0.45V<Vin<Vcc
RRST	Reset Pull-down Resistor	RES	50	300	kΩ	
CIO	Pin Capacitance			10	pF	Freq= 1MHz, Ta= 25℃
ICC	Power Supply Current	VDD		11	mA	Active mode, 12MHz
				10	mA	Idle mode, 12MHz
				20	μA	Power down mode

Notes: 1. Port in Push-Pull Output Mode
2. Port in Quasi-Bidirectional Mode

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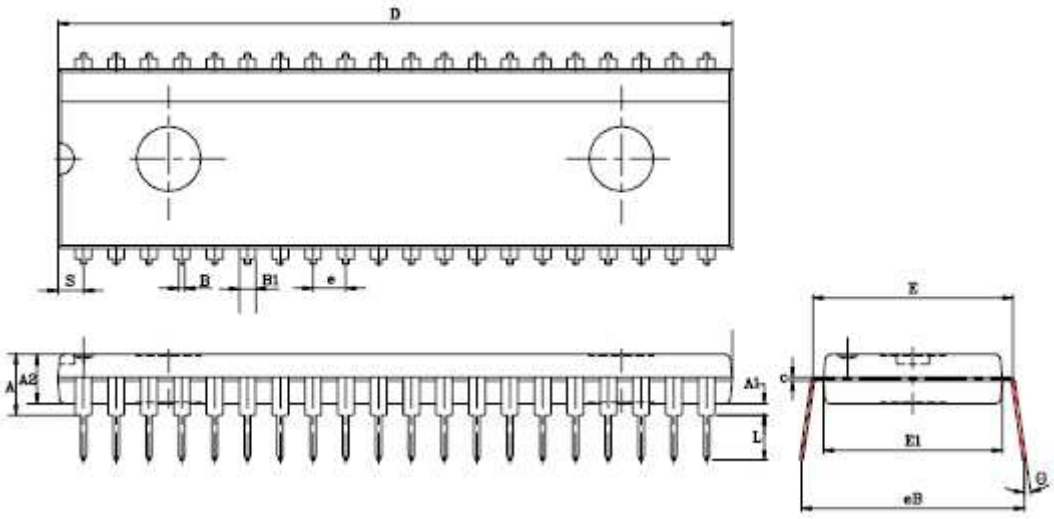
Package Information – PDIP 600 mil



Symbol	Dimension in mm			Dimension in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	—	—	5.59	—	—	0.220
A1	0.25	—	—	0.010	—	—
A2	3.18	—	4.95	0.125	—	0.195
B	0.36	—	0.58	0.014	—	0.023
B1	0.76	—	1.78	0.030	—	0.070
c	0.20	—	0.38	0.008	—	0.015
D	50.29	—	53.21	1.980	—	2.095
E	14.99	—	15.88	0.590	—	0.625
E1	12.32	—	14.73	0.485	—	0.580
e	—	2.54	—	—	0.100	—
eB	15.24	—	17.78	0.600	—	0.700
L	2.921	—	5.08	0.115	—	0.200
S	—	—	2.43	—	—	0.096
θ	0°	—	15°	0°	—	15°

Note:

1. Dimension D & E1 do not include mold protrusion. D and E1 are maximum plastic body size dimension including mold mismatch.

2. Dimension B1 does not include dambar protrusion.

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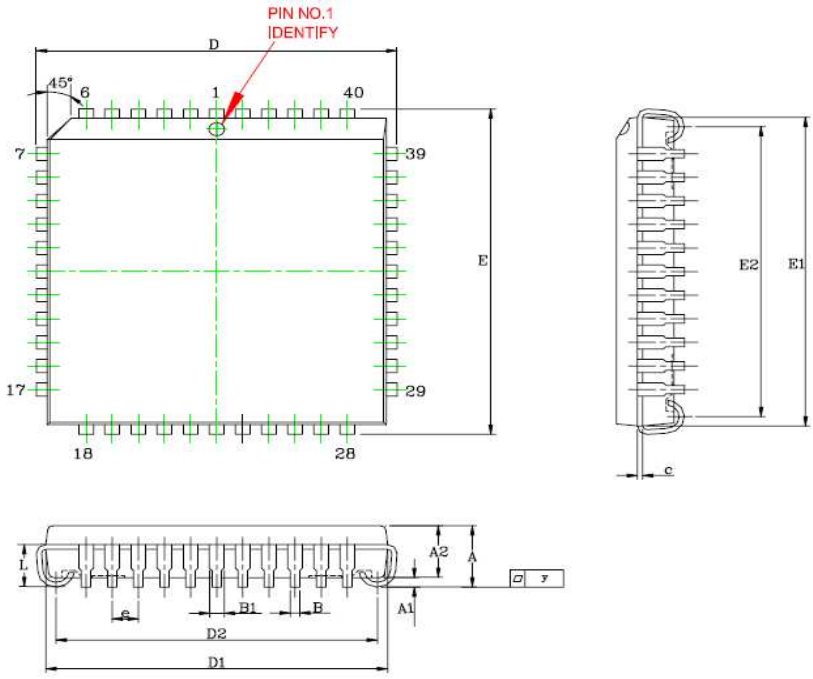
Package Information – PLCC



Symbol	Dimension in mm			Dimension in inch		
	Min.	Nom.	Max.	Min.	Nom.	Max.
A	4.19	–	4.70	0.165	–	0.185
A1	0.51	–	0.65	0.020	–	0.026
A2	3.68	—	4.01	0.145	—	0.158
B	0.33	—	0.56	0.013	—	0.022
B1	0.66	—	0.81	0.026	—	0.032
c	0.18	—	0.33	0.007	—	0.013
D	17.27	—	17.78	0.680	—	0.700
D1	16.46	—	16.71	0.648	—	0.658
D2	14.99	—	16.00	0.590	—	0.630
E	17.27	—	17.78	0.680	—	0.700
E1	16.46	—	16.71	0.648	—	0.658
E2	14.99	—	16.00	0.590	—	0.630
e	–	1.27	–	—	0.050	—
L	2.29	—	3.05	0.090	—	0.120
y	–	—	0.10		—	0.004

Note:

1. Dimension D & E1 do not include mold protrusion. D and E1 are maximum plastic body size dimension including mold mismatch.

2. Dimension B1 does not include dambar protrusion.

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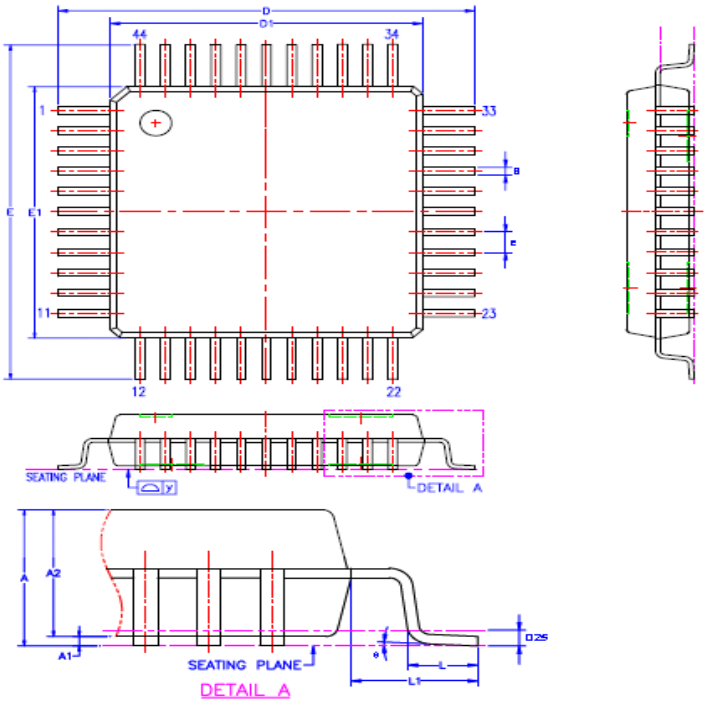

Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	2.70	—	—	0.106
A1	0.05	—	0.50	0.002	—	0.020
A2	1.90	—	2.20	0.075	—	0.087
B	0.29	—	0.45	0.011	—	0.018
c	0.10	—	0.23	0.004	—	0.009
D	13.00	—	13.40	0.512	—	0.528
D1	9.90	—	10.10	0.390	—	0.398
E	13.00	—	13.40	0.512	—	0.528
E1	9.90	—	10.10	0.390	—	0.398
e	—	0.80	—	—	0.031	—
L	0.73	—	1.03	0.029	—	0.041
L1	—	1.60	—	—	0.063	—
y	—	0.10	—	—	0.004	—
θ	0°	—	7°	0°	—	7°

Note:
1. Dimension D & E1 do not include mold protrusion. D and E1 are maximum plastic body size dimension including mold mismatch.
2. Dimension B1 does not include dambar protrusion.

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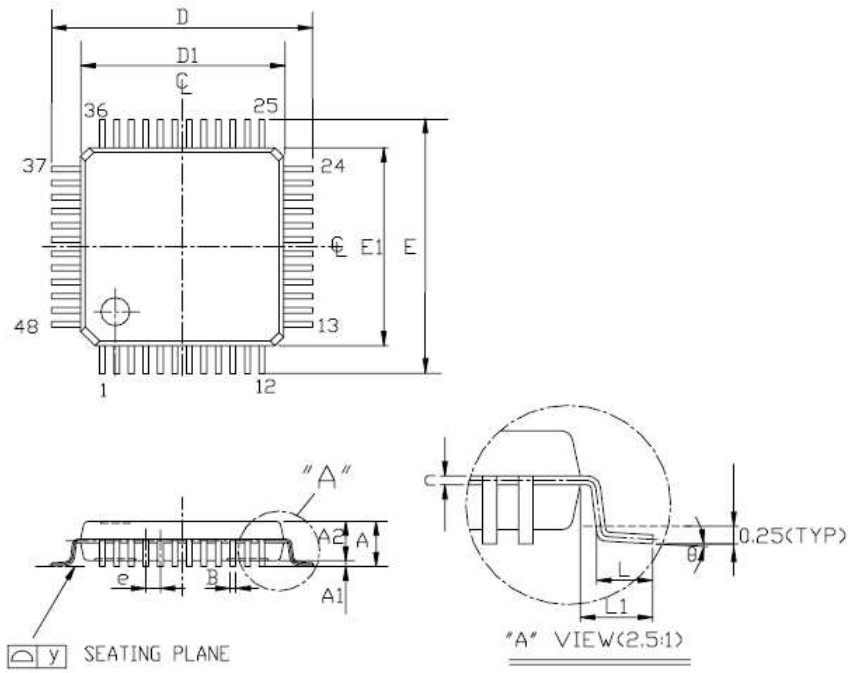
Package Information – 48 pin LQFP



Symbol	Dimension in mm			Dimension in inch		
	Min	Nom	Max	Min	Nom	Max
A	—	—	1.60	—	—	0.063
A1	0.05	—	0.15	0.002	—	0.006
A2	1.35	—	4.15	0.053	—	0.163
B	0.17	—	0.27	0.007	—	0.011
c	0.09	—	0.20	0.004	—	0.008
D	—	9.00	—	—	0.35	—
D1	—	7.00	—	—	0.28	—
E	—	9.00	—	—	0.35	—
E1	—	7.00	—	—	0.28	—
e	—	0.50	—	—	0.02	—
L	0.45	0.60	0.75	0.018	—	0.030
L1	—	1.00	—	—	0.039	—
y	—	0.10	—	—	0.004	—
θ	0°	—	7°	0°	—	7°

Note:
1. Dimension D & E1 do not include mold protrusion. D and E1 are maximum plastic body size dimension including mold mismatch.
2. Dimension B1 does not include dambar protrusion.

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