

## 32-Channel Vacuum-Fluorescent Display Driver

### Features

- ▶ 32 output lines
- ▶ 90V output swing
- ▶ Active pull-down
- ▶ Latches on all outputs
- ▶ Up to 6.0MHz @  $V_{DD} = 5.0V$
- ▶ -40°C to +85°C operation

### Applications

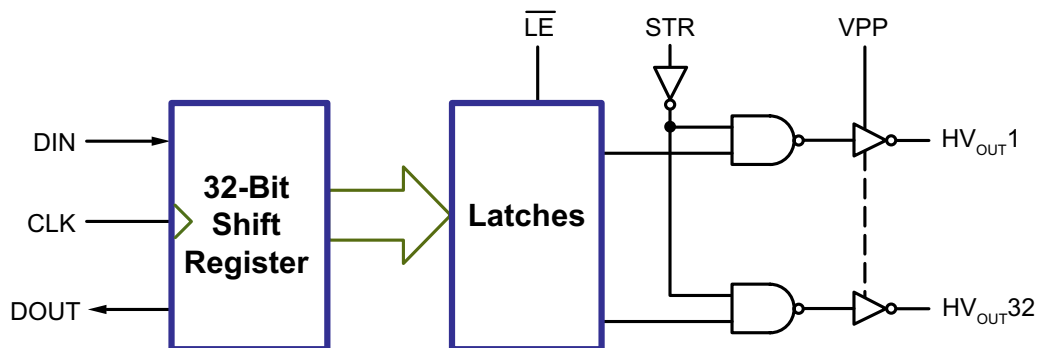
- ▶ Vacuum fluorescent displays
- ▶ DC plasma displays

### General Description

The HV518 is designed for vacuum fluorescent or DC plasma applications, where it can serve as a segment, digit or matrix display driver. Each device has 32 outputs, 32 latches and a 32-bit cascadable shift register.

Serial data enters the shift register on the LOW-to-HIGH transition of the clock input. With latch enable ( $\overline{LE}$ ) HIGH, parallel data is transferred to the output buffers through a 32-bit latch. When  $\overline{LE}$  is low the data is stored in the latch. When STROBE (STR) is LOW, all outputs are enabled; if STROBE is HIGH, all outputs are LOW.

### Block Diagram



## Ordering Information

Device	Package Options	
	40-Lead PDIP 2.095x.580in body (max) .250in height (max) .100in pitch	44-Lead PLCC .653x.653in body .180in height (max) .050in pitch
HV518	HV518P-G	HV518PJ-G

-G indicates package is RoHS compliant ('Green')



## Absolute Maximum Ratings

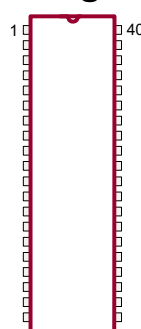
Parameter	Value
Supply voltage, $V_{DD}$	-0.5V to +6.0V
Supply voltage, $V_{PP}$	-0.5V to +90V
Logic input levels	-0.5V to $V_{DD} + 0.5V$
Continuous total power dissipation <sup>1,2</sup>	1200mW
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to GND.

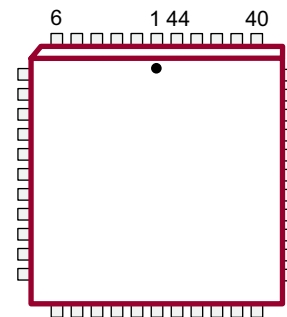
### Notes:

- Duty cycle is limited by the total power dissipated in the package.
- For operation above 25°C ambient, derate linearly to 85°C at 20mW/°C.

## Pin Configurations



40-Lead PDIP (P)  
(top view)



44-Lead PLCC (PJ)  
(top view)

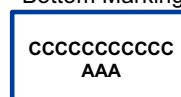
## Product Markings

### Top Marking



Y = Last Digit of Year Sealed  
 WW = Week Sealed  
 L = Lot Number  
 C = Country of Origin\*  
 A = Assembler ID\*  
 — = "Green" Packaging  
 \*May be part of top marking

### Bottom Marking



Package may or may not include the following marks: Si or

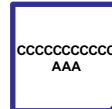
### 40-Lead PDIP (P)

### Top Marking



YY = Year Sealed  
 WW = Week Sealed  
 L = Lot Number  
 C = Country of Origin\*  
 A = Assembler ID\*  
 — = "Green" Packaging  
 \*May be part of top marking

### Bottom Marking



Package may or may not include the following marks: Si or

### 44-Lead PLCC (PJ)

## Recommended Operating Conditions ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Sym	Parameter	Min	Max	Unit	Conditions
$V_{DD}$	Logic supply voltage	4.5	5.5	V	---
$V_{PP}$	High voltage supply	8.0	80	V	---
$V_{IH}$	High-level input voltage	3.5	-	V	$V_{DD} = 4.5\text{V}$ , See Figure 1
$V_{IL}$	Low-level input voltage	-	1.0	V	$V_{DD} = 4.5\text{V}$ , See Figure 1
$I_{OH}$	High-level output current	-25	-	mA	---
$I_{OL}$	Low-level output current	-	2.0	mA	---
$f_{CLK}$	Clock frequency	-	6.0	MHz	$V_{DD} = 4.5\text{V}$ , See Figure 1
$t_{w(CKH)}$	Pulse duration, clock high	83	-	ns	$V_{DD} = 4.5\text{V}$
$t_{w(CKL)}$	Pulse duration, clock low	83	-	ns	$V_{DD} = 4.5\text{V}$
$t_{su}$	Setup time, data before clock	75	-	ns	$V_{DD} = 4.5\text{V}$
$t_h$	Hold time, data after clock	75	-	ns	$V_{DD} = 4.5\text{V}$
$T_A$	Operating ambient temperature	-40	85	$^\circ\text{C}$	---

## Electrical Characteristics (over recommended ranges of operating ambient temperature unless otherwise noted.)

Sym	Parameter	Min	Typ	Max	Units	Conditions	
$I_{DD}$	Supply current	-	-	10	mA	$V_{DD} = 5.0\text{V}$ , $f_{CH} = 6.0\text{ MHz}$	
$I_{DDQ}$	Quiescent supply current	-	-	0.5	mA	$V_{DD} = 5.5\text{V}$ , $V_{IN} = 0\text{V}$	
$I_{PP}$	Supply current	-	-	12	mA	Outputs high, $T_A = -40^\circ$	
		-	7.0	10	mA	Outputs high, $T_A = 0\text{ to }+85^\circ$	
		-	-	500	$\mu\text{A}$	Outputs low	
$V_{OH}$	HV <sub>IN</sub> operating current	HV output	70	-	-	V	$I_{OH} = -25\text{mA}$
		Serial output	4.5	4.9	5.0		$V_{DD} = 5.0\text{V}$ , $I_{OH} = -20\mu\text{A}$
$V_{OL}$	LV <sub>IN</sub> operating current	HV output	-	-	5.0	V	$I_{OL} = 1.0\text{mA}$
		Serial output	-	0.06	0.8		$I_{OL} = 20\mu\text{A}$
$I_{IH}$	Logic input current high	-	0.1	1.0	$\mu\text{A}$	$V_{IH} = V_{DD}$	
$I_{IL}$	Logic input current low	-	-0.1	-1.0	$\mu\text{A}$	$V_{IL} = 0\text{V}$	

### Note:

The total number of ON outputs times the duty cycle must not exceed the allowable package power dissipation.

## Switching Characteristics ( $V_{PP} = 80\text{V}$ , $C_L = 50\text{pF}$ , $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Sym	Parameter	Min	Typ	Max	Unit	Conditions	
$t_d$	Delay time, clock to data output	-	-	600	ns	$C_L = 15\text{pF}$ , See Figure 2	
$t_{DHL}$	Delay time, high-to-low-level, HV output	From latch enable	-	-	1.5	$\mu\text{s}$	$V_{DD} = 4.5\text{V}$ , See Figure 3
		From strobe	-	-	1.0		$V_{DD} = 4.5\text{V}$ , See Figure 4
$t_{DLH}$	Delay time, low-to-high-level, HV output	From latch enable	-	-	1.5	$\mu\text{s}$	$V_{DD} = 4.5\text{V}$ , See Figure 3
		From strobe	-	-	1.0		$V_{DD} = 4.5\text{V}$ , See Figure 4
$t_{THL}$	Transition time, high-to-low-level, HV output	-	-	3.0	$\mu\text{s}$	$V_{DD} = 4.5\text{V}$ , See Figure 4	
$t_{TLH}$	Transition time, low-to-high-level, HV output	-	-	2.5	$\mu\text{s}$	$V_{DD} = 4.5\text{V}$ , See Figure 4	

## Power-Up/ Power-Down Sequences

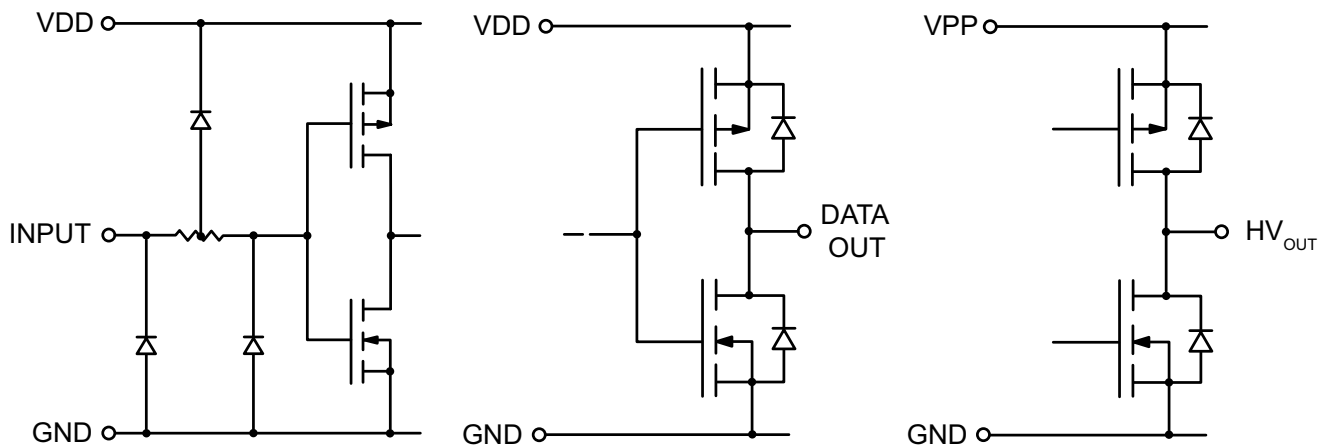
*Power-up sequence should be the following:*

1. Connect ground.
2. Apply  $V_{DD}$ .
3. Set all inputs (Data, CLK, EN, etc.) to a known state.
4. Apply  $V_{PP}$ .

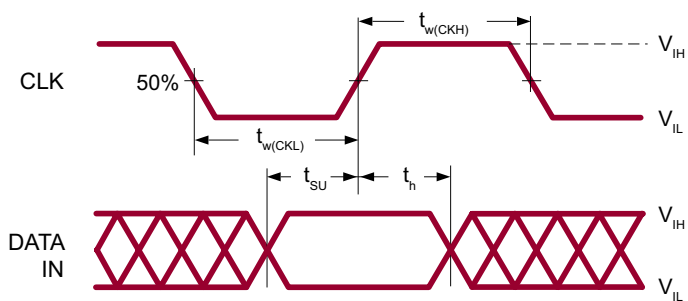
*The  $V_{PP}$  should not drop below  $V_{DD}$  or float during operation.*

*Power-down sequence should be the reverse of the above.*

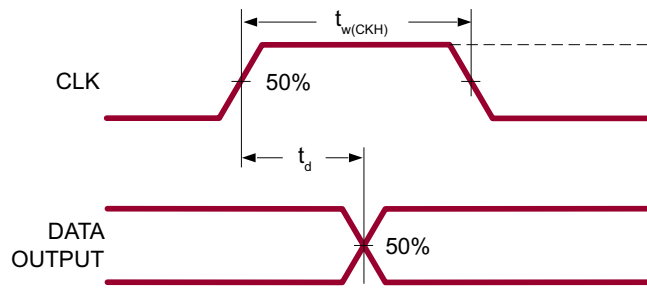
## Input and Output Equivalent Circuits



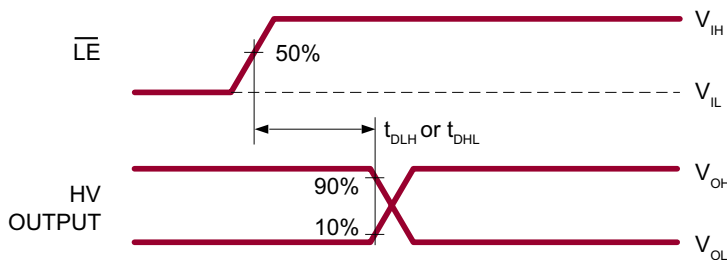
## Parameter Measurement Information



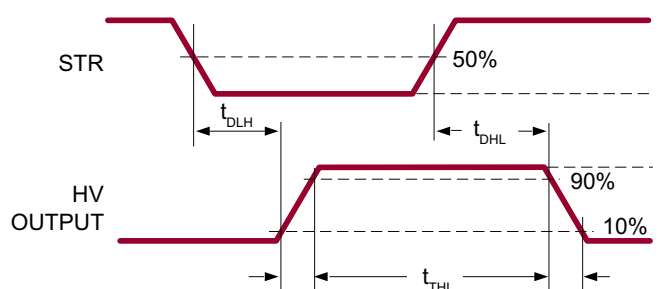
**Figure 1:** Input Timing Voltage Waveforms



**Figure 2:** Output Timing Voltage Waveforms



**Figure 3:** Timing Voltage Waveforms



**Figure 4:** Switching-Time Voltage Waveforms

**Note:**

*For testing purposes, all input pulses have maximum rise and fall times of 30 nsec.*

### Truth Tables

#### Input

Data In	CLK	Data Out
H		H
L		L
X	No Change	*

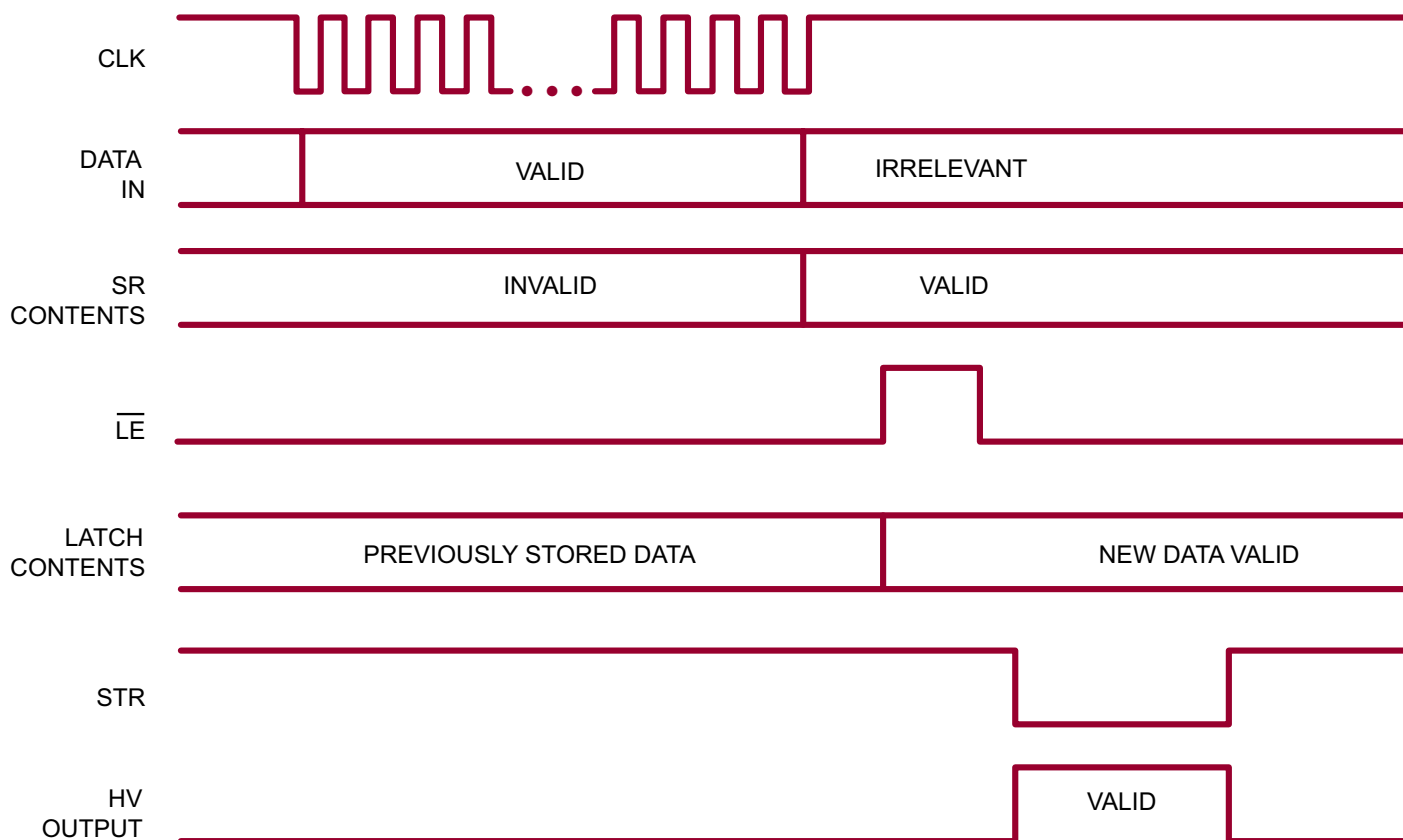
\* Previous state.

#### Output

Data In	$\overline{LE}$	STR	HV Outputs
X	X	H	All Low
H	H	L	High
L	H	L	Low
X	L	L	*

\* Previous state.

### Typical Operating Sequence



## Pin Descriptions

### 40-Lead PDIP (P)

Pin #	Function
1	VPP
2	SERIAL OUT
3	HV <sub>OUT</sub> 32
4	HV <sub>OUT</sub> 31
5	HV <sub>OUT</sub> 30
6	HV <sub>OUT</sub> 29
7	HV <sub>OUT</sub> 28
8	HV <sub>OUT</sub> 27
9	HV <sub>OUT</sub> 26
10	HV <sub>OUT</sub> 25
11	HV <sub>OUT</sub> 24
12	HV <sub>OUT</sub> 23
13	HV <sub>OUT</sub> 22
14	HV <sub>OUT</sub> 21

Pin #	Function
15	HV <sub>OUT</sub> 20
16	HV <sub>OUT</sub> 19
17	HV <sub>OUT</sub> 18
18	HV <sub>OUT</sub> 17
19	STR
20	GND
21	CLK
22	$\overline{\text{LE}}$
23	HV <sub>OUT</sub> 16
24	HV <sub>OUT</sub> 15
25	HV <sub>OUT</sub> 14
26	HV <sub>OUT</sub> 13
27	HV <sub>OUT</sub> 12
28	HV <sub>OUT</sub> 11

Pin #	Function
29	HV <sub>OUT</sub> 10
30	HV <sub>OUT</sub> 9
31	HV <sub>OUT</sub> 8
32	HV <sub>OUT</sub> 7
33	HV <sub>OUT</sub> 6
34	HV <sub>OUT</sub> 5
35	HV <sub>OUT</sub> 4
36	HV <sub>OUT</sub> 3
37	HV <sub>OUT</sub> 2
38	HV <sub>OUT</sub> 1
39	DATA IN
40	VDD

### 44-Lead PLCC (PJ)

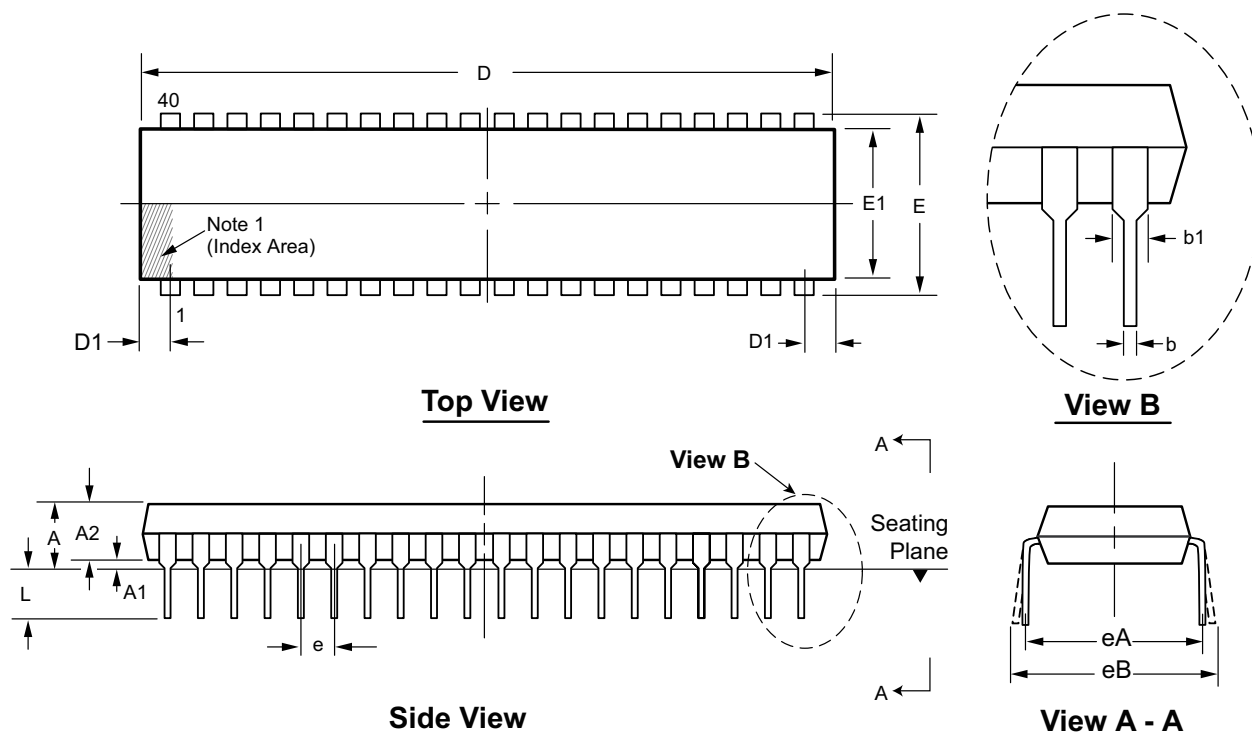
Pin #	Function
1	VPP
2	SERIAL OUT
3	HV <sub>OUT</sub> 32
4	HV <sub>OUT</sub> 31
5	HV <sub>OUT</sub> 30
6	NC
7	HV <sub>OUT</sub> 29
8	HV <sub>OUT</sub> 28
9	HV <sub>OUT</sub> 27
10	HV <sub>OUT</sub> 26
11	HV <sub>OUT</sub> 25
12	HV <sub>OUT</sub> 24
13	HV <sub>OUT</sub> 23
14	HV <sub>OUT</sub> 22
15	HV <sub>OUT</sub> 21

Pin #	Function
16	HV <sub>OUT</sub> 20
17	HV <sub>OUT</sub> 19
18	N/C
19	HV <sub>OUT</sub> 18
20	HV <sub>OUT</sub> 17
21	STR
22	GND
23	CLK
24	$\overline{\text{LE}}$
25	HV <sub>OUT</sub> 16
26	HV <sub>OUT</sub> 15
27	HV <sub>OUT</sub> 14
28	N/C
29	N/C
30	HV <sub>OUT</sub> 13

Pin #	Function
31	HV <sub>OUT</sub> 12
32	HV <sub>OUT</sub> 11
33	HV <sub>OUT</sub> 10
34	HV <sub>OUT</sub> 9
35	HV <sub>OUT</sub> 8
36	HV <sub>OUT</sub> 7
37	HV <sub>OUT</sub> 6
38	HV <sub>OUT</sub> 5
39	HV <sub>OUT</sub> 4
40	HV <sub>OUT</sub> 3
41	HV <sub>OUT</sub> 2
42	HV <sub>OUT</sub> 1
43	DATA IN
44	VDD

# 40-Lead PDIP (.600in Row Spacing) Package Outline (P)

2.095x.580in body (max), .250in height (max), .100in pitch



**Note:**  
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	eA	eB	L	
Dimension (inches)	MIN	.140*	.015	.125	.014	.030	1.980	.065 <sup>†</sup>	.590 <sup>†</sup>	.485	.100 BSC	.600 BSC	.600*	.115
	NOM	-	-	-	-	-	-	-	-	-			-	-
	MAX	.250	.055*	.195	.023 <sup>†</sup>	.070	2.095	.085*	.625	.580			.700	.200

JEDEC Registration MS-011, Variation AC, Issue B, June, 1988.

\* This dimension is not specified in the JEDEC drawing.

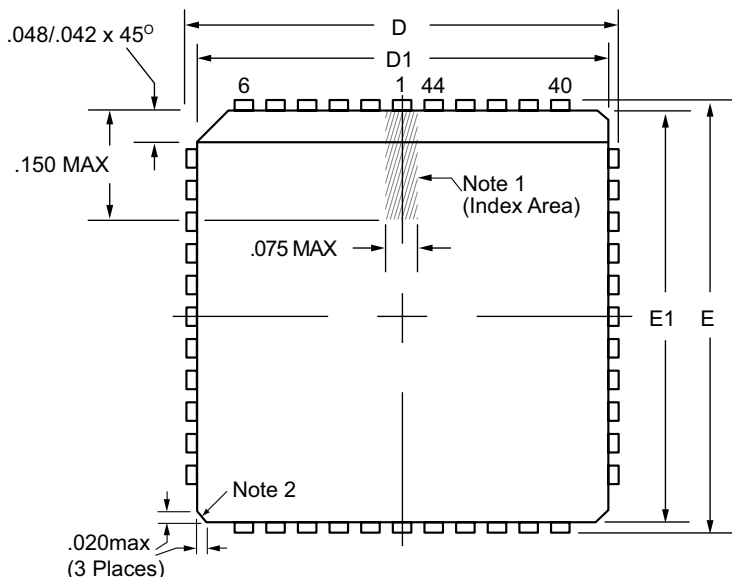
† This dimension differs from the JEDEC drawing.

Drawings not to scale.

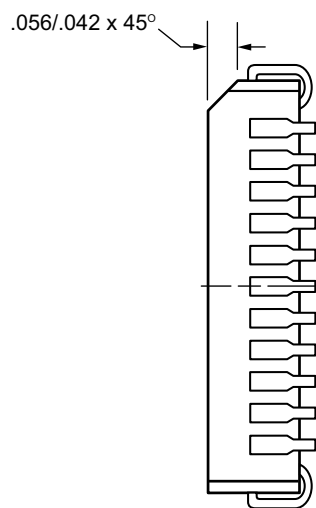
Supertex Doc. #: DSPD-40DIPP, Version D041009.

# 44-Lead PLCC Package Outline (PJ)

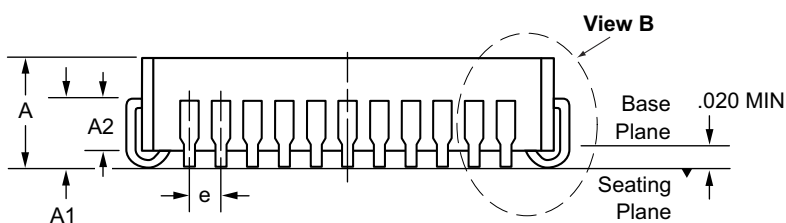
.653x.653in body, .180in height (max), .050in pitch



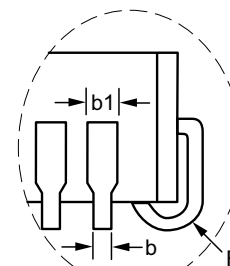
**Top View**



**Vertical Side View**



**Horizontal Side View**



**View B**

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Actual shape of this feature may vary.

Symbol	A	A1	A2	b	b1	D	D1	E	E1	e	R	
Dimension (inches)	MIN	.165	.090	.062	.013	.026	.685	.650	.685	.650	.050 BSC	.025
	NOM	.172	.105	-	-	-	.690	.653	.690	.653		.035
	MAX	.180	.120	.083	.021	.036 <sup>†</sup>	.695	.656	.695	.656		.045

JEDEC Registration MS-018, Variation AC, Issue A, June, 1993.

<sup>†</sup> This dimension differs from the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #: DSPD-44PLCCPJ, Version F031111.**

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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