



N-Channel Enhancement-Mode Vertical DMOS FET

Features

- ▶ Low threshold (2.0V max.)
- ▶ High input impedance and high gain
- ▶ Free from secondary breakdown
- ▶ Low C_{iss} and fast switching speeds

Applications

- ▶ Logic level interfaces - ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options			BV_{DSS}/BV_{DGS} (V)	$R_{DS(ON)}$ (max) (Ω)	$I_{D(ON)}$ (min) (A)	$V_{GS(th)}$ (max) (V)
	TO-236AB (SOT-23)	TO-92	TO-243AA (SOT-89)				
TN5325	TN5325K1-G	TN5325N3-G	TN5325N8-G	250	7.0	1.2	2.0

-G indicates package is RoHS compliant ('Green')



Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV_{DSS}
Drain-to-gate voltage	BV_{DGS}
Gate-to-source voltage	$\pm 20V$
Operating and storage temperature	$-55^{\circ}C$ to $+150^{\circ}C$
Soldering temperature*	$300^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations



Product Marking

N3CW W = Code for week sealed
_____ = "Green" Packaging
TO-236AB (SOT-23) (K1)

SiTN YY = Year Sealed
5 3 2 5 WW = Week Sealed
YYWW _____ = "Green" Packaging
TO-92 (N3)

TN3CW W = Code for week sealed
_____ = "Green" Packaging
TO-243AA (SOT-89) (N8)

Packages may or may not include the following marks: Si or

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (A)	Power Dissipation @ $T_A = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR} [†] (mA)	I_{DRM} (A)
TO-236AB (SOT-23)	150	0.4	0.36	200	350	150	0.4
TO-92	215	0.8	0.74	125	170	215	0.8
TO-243AA (SOT-89)	316	1.5	1.6 [‡]	15	78 [‡]	316	1.5

Notes:

[†] I_D (continuous) is limited by max rated T_j .

[‡] Mounted on FR5 Board, 25mm x 25mm x 1.57mm.

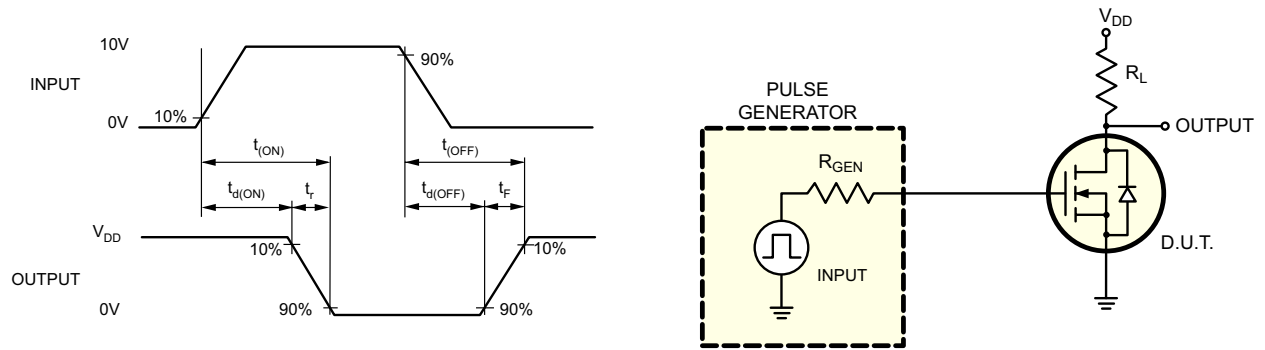
Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSS}	Drain-to-source breakdown voltage	250	-	-	V	$V_{GS} = 0V, I_D = 100\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	0.6	-	2.0	V	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
$\Delta V_{GS(th)}$	Change in $V_{GS(th)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{GS} = V_{DS}, I_D = 1.0\text{mA}$
I_{GSS}	Gate body leakage	-	-	100	nA	$V_{GS} = \pm 20V, V_{DS} = 0V$
I_{DSS}	Zero gate voltage drain current	-	-	1.0	μA	$V_{GS} = 0V, V_{DS} = 100V$
		-	-	10		$V_{GS} = 0V, V_{DS} = \text{Max Rating}$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}, V_{GS} = 0V, T_A = 125^\circ\text{C}$
$I_{D(ON)}$	On-state drain current	0.6	-	-	A	$V_{GS} = 4.5V, V_{DS} = 25V$
		1.2	-	-		$V_{GS} = 10V, V_{DS} = 25V$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	-	8.0	Ω	$V_{GS} = 4.5V, I_D = 150\text{mA}$
		-	-	7.0		$V_{GS} = 10V, I_D = 1.0\text{A}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.0	%/ $^\circ\text{C}$	$V_{GS} = 4.5V, I_D = 150\text{mA}$
G_{FS}	Forward transductance	150	-	-	mmho	$V_{DS} = 25V, I_D = 200\text{mA}$
C_{ISS}	Input capacitance	-	-	110	pF	$V_{GS} = 0V,$ $V_{DS} = 25V,$ $f = 1.0\text{MHz}$
C_{OSS}	Common source output capacitance	-	-	60		
C_{RSS}	Reverse transfer capacitance	-	-	23		
$t_{d(ON)}$	Turn-on delay time	-	-	20	ns	$V_{DD} = 25V,$ $I_D = 150\text{mA},$ $R_{GEN} = 25\Omega$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	25		
t_f	Fall time	-	-	25		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = 0V, I_{SD} = 200\text{mA}$
t_{rr}	Reverse recovery time	-	300	-	ns	$V_{GS} = 0V, I_{SD} = 200\text{mA}$

Notes:

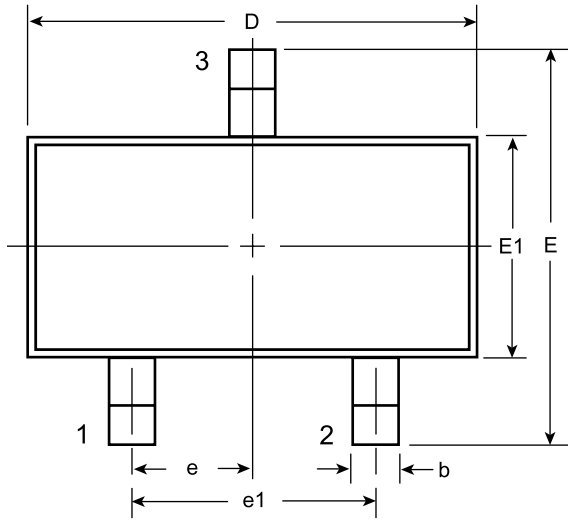
- All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300 μs pulse, 2% duty cycle.)
- All A.C. parameters sample tested.

Switching Waveforms and Test Circuit

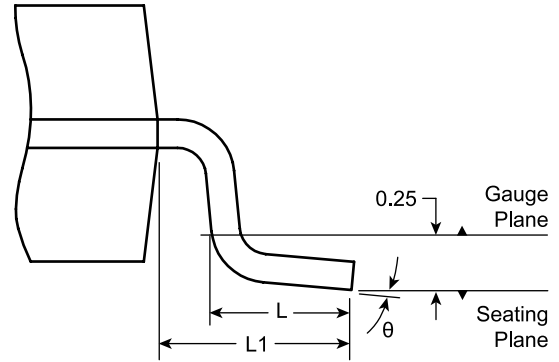


3-Lead TO-236AB (SOT-23) Package Outline (K1)

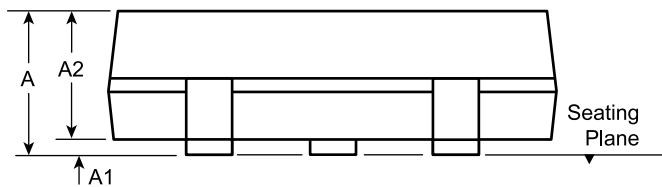
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



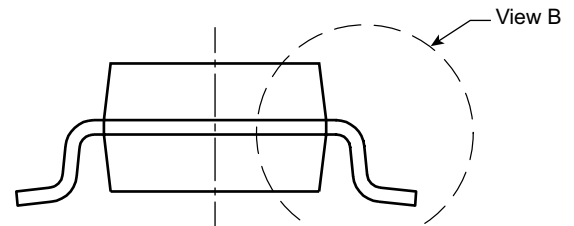
Top View



View B



Side View



View A - A

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	θ
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 [†]	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

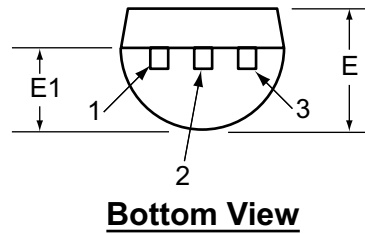
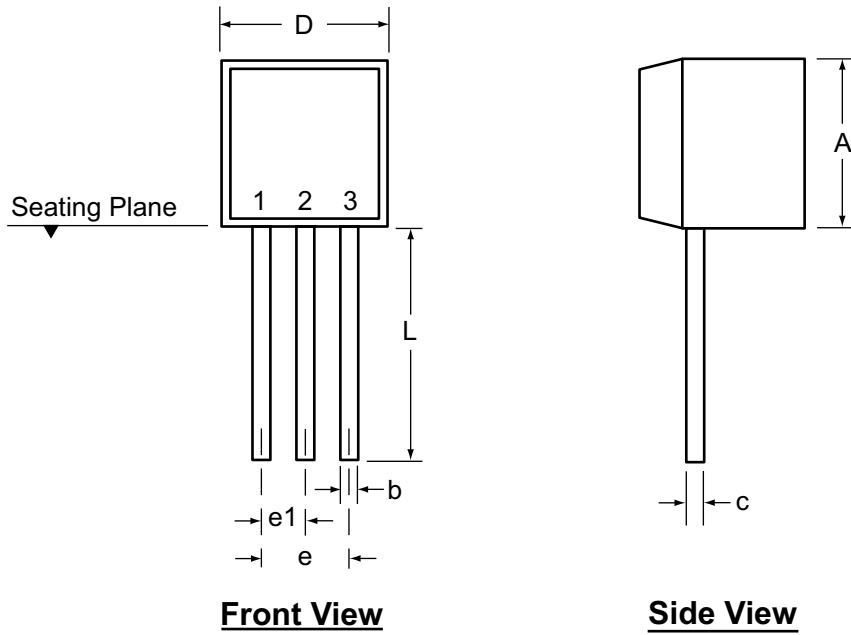
JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

[†] This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO236ABK1, Version C041309.

3-Lead TO-92 Package Outline (N3)



Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

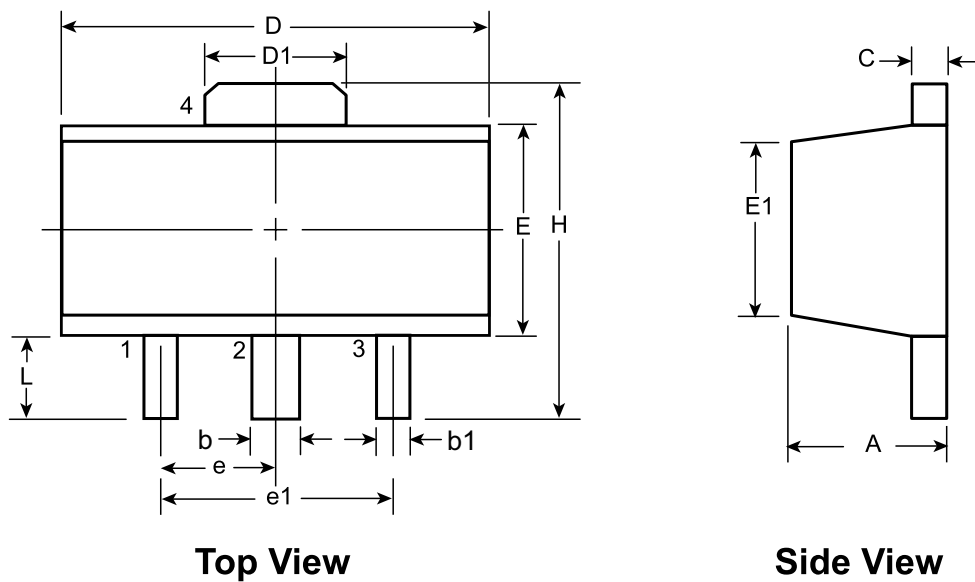
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Top View

Side View

Symbol	A	b	b1	C	D	D1	E	E1	e	e1	H	L		
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

† This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version E051509.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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