



## N-Channel Enhancement-Mode Vertical DMOS FET

### Features

- ▶ Free from secondary breakdown
- ▶ Low power drive requirement
- ▶ Ease of paralleling
- ▶ Low  $C_{ISS}$  and fast switching speeds
- ▶ Excellent thermal stability
- ▶ Integral source-drain diode
- ▶ High input impedance and high gain

### Applications

- ▶ Logic level interfaces – ideal for TTL and CMOS
- ▶ Solid state relays
- ▶ Battery operated systems
- ▶ Photo-voltaic drives
- ▶ Analog switches
- ▶ General purpose line drivers
- ▶ Telecom switches

### General Description

This low threshold, enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

### Ordering Information

Device	Package Option	$BV_{DSS}/BV_{DGS}$ (V)	$R_{DS(ON)}$ (max) ( $\Omega$ )	$V_{GS(th)}$ (max) (V)
	TO-236AB (SOT-23)			
TN2130	TN2130K1-G	300	25	2.4

-G indicates package is RoHS compliant ('Green')



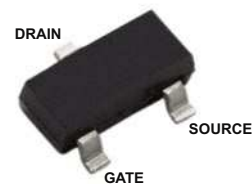
### Absolute Maximum Ratings

Parameter	Value
Drain-to-Source	$BV_{DSS}$
Drain-to-Gate	$BV_{DGS}$
Gate-to-Source	$\pm 20V$
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

\* Distance of 1.6mm from case for 10 seconds.

### Pin Configuration



TO-236AB (SOT-23) (K1)

### Product Marking

**N1TW** W = Code for Week Sealed  
 \_\_\_\_\_ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-236AB (SOT-23) (K1)

### Thermal Characteristics

Package	I <sub>D</sub> (continuous) <sup>†</sup> (mA)	I <sub>D</sub> (pulsed) (mA)	Power Dissipation @T <sub>A</sub> = 25°C (W)	θ <sub>JC</sub> (°C/W)	θ <sub>JA</sub> (°C/W)	I <sub>DR</sub> <sup>†</sup> (mA)	I <sub>DRM</sub> (mA)
TO-236AB (SOT-23)	85	200	0.36	200	350	85	200

**Notes:**

<sup>†</sup> I<sub>D</sub> (continuous) is limited by max rated T<sub>J</sub>.

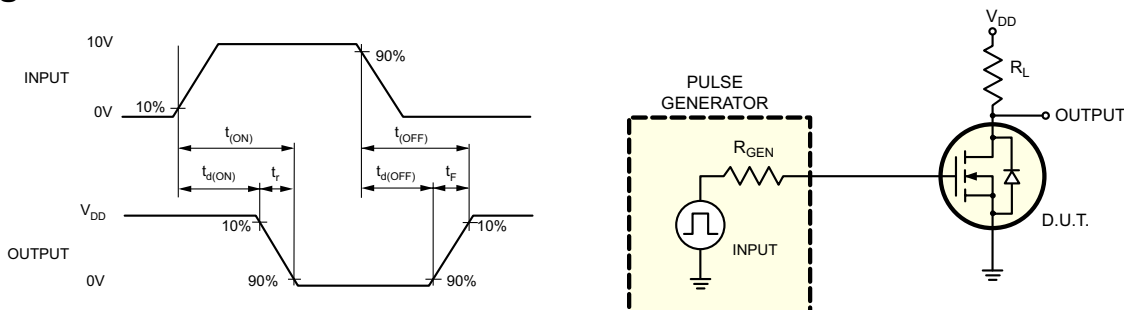
### Electrical Characteristics (T<sub>A</sub> = 25°C unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV <sub>DSS</sub>	Drain-to-source breakdown voltage	300	-	-	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 1.0mA
V <sub>GS(th)</sub>	Gate threshold voltage	0.8	-	2.4	V	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
ΔV <sub>GS(th)</sub>	Change in V <sub>GS(th)</sub> with temperature	-	-	-5.5	mV/°C	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 1.0mA
I <sub>GSS</sub>	Gate body leakage	-	-	100	nA	V <sub>GS</sub> = ± 20V, V <sub>DS</sub> = 0V
I <sub>DSS</sub>	Zero gate voltage drain current	-	-	10	μA	V <sub>GS</sub> = 0V, V <sub>DS</sub> = Max Rating
		-	-	100		V <sub>DS</sub> = 0.8Max Rating, V <sub>GS</sub> = 0V, T <sub>A</sub> = 125°C
I <sub>D(ON)</sub>	On-state drain current	250	-	-	mA	V <sub>GS</sub> = 10V, V <sub>DS</sub> = 25V
R <sub>DS(ON)</sub>	Static drain-to-source on-state resistance	-	-	25	Ω	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 120mA
ΔR <sub>DS(ON)</sub>	Change in R <sub>DS(ON)</sub> with temperature	-	-	1.1	%/°C	V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 120mA
G <sub>FS</sub>	Forward transductance	-	250	-	mmho	V <sub>DS</sub> = 25V, I <sub>D</sub> = 100mA
C <sub>ISS</sub>	Input capacitance	-	-	50	pF	V <sub>GS</sub> = 0V, V <sub>DS</sub> = 25V, f = 1.0MHz
C <sub>OSS</sub>	Common source output capacitance	-	-	15		
C <sub>RSS</sub>	Reverse transfer capacitance	-	-	5.0		
t <sub>d(ON)</sub>	Turn-on delay time	-	-	10	ns	V <sub>DD</sub> = 25V, I <sub>D</sub> = 120mA, R <sub>GEN</sub> = 25Ω
t <sub>r</sub>	Rise time	-	-	7.0		
t <sub>d(OFF)</sub>	Turn-off delay time	-	-	12		
t <sub>f</sub>	Fall time	-	-	15		
V <sub>SD</sub>	Diode forward voltage drop	-	-	1.8	V	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 120mA
t <sub>rr</sub>	Reverse recovery time	-	400	-	ns	V <sub>GS</sub> = 0V, I <sub>SD</sub> = 120mA

**Notes:**

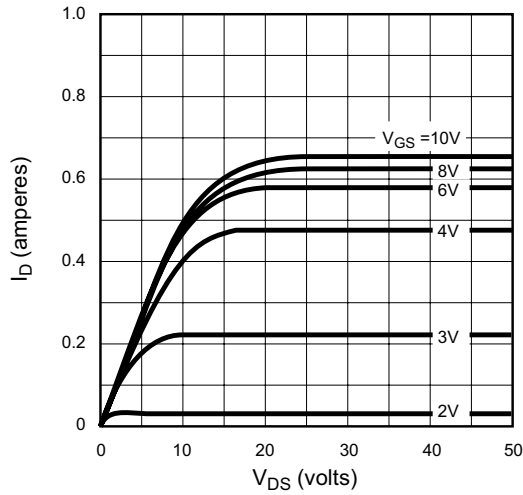
1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300μs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

### Switching Waveforms and Test Circuit

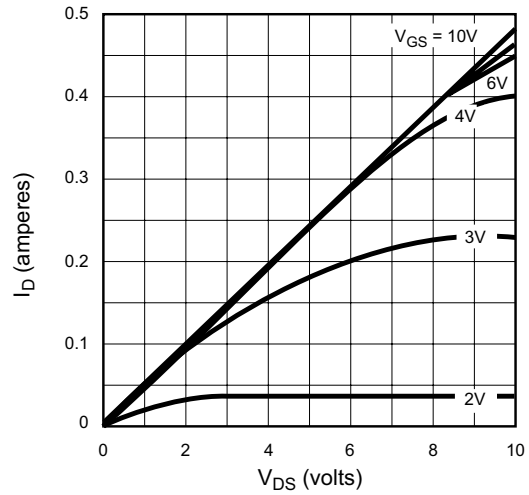


# Typical Performance Curves

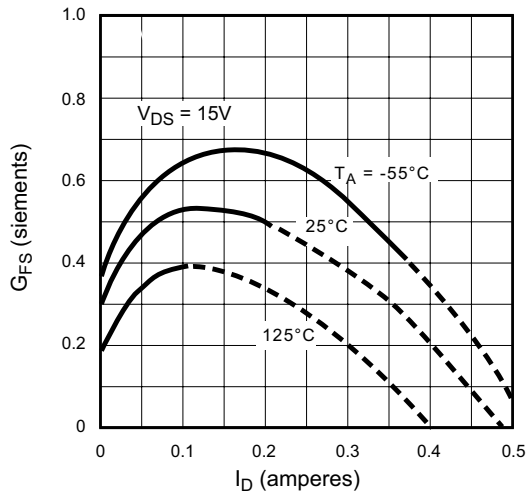
Output Characteristics



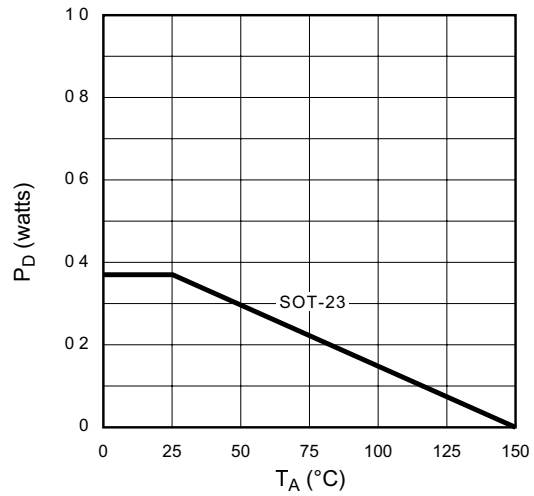
Saturation Characteristics



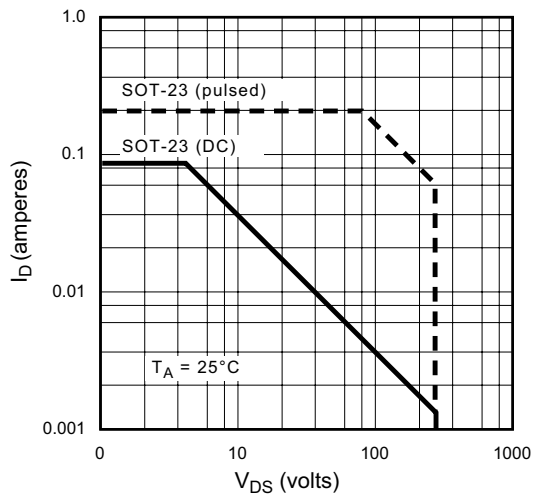
Transconductance vs. Drain Current



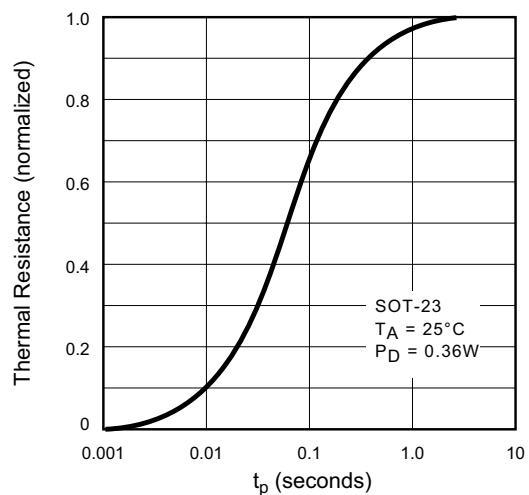
Power Dissipation vs. Temperature



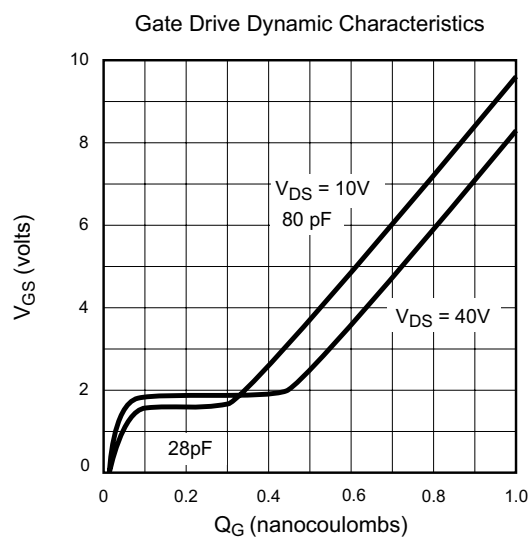
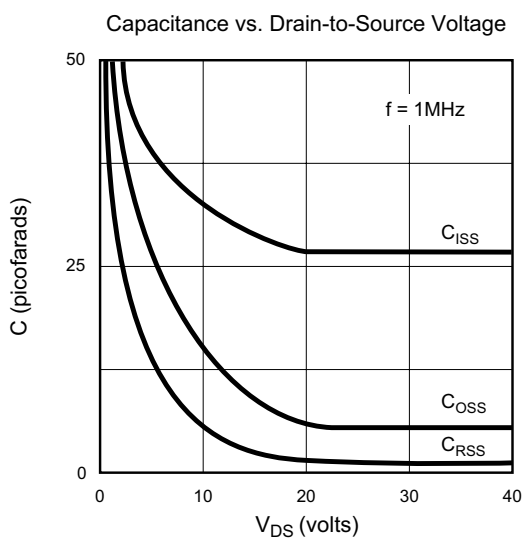
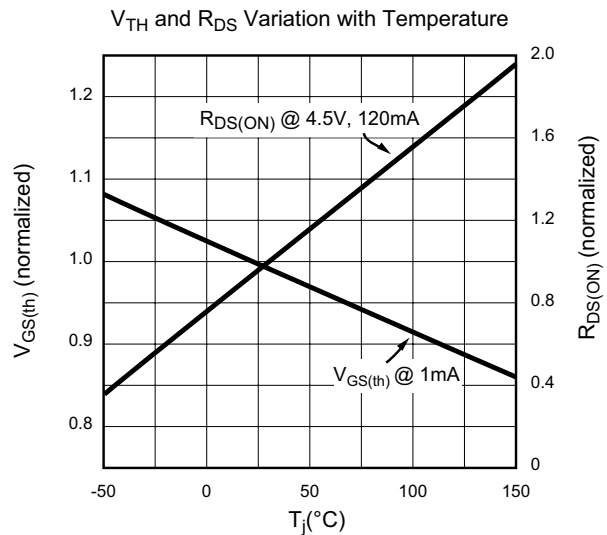
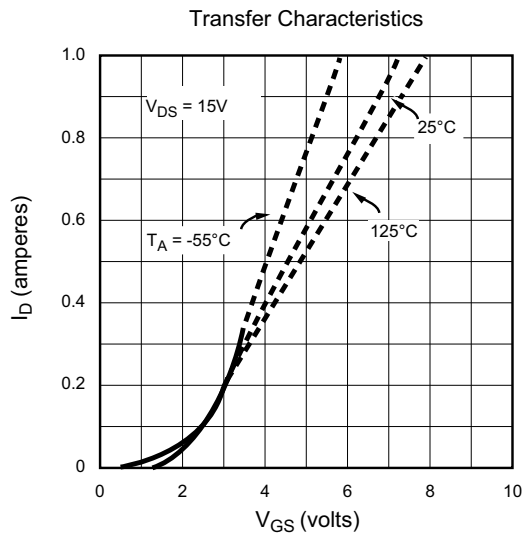
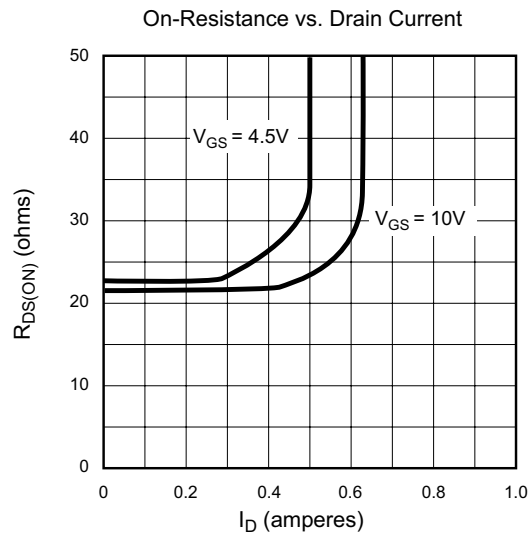
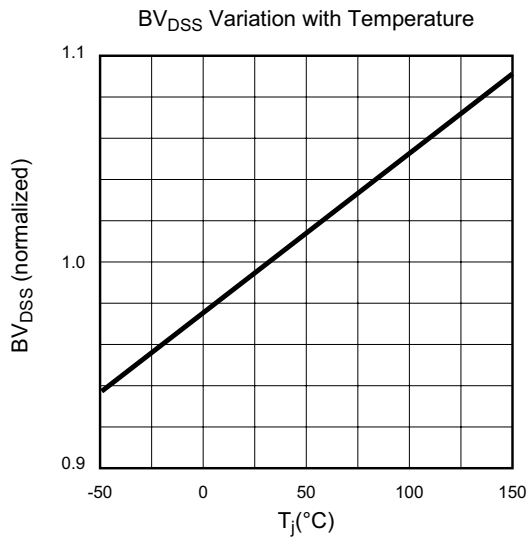
Maximum Rated Safe Operating Area



Thermal Response Characteristics

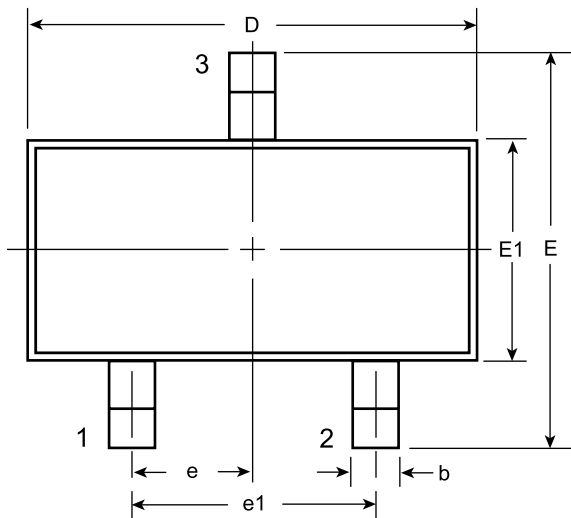


Typical Performance Curves (cont.)

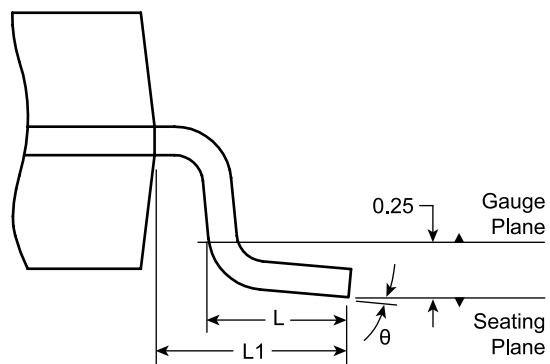


### 3-Lead TO-236AB (SOT-23) Package Outline (K1)

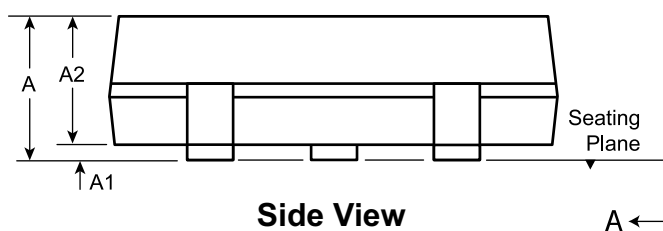
2.90x1.30mm body, 1.12mm height (max), 1.90mm pitch



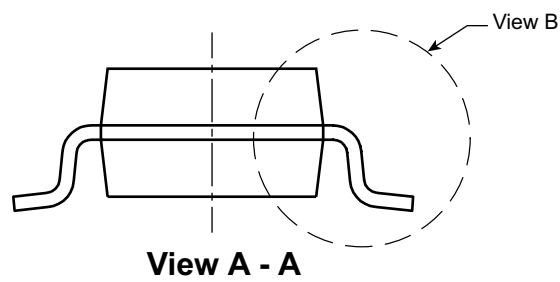
**Top View**



**View B**



**Side View**



**View A - A**

Symbol		A	A1	A2	b	D	E	E1	e	e1	L	L1	$\theta$
Dimension (mm)	MIN	0.89	0.01	0.88	0.30	2.80	2.10	1.20	0.95 BSC	1.90 BSC	0.20 <sup>†</sup>	0.54 REF	0°
	NOM	-	-	0.95	-	2.90	-	1.30			0.50		-
	MAX	1.12	0.10	1.02	0.50	3.04	2.64	1.40			0.60		8°

JEDEC Registration TO-236, Variation AB, Issue H, Jan. 1999.

<sup>†</sup> This dimension is a non-JEDEC dimension.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO236ABK1, Version B072208.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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