



N-Channel Depletion-Mode Vertical DMOS FETs

Features

- ▶ High input impedance
- ▶ Low input capacitance
- ▶ Fast switching speeds
- ▶ Low on-resistance
- ▶ Free from secondary breakdown
- ▶ Low input and output leakage

Applications

- ▶ Normally-on switches
- ▶ Solid state relays
- ▶ Converters
- ▶ Linear amplifiers
- ▶ Constant current sources
- ▶ Power supply circuits
- ▶ Telecom

General Description

The Supertex DN2540 is a low threshold depletion mode (normally-on) transistor utilizing an advanced vertical DMOS structure and Supertex's well-proven silicon-gate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and with the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package Options			BV _{DSX} /BV _{DGX} (V)	R _{DS(ON)} (max) (Ω)	I _{DSS} (min) (mA)
	TO-92	TO-220	TO-243AA (SOT-89)			
DN2540	DN2540N3-G	DN2540N5-G	DN2540N8-G	400	25	150

-G indicates package is RoHS compliant ('Green')



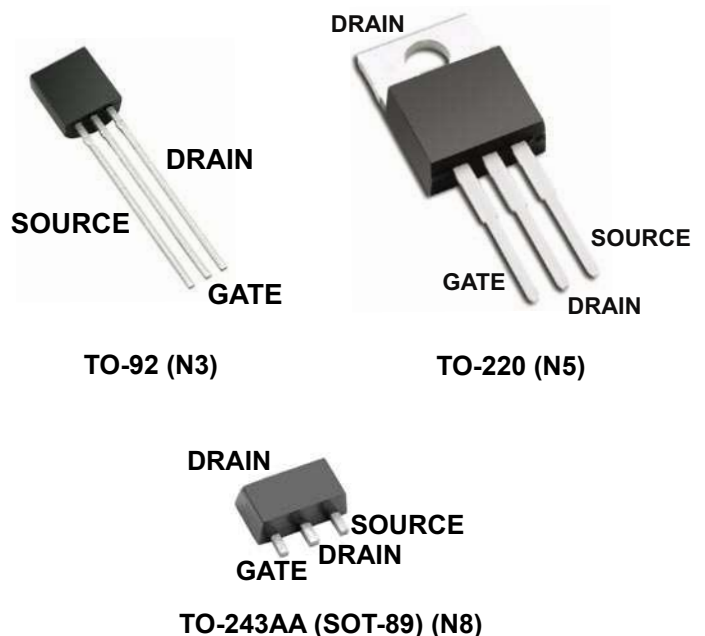
Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV _{DSX}
Drain-to-gate voltage	BV _{DGX}
Gate-to-source voltage	±20V
Operating and storage temperature	-55°C to +150°C
Soldering temperature*	300°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

* Distance of 1.6mm from case for 10 seconds.

Pin Configurations



Product Marking



YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)



L = Lot Number
 YY = Year Sealed
 WW = Week Sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-220 (N5)



W = Code for week sealed
 _____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-243AA (SOT-89) (N8)

Thermal Characteristics

Package	I_D (continuous) [†] (mA)	I_D (pulsed) (mA)	Power Dissipation @ $T_c = 25^\circ\text{C}$ (W)	θ_{jc} ($^\circ\text{C}/\text{W}$)	θ_{ja} ($^\circ\text{C}/\text{W}$)	I_{DR}^\ddagger (mA)	I_{DRM} (mA)
TO-92	120	500	1.0	125	170	120	500
TO-220	500	500	15	8.3	70	500	500
TO-243AA	170	500	1.6 [‡] ($T_A = 25^\circ\text{C}$)	15	78 [‡]	170	500

Notes:

- [†] I_D (continuous) is limited by max rated T_j
- [‡] Mounted on FR5 board, 25mm x 25mm x 1.57mm, $T_A = 25^\circ\text{C}$.

Electrical Characteristics ($T_A = 25^\circ\text{C}$ unless otherwise specified)

Sym	Parameter	Min	Typ	Max	Units	Conditions
BV_{DSX}	Drain-to-source breakdown voltage	400	-	-	V	$V_{GS} = -5.0\text{V}$, $I_D = 100\mu\text{A}$
$V_{GS(OFF)}$	Gate-to-source off voltage	-1.5	-	-3.5	V	$V_{DS} = 25\text{V}$, $I_D = 10\mu\text{A}$
$\Delta V_{GS(OFF)}$	Change in $V_{GS(OFF)}$ with temperature	-	-	-4.5	mV/ $^\circ\text{C}$	$V_{DS} = 25\text{V}$, $I_D = 10\mu\text{A}$
I_{GSS}	Gate body leakage current	-	-	100	nA	$V_{GS} = \pm 20\text{V}$, $V_{DS} = 0\text{V}$
$I_{D(OFF)}$	Drain-to-source leakage current	-	-	10	μA	$V_{DS} = \text{Max rating}$, $V_{GS} = -10\text{V}$
		-	-	1.0	mA	$V_{DS} = 0.8 \text{ Max Rating}$, $V_{GS} = -10\text{V}$, $T_A = 125^\circ\text{C}$
I_{DSS}	Saturated drain-to-source current	150	-	-	mA	$V_{GS} = 0\text{V}$, $V_{DS} = 25\text{V}$
$R_{DS(ON)}$	Static drain-to-source on-state resistance	-	17	25	Ω	$V_{GS} = 0\text{V}$, $I_D = 120\text{mA}$
$\Delta R_{DS(ON)}$	Change in $R_{DS(ON)}$ with temperature	-	-	1.1	%/ $^\circ\text{C}$	$V_{GS} = 0\text{V}$, $I_D = 120\text{mA}$
G_{FS}	Forward transconductance	-	325	-	mmho	$V_{DS} = 10\text{V}$, $I_D = 100\text{mA}$
C_{ISS}	Input capacitance	-	200	300	pF	$V_{GS} = -10\text{V}$, $V_{DS} = 25\text{V}$, $f = 1\text{MHz}$
C_{OSS}	Common source output capacitance	-	12	30		
C_{RSS}	Reverse transfer capacitance	-	1.0	5.0		

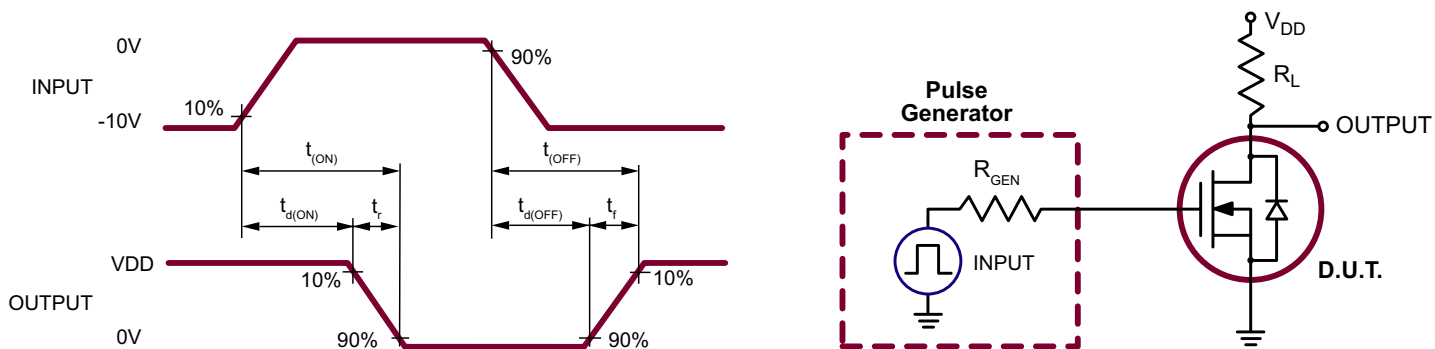
Electrical Characteristics (cont.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$t_{d(ON)}$	Turn-on delay time	-	-	10	ns	$V_{DD} = 25V,$ $I_D = 150mA,$ $R_{GEN} = 25\Omega,$
t_r	Rise time	-	-	15		
$t_{d(OFF)}$	Turn-off delay time	-	-	15		
t_f	Fall time	-	-	20		
V_{SD}	Diode forward voltage drop	-	-	1.8	V	$V_{GS} = -10V, I_{SD} = 120mA$
t_{rr}	Reverse recovery time	-	800	-	ns	$V_{GS} = -10V, I_{SD} = 1.0A$

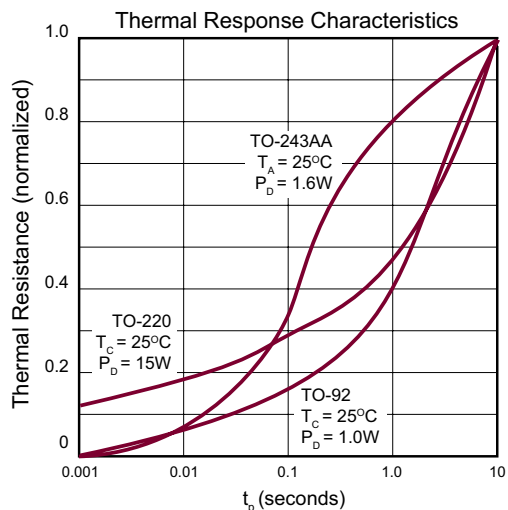
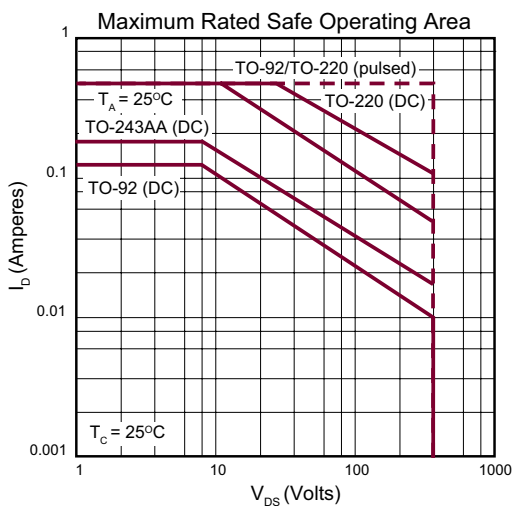
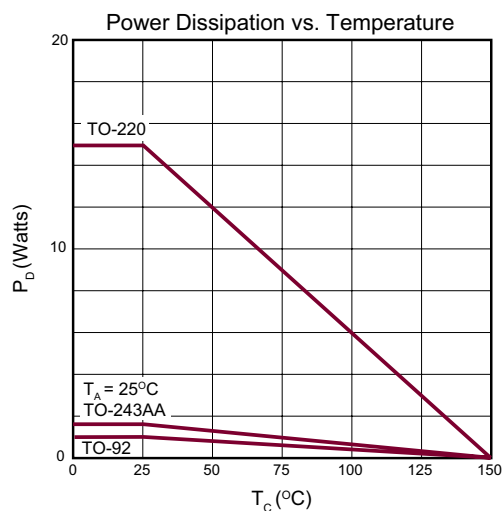
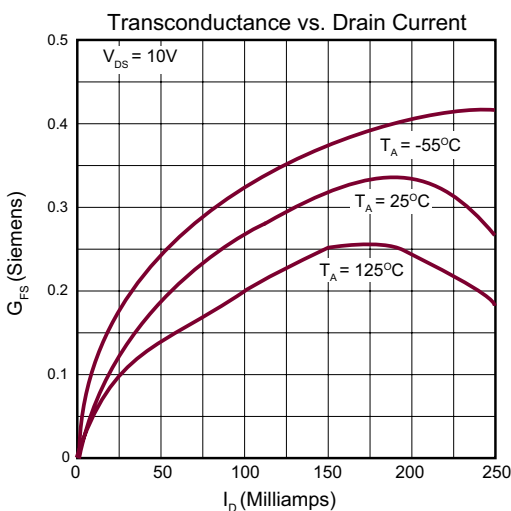
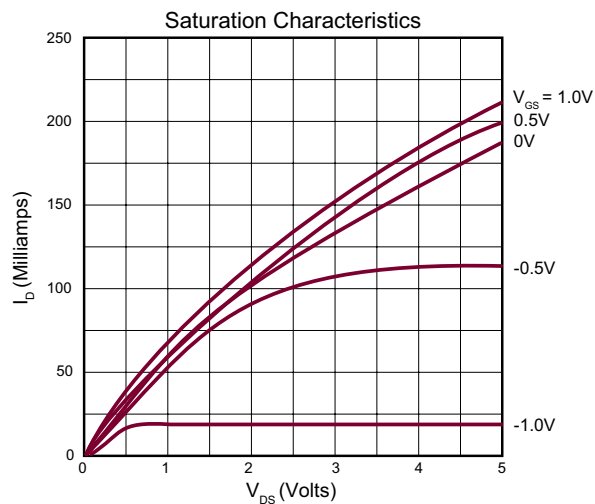
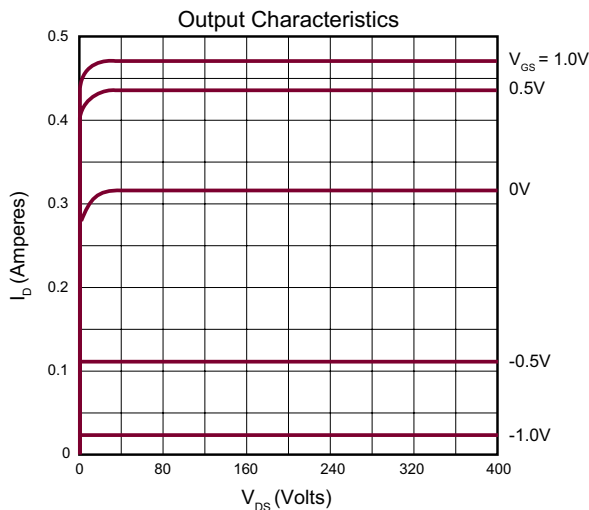
Notes:

1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
2. All A.C. parameters sample tested.

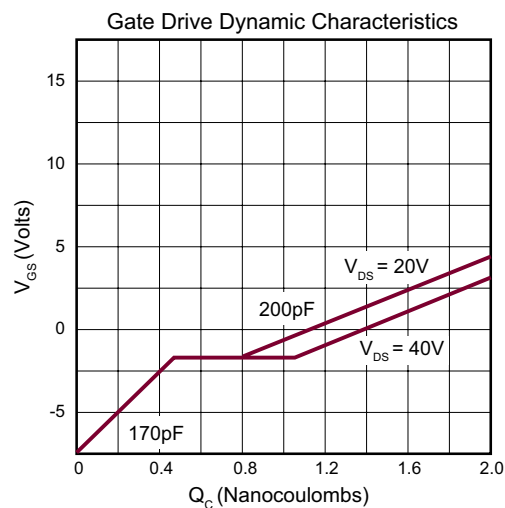
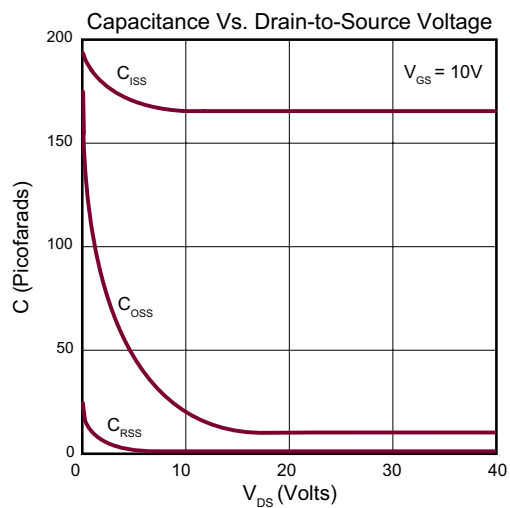
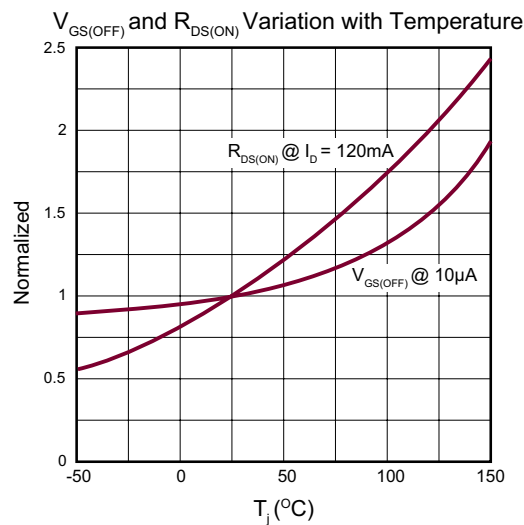
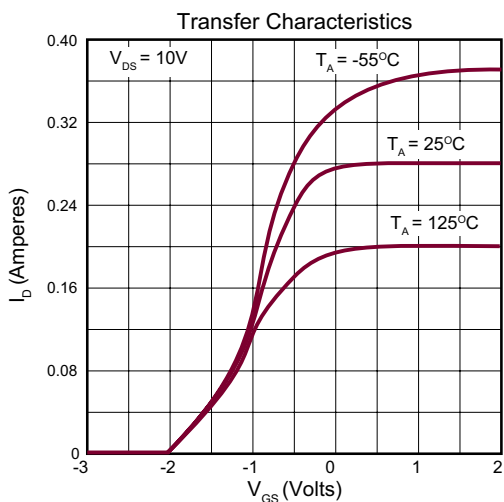
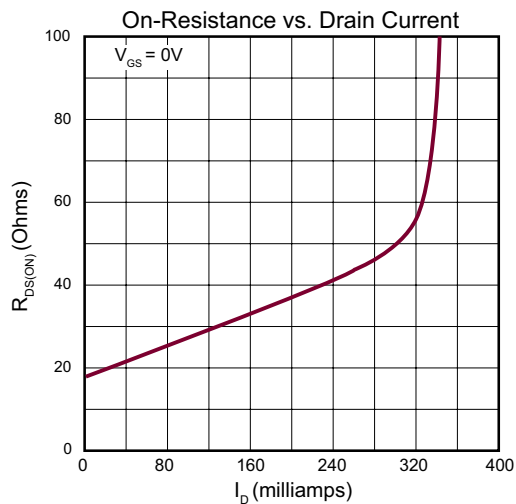
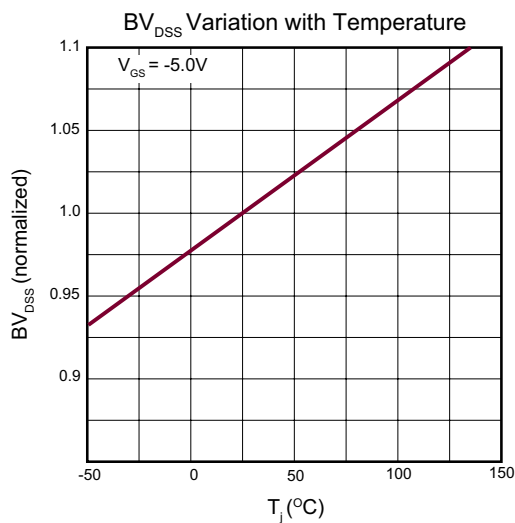
Switching Waveforms and Test Circuit



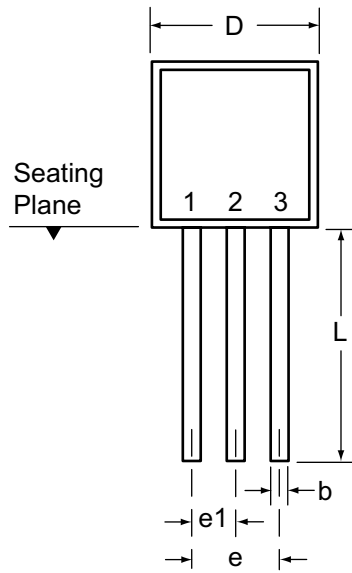
Typical Performance Curves



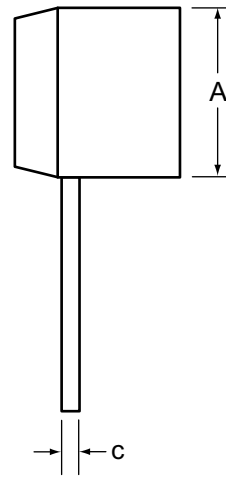
Typical Performance Curves (cont.)



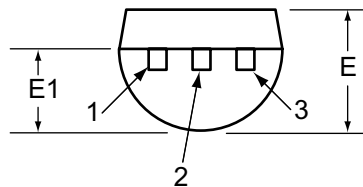
3-Lead TO-92 Package Outline (N3)



Front View



Side View



Bottom View

Symbol	A	b	c	D	E	E1	e	e1	L	
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

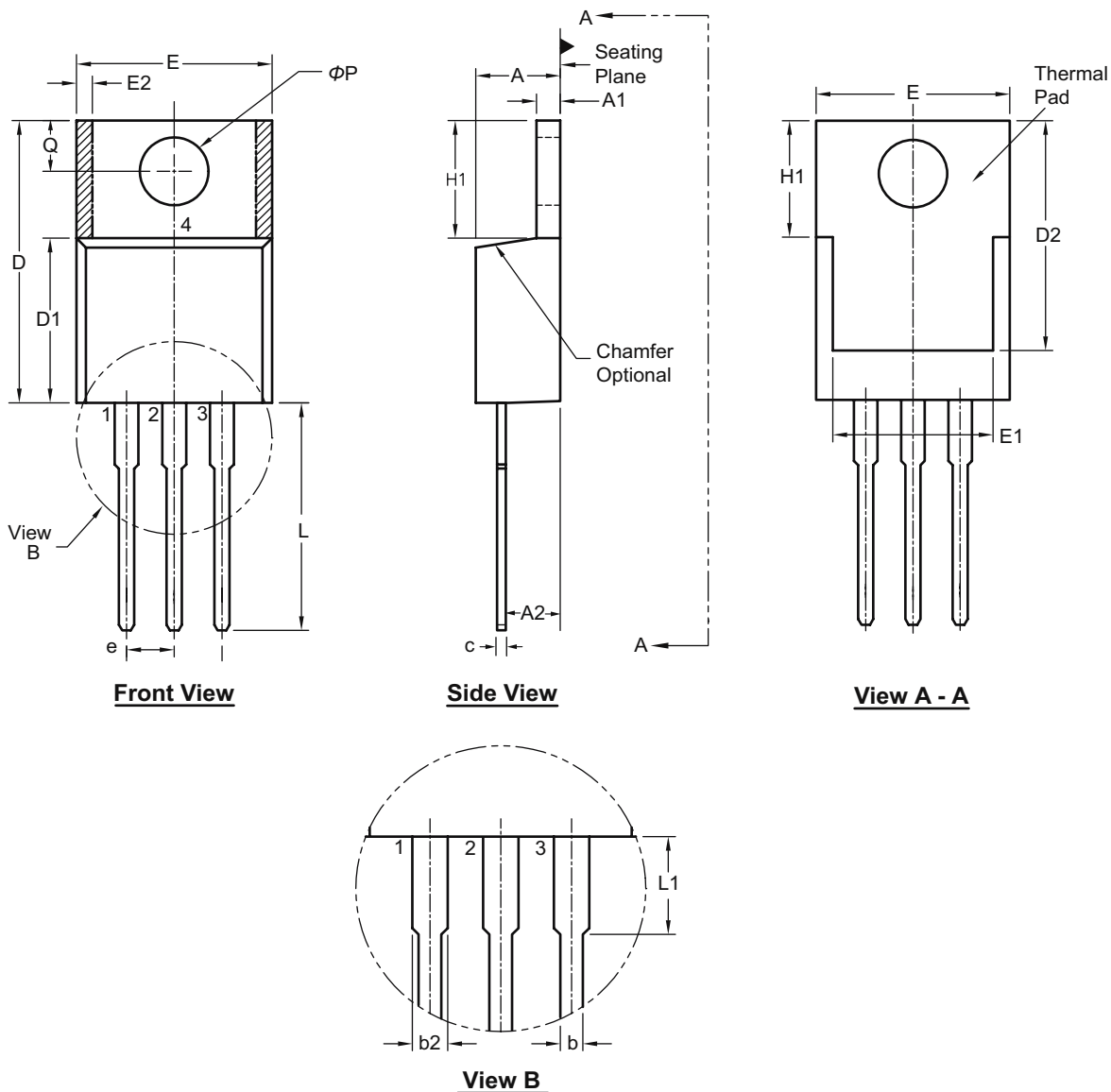
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

3-Lead TO-220 Package Outline (N5)



Symbol	A	A1	A2	b	b2	c	D	D1	D2	E	E1	E2	e	H1	L	L1	Q	ϕP		
Dimension (inches)	MIN	.140	.020	.080	.015	.045	.012†	.560	.326†	.474†	.380	.270	0.20*	.100 BSC	.230	.500	.200*	.100	.139	
	NOM	-	-	-	.027	.057	-	-	-	-	-	-	-		-	-	-	-	-	-
	MAX	.190	.055	.120†	.040	.070	.024	.650	.361†	.507	.420	.350	.030		.270	.580	.250	.135	.161	

JEDEC Registration TO-220, Variation AB, Issue K, April 2002.

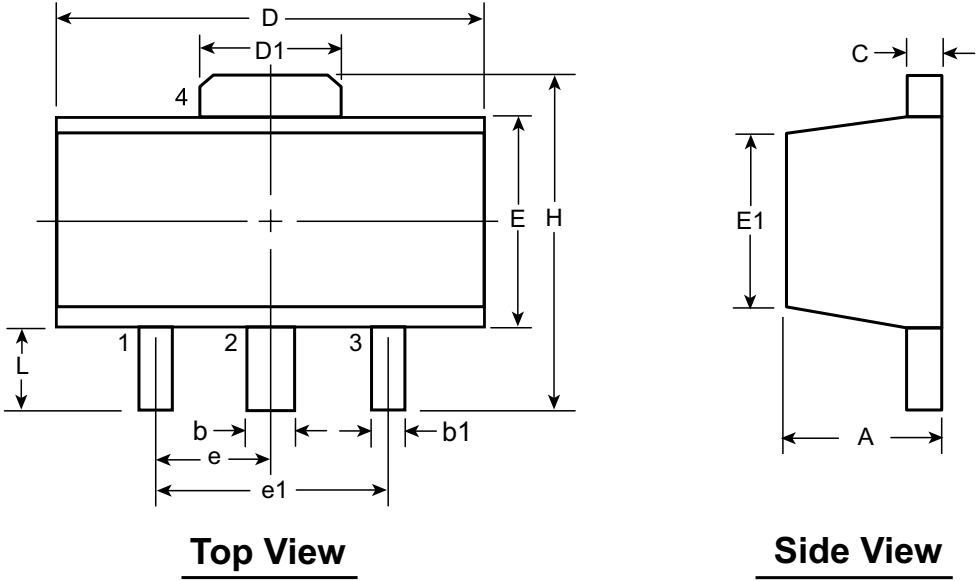
* This dimension is not specified in the JEDEC drawing.

† This dimension differs from the JEDEC drawing.

Drawings not to scale.

Supertex Doc. #: DSPD-3TO220N5, Version C041009.

3-Lead TO-243AA (SOT-89) Package Outline (N8)



Symbol		A	b	b1	C	D	D1	E	E1	e	e1	H	L	
Dimensions (mm)	MIN	1.40	0.44	0.36	0.35	4.40	1.62	2.29	2.00†	1.50 BSC	3.00 BSC	3.94	0.89	
	NOM	-	-	-	-	-	-	-	-			-	-	-
	MAX	1.60	0.56	0.48	0.44	4.60	1.83	2.60	2.29			4.25	1.20	

JEDEC Registration TO-243, Variation AA, Issue C, July 1986.

† This dimension differs from the JEDEC drawing

Drawings not to scale.

Supertex Doc. #: DSPD-3TO243AAN8, Version E051509.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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