16-Channel Unipolar Positive High Voltage Analog Switch

Features

- 16 Channels of unipolar positive analog switch
- 3.3V input logic level compatible
- 5.0µS switching response time
- HVCMOS technology for high performance
- Very low quiescent power dissipation: 10µA
- DC to 50MHz small signal frequency response
- -50dB typical off-isolation at 5.0MHz
- CMOS logic circuitry for low power
- Excellent noise immunity
- Flexible operating supply voltages

Applications

- Medical ultrasound probe select switch
- Piezoelectric transducer switching
- High voltage actuator control interface
- Optical MEMs modules

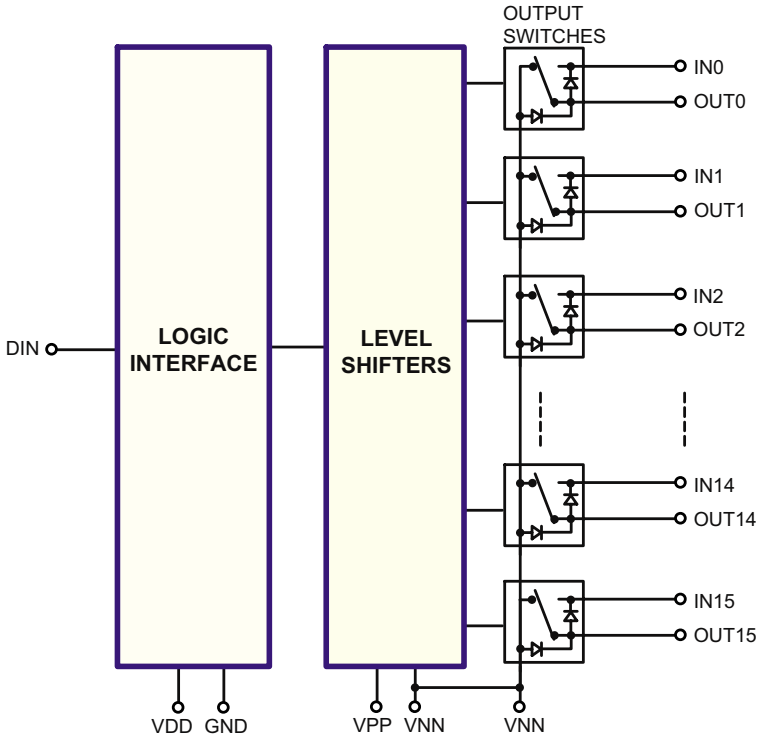
General Description

The Supertex HV2612 is a 16-channel, unipolar, positive voltage analog switch integrated circuit (IC). It is intended for use in applications that require high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging, piezoelectric transducer drivers, and MEMS devices.

The low voltage to high voltage level-shifter directly couples the input control signal to an array of sixteen N-MOSFET output switches simultaneously. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The HV2612 is suitable for positive voltage supplies from +100 to +140V; negative voltage supplies from 0 to -10V; and logic voltage ranges of +3.0 to +5.0V. The device is in a 48-lead LQFP package.

Block Diagram

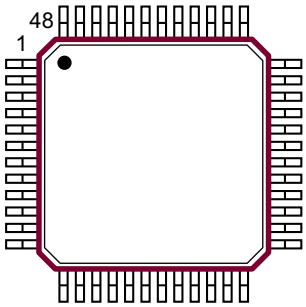


Ordering Information

Device	Package Option
	48-Lead LQFP *7.00x7.00mm body* *1.6mm height (max)* *0.50mm pitch*
HV2612	HV2612FG-G

-G indicates package is RoHS compliant ('Green')

Pin Configuration



48-Lead LQFP (FG)
(top view)

Product Marking

Top Marking

Bottom Marking

YY = Year Sealed
WW = Week Sealed
L = Lot Number
C = Country of Origin*
A = Assembler ID*
_____ = "Green" Packaging

**May be part of top marking*

Package may or may not include the following marks: Si or

48-Lead LQFP (FG)

Absolute Maximum Ratings

Parameter	Value
V_{DD} logic supply	-0.5V to +7.0V
V_{PP} - V_{NN} differential supply	160V
V_{PP} positive supply	-0.5V to V_{NN} +160V
V_{NN} negative supply	+0.5V to -12V
Logic input voltage	-0.5V to V_{DD} +0.3V
$V_{IN(0-15)}$ and $V_{OUT(0-15)}$ signal pin	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Operation Conditions

Symbol	Parameter	Value
V_{DD}	Logic power supply voltage	+3.0V to +5.5V
V_{PP}	Positive high voltage supply	+100V to +140V
V_{NN}	Negative high voltage supply	0V to -10V
V_{IH}	High level input voltage	0.9V_{DD} to V_{DD}
V_{IL}	Low level input voltage	0V to 0.1V_{DD}
$V_{IN(0-15)}$	Analog signal voltage peak-to-peak	V_{NN} +10V to V_{PP} -10V
T_A	Operating free air temperature	0°C to 70°C

Notes:

1. *Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.*
2. *$V_{IN(X)}$ and $V_{OUT(X)}$ must be within V_{NN} and V_{PP} or floating during power up/down transition.*
3. *Rise and fall times of power supplies V_{DD}, V_{NN}, and V_{PP} should not be less than 1.0msec.*

DC Electrical Characteristics

(Over normal operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R_{ONS1}	Small signal switch on-resistance input to output	-	-	-	8.0	-	-	-	Ω	I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = 0V
		-	-	-	8.5	10	-	-		I_{SIG} = 200mA	
		-	-	-	7.5	-	-	-		I_{SIG} = 5.0mA	V_{PP} = +140V, V_{NN} = -10V
		-	-	-	8.0	-	-	-		I_{SIG} = 200mA	
R_{ONS1}	Small signal switch on-resistance output to V_{NN}	-	-	-	31	-	-	-	Ω	I_{SIG} = 5.0mA	V_{PP} = +100V, V_{NN} = 0V
		-	-	-	41	-	-	-		I_{SIG} = 200mA	
		-	-	-	27	-	-	-		I_{SIG} = 5.0mA	V_{PP} = +140V, V_{NN} = -10V
		-	-	-	33	-	-	-		I_{SIG} = 200mA	
ΔR_{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I_{SIG} = 5.0mA, V_{PP} = +100V, V_{NN} = 0V	
I_{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	µA	V_{SIG} = V_{PP} -10V	
I_{PPQ}	Quiescent V_{PP} supply current	-	-	-	10	50	-	-	µA	All switches off	
		-	-	-	10	50	-	-		All switches on, I_{SW} = 5.0mA	
I_{NNQ}	Quiescent V_{NN} supply current	-	-	-	-8.0	-30	-	-	µA	All switches off	
		-	-	-	-8.0	-30	-	-		All switches on, I_{SW} = 5.0mA	
I_{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V_{SIG} duty cycle < 0.1%	
f_{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I_{PP}	Average V_{PP} supply current	-	1.5	-	-	1.5	-	1.6	mA	V_{PP} = +100V, V_{NN} = 0V	All output switches are turning On and Off at 50KHz with no load.
		-	2.5	-	-	2.5	-	2.6		V_{PP} = +140V, V_{NN} = -10V	
I_{NN}	Average V_{NN} supply current	-	1.5	-	-	1.5	-	1.6		V_{PP} = +100V, V_{NN} = 0V	
		-	2.5	-	-	2.5	-	2.6		V_{PP} = +140V, V_{NN} = -10V	
I_{DD}	Average V_{DD} supply current	-	1.0	-	-	1.0	-	1.1	mA	f_{DIN} = 50KHz, V_{DD} = 3.0V	
		-	1.2	-	-	1.2	-	1.3		f_{DIN} = 50KHz, V_{DD} = 5.0V	
I_{DDQ}	Quiescent V_{DD} supply current	-	10	-	-	10	-	10	µA	All logic inputs are static.	
C_{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

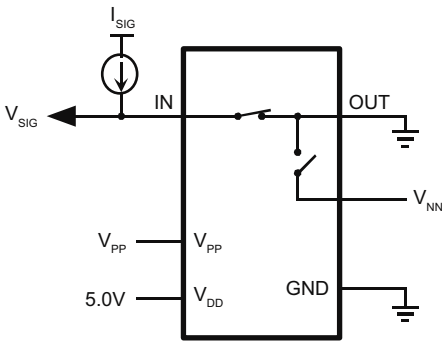
(over recommended operating conditions, V_{DD} = 3.0V, DIN $t_R = t_F \geq$ 5ns, 50% duty cycle, unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
f_{DIN}	D_{IN} frequency	-	50	-	-	50	-	50	KHz	V_{DD}= 3.0 - 5.0V
T_R,T_F	D_{IN} rise and fall times	-	30	-	-	30	-	30	ns	Must be faster than 30ns
T_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	µs	$V_{SIG} = V_{PP}$ R_{LOAD} = 1.0KΩ
T_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0		
dv/dt	Maximum V_{SIG} slew rate	-	20	-	-	20	-	20	v/ns	V_{PP} = +100V
		-	20	-	-	20	-	20		V_{PP} = +140V
K_O	Off isolation	-48	-	-48	-55	-	-48	-	dB	f = 5.0MHz, 50Ω load
K_{CR}	Switch crosstalk	-60	-	-60	-60	-	-60	-	dB	f = 5.0MHz, 50Ω load
I_{ID}	Output switch isolation diode current	-	1.0	-	-	1.0	-	1.0	A	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance IN_X to GND	-	24	-	-	24	-	24	pF	0V, f = 1.0MHz
$C_{SG(ON)}$	On capacitance IN_X to GND	-	36	-	-	36	-	36		

Truth Table

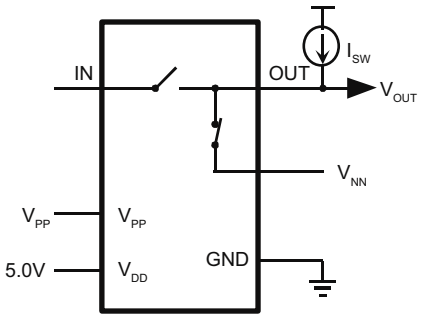
DIN	OUT0	OUT1	...	OUT7	OUT8	...	OUT15
L	All Switches from OUT(0-15) to IN(0-15) are OFF						
	All Switches from OUT(0-15) to VNN are ON						
H	All Switches from OUT(0-15) to IN(0-15) are ON						
	All Switches from OUT(0-15) to VNN are OFF						

Test Circuits



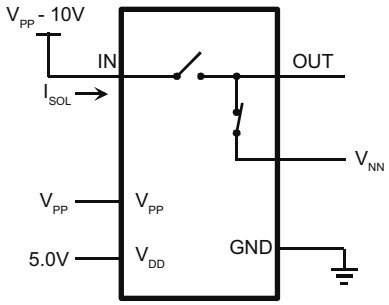
$$R_{SW} = \frac{V_{SIG}}{I_{SIG}}$$

Input to Output
Switch Resistance

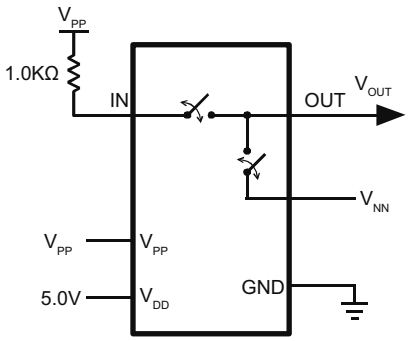


$$R_{SW\text{-}GND} = \frac{V_{OUT}}{I_{SW}}$$

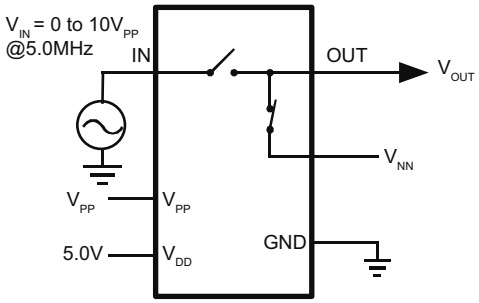
Output to V_{NN}
Switch Resistance



Input Switch Off
Leakage Current

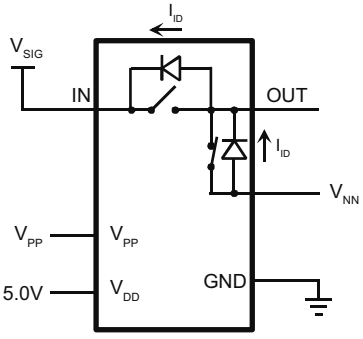


Switch T_{ON} and T_{OFF}

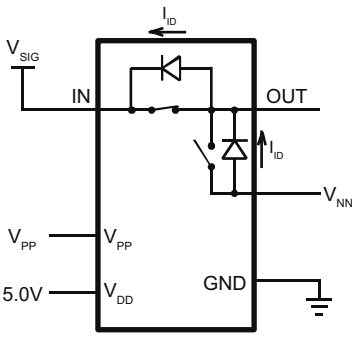


$$KO = 20Log \frac{V_{OUT}}{V_{IN}}$$

Switch Off Isolation



Isolation Diode Current



Isolation Diode Current

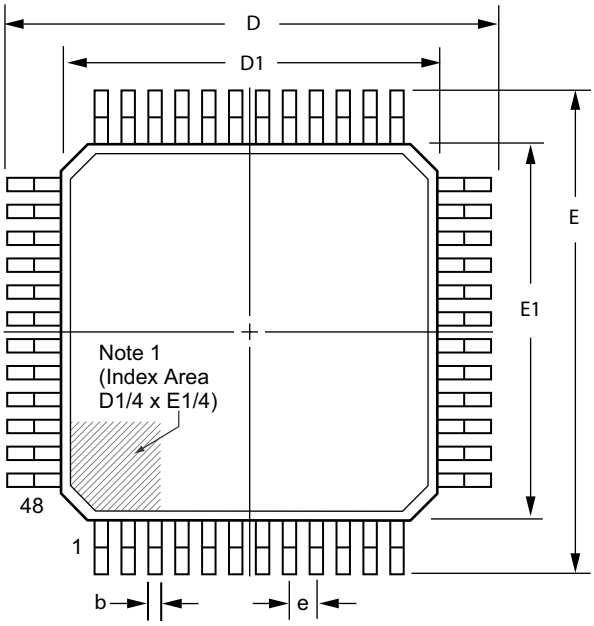
Pin Configuration (48-Lead LQFP)

Pin #	Function	Pin #	Function	Pin #	Function	Pin #	Function
1	VNN	13	VNN	25	OUT15	37	OUT10
2	VNN	14	NC	26	IN15	38	IN10
3	OUT4	15	VPP	27	OUT14	39	OUT9
4	IN4	16	NC	28	IN14	40	IN9
5	OUT3	17	GND	29	OUT13	41	OUT8
6	IN3	18	VDD	30	IN13	42	IN8
7	OUT2	19	DIN	31	OUT12	43	OUT7
8	IN2	20	NC	32	IN12	44	IN7
9	OUT1	21	NC	33	OUT11	45	OUT6
10	IN1	22	NC	34	IN11	46	IN6
11	OUT0	23	VNN	35	VNN	47	OUT5
12	IN0	24	VNN	36	VNN	48	IN5

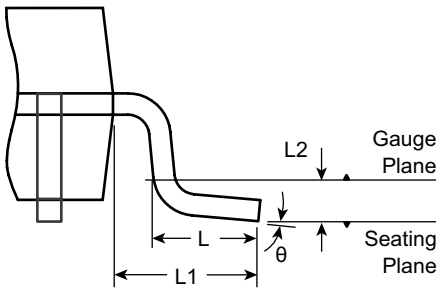
NC = No Internal Connection.

48-Lead LQFP Package Outline (FG)

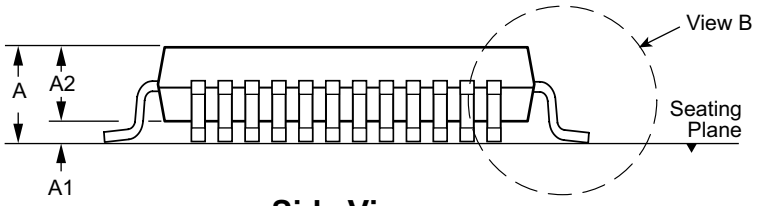
7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



Top View



View B



Side View

Note:

1. *A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.*

Symbol		A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	θ
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60			3.5°
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75			7°

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.
** This dimension is not specified in the JEDEC drawing.*

Drawings are not to scale.

Supertex Doc. #: *DSPD-48LQFPFG Version, D041309.*

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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