

## Low Charge Injection 16-Channel High Voltage Analog Switch

### Features

- ▶ HVCMOS technology for high performance
- ▶ 16-channel high voltage analog switch
- ▶ 3.3V input logic level compatible
- ▶ 20MHz data shift clock frequency
- ▶ Very low quiescent power dissipation (-10µA)
- ▶ Low parasitic capacitance
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical OFF-isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ Cascadable serial data register with latches
- ▶ Flexible operating supply voltages

### Applications

- ▶ Medical ultrasound imaging
- ▶ NDT metal flaw detection
- ▶ Piezoelectric transducer drivers
- ▶ Optical MEMS modules

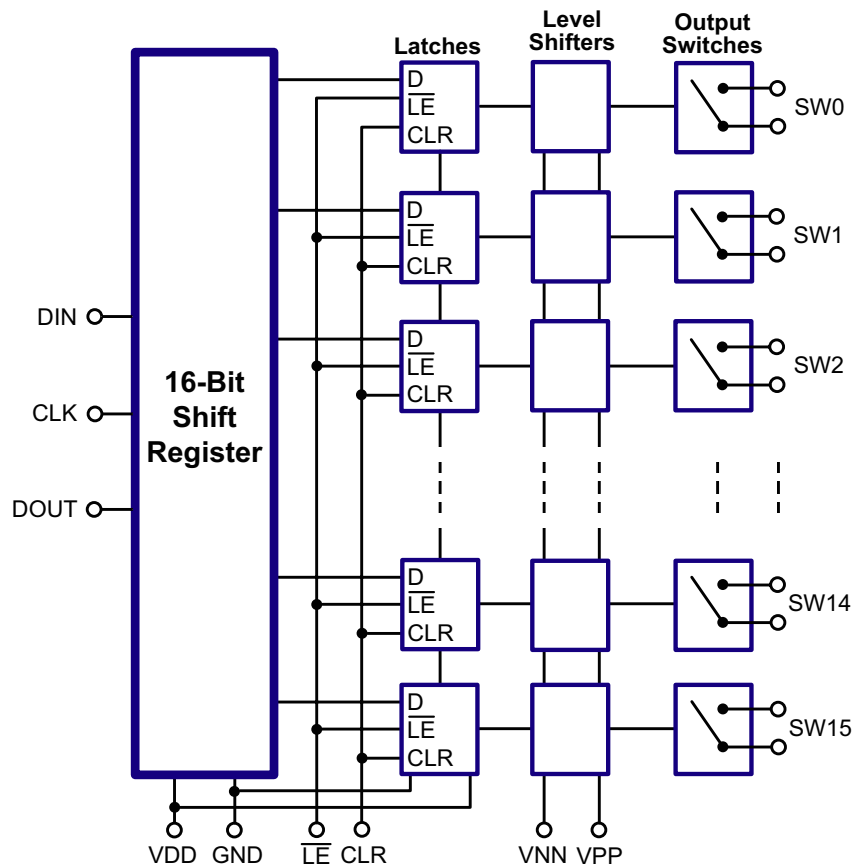
### General Description

The Supertex HV2601 is a low charge injection 16-channel high voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as medical ultrasound imaging and other piezoelectric transducer drivers.

Input data are shifted into a 16-bit shift register that can then be retained in a 16-bit latch. To reduce any possible clock feed-through noise, the latch enable bar should be left high until all bits are clocked in. Data are clocked in during the rising edge of the clock. Using HVCMOS technology, this device combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

The device is suitable for various combinations of high voltage supplies, e.g.,  $V_{PP}/V_{NN}$ : +40V/-160V, +100V/-100V, and +160V/-40V.

### Block Diagram



## Ordering Information

Device	Package Options		
	42-Ball Bumped Die 5.29x5.30mm body 1.01mm height (max) 0.52 / 0.60mm pitch	48-Lead LQFP 7.00x7.00mm body 1.60mm height (max) 0.50mm pitch	48-Ball fpBGA 7.00x8.00mm body 1.16mm height (max) 0.75mm pitch
HV2601	HV2601BD M936	HV2601FG-G	HV2601GA-G

-G indicates package is RoHS compliant ('Green').  
Bumped Die package is RoHS compliant ('Green').  
M936 specifies product in tape and reel.

## Absolute Maximum Ratings

Parameter	Value
V <sub>DD</sub> logic supply	-0.5V to +7.0V
V <sub>PP</sub> - V <sub>NN</sub> differential supply	220V
V <sub>PP</sub> positive supply	-0.5V to V <sub>NN</sub> +200V
V <sub>NN</sub> negative supply	+0.5V to -200V
Logic input voltage	-0.5V to V <sub>DD</sub> +0.3V
Analog signal range	V <sub>NN</sub> to V <sub>PP</sub>
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to 150°C
Power dissipation:	
42-Ball Bumped Die (BD)	1.5W
48-Lead LQFP (FG)	1.0W
48-Ball fpBGA (GA)	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

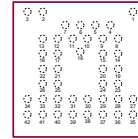
## Recommended Operating Conditions

Sym	Parameter	Value
V <sub>DD</sub>	Logic power supply voltage	3.0V to 5.5V
V <sub>PP</sub>	Positive high voltage supply	+40V to V <sub>NN</sub> +200V
V <sub>NN</sub>	Negative high voltage supply	-40V to -160V
V <sub>IH</sub>	High level input voltage	0.9V <sub>DD</sub> to V <sub>DD</sub>
V <sub>IL</sub>	Low level input voltage	0V to 0.1V <sub>DD</sub>
V <sub>SIG</sub>	Analog signal voltage peak-to-peak	V <sub>NN</sub> +10V to V <sub>PP</sub> -10V
T <sub>A</sub>	Operating free air temperature	0°C to 70°C

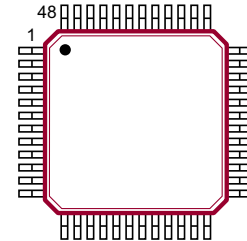
### Notes:

- Power up/down sequence is arbitrary except GND must be powered-up first and powered-down last.
- V<sub>SIG</sub> must be within V<sub>NN</sub> and V<sub>PP</sub> or floating during power up/down transition.
- Rise and fall times of power supplies V<sub>DD</sub>, V<sub>PP</sub> and V<sub>NN</sub> should not be less than 1.0msec.

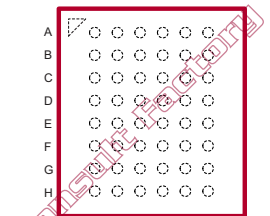
## Pin Configurations



42-Ball Bumped Die (BD)  
(top view)

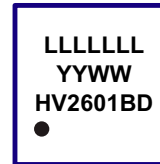


48-Lead LQFP (FG)  
(top view)



48-Ball fpBGA (GA)  
(top view)

## Product Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number

Package may or may not include the following marks: Si or

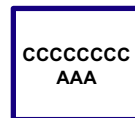
### 42-Ball Bumped Die (BD)

#### Top Marking



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number

#### Bottom Marking



C = Country of Origin\*  
A = Assembler ID\*  
\_\_\_\_ = "Green" Packaging

\*May be part of top marking

Package may or may not include the following marks: Si or

### 48-Lead LQFP (FG)



YY = Year Sealed  
WW = Week Sealed  
L = Lot Number  
\_\_\_\_ = "Green" Packaging

### 48-Ball fpBGA (GA)

Packages may or may not include the following marks: Si or

## DC Electrical Characteristics

(over recommended operating conditions unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R <sub>ONS</sub>	Small signal switch ON-resistance	-	30	-	26	38	-	48	Ω	I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +40V
		-	25	-	22	27	-	32		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -160V
		-	25	-	22	27	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +100V
		-	18	-	18	24	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -100V
		-	23	-	20	25	-	30		I <sub>SIG</sub> = 5.0mA	V <sub>PP</sub> = +160V
		-	22	-	16	25	-	27		I <sub>SIG</sub> = 200mA	V <sub>NN</sub> = -40V
ΔR <sub>ONS</sub>	Small signal switch ON-resistance matching	-	20	-	5.0	20	-	20	%	I <sub>SIG</sub> = 5.0mA, V <sub>PP</sub> = +100V, V <sub>NN</sub> = -100V	
R <sub>ONL</sub>	Large signal switch ON-resistance	-	-	-	15	-	-	-	Ω	V <sub>SIG</sub> = V <sub>PP</sub> - 10V, I <sub>SIG</sub> = 1.0A	
I <sub>SOL</sub>	Switch OFF leakage per switch*	-	5.0	-	1.0	10	-	15	μA	V <sub>SIG</sub> = V <sub>PP</sub> - 10V and V <sub>NN</sub> + 10V	
V <sub>OS</sub>	DC offset switch OFF*	-	300	-	100	300	-	300	mV	100kΩ load	
	DC offset switch ON*	-	500	-	100	500	-	500	mV		
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches OFF	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches OFF	
I <sub>PPQ</sub>	Quiescent V <sub>PP</sub> supply current	-	-	-	10	50	-	-	μA	All switches ON, I <sub>SW</sub> = 5.0mA	
I <sub>NNQ</sub>	Quiescent V <sub>NN</sub> supply current	-	-	-	-10	-50	-	-	μA	All switches ON, I <sub>SW</sub> = 5.0mA	
I <sub>SW</sub>	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V <sub>SIG</sub> duty cycle < 0.1%	
f <sub>SW</sub>	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I <sub>PP</sub>	Average V <sub>PP</sub> supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +40V	All output switches are turning ON and OFF at 50kHz with no load.
		-	4.0	-	-	5.5	-	5.5		V <sub>NN</sub> = -160V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
I <sub>NN</sub>	Average V <sub>NN</sub> supply current	-	6.5	-	-	7.0	-	8.0	mA	V <sub>PP</sub> = +160V	All output switches are turning ON and OFF at 50kHz with no load.
		-	4.0	-	-	5.0	-	5.5		V <sub>NN</sub> = -40V	
		-	4.0	-	-	5.0	-	5.5		V <sub>PP</sub> = +100V V <sub>NN</sub> = -100V	
I <sub>DD</sub>	Average V <sub>DD</sub> supply current	-	4.0	-	-	4.0	-	4.0	mA	f <sub>CLK</sub> = 5.0MHz, V <sub>DD</sub> = 5.0V	
I <sub>DDQ</sub>	Quiescent V <sub>DD</sub> supply current	-	10	-	-	10	-	10	μA	All logic inputs are static	
I <sub>SOR</sub>	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = V <sub>DD</sub> - 0.7V	
I <sub>SINK</sub>	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V <sub>OUT</sub> = 0.7V	
C <sub>IN</sub>	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

\* See Test Circuits on page 5

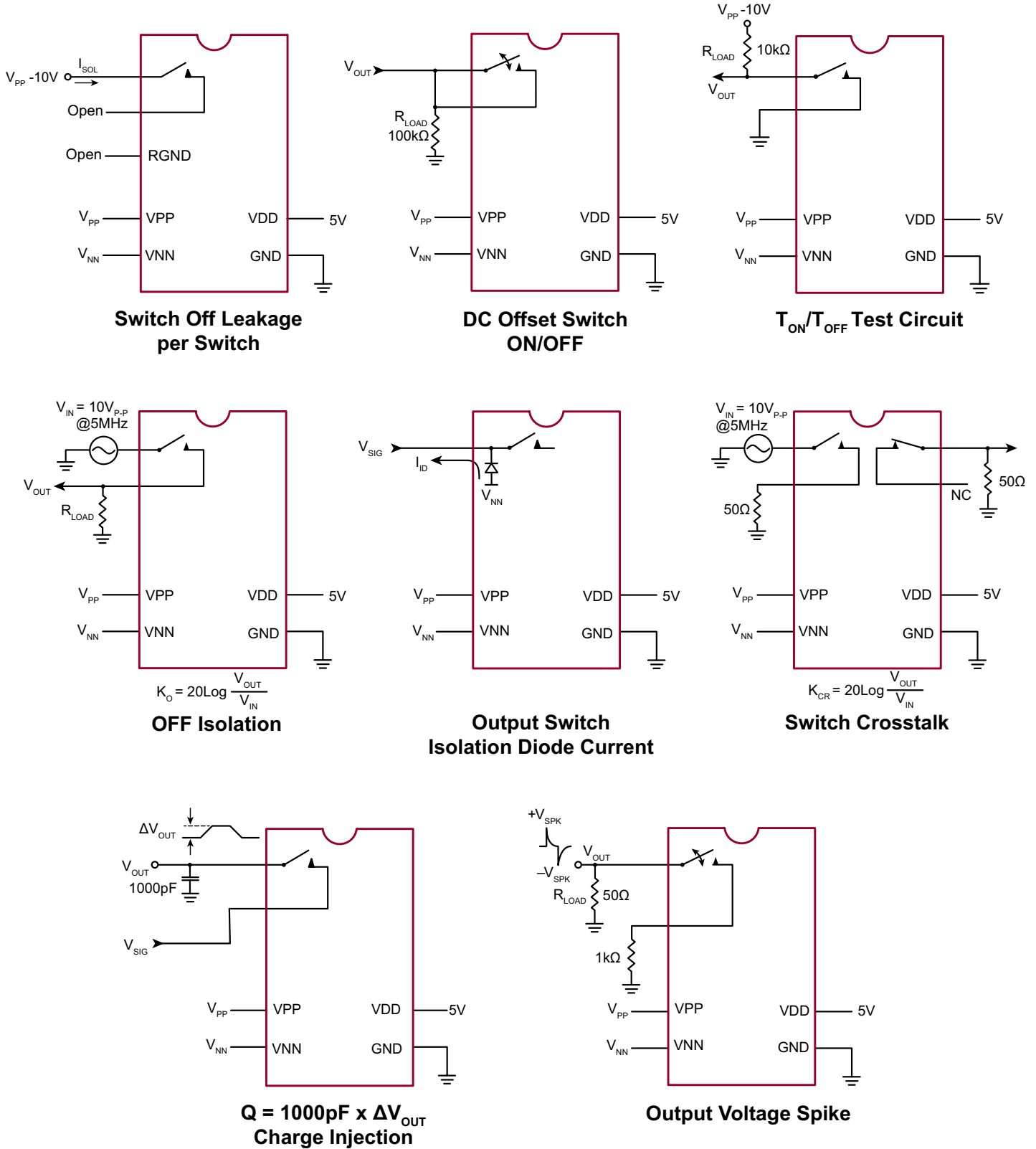
## AC Electrical Characteristics

(over recommended operating conditions,  $V_{DD} = 5.0V$ ,  $t_R = t_F \leq 5ns$ , 50% duty cycle,  $C_{LOAD} = 20pF$  unless otherwise noted)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
$t_{SD}$	Set up time before $\overline{LE}$ rises	25	-	25	-	-	25	-	ns	---
$t_{WLE}$	Time width of $\overline{LE}$	56	-	-	56	-	56	-	ns	$V_{DD} = 3.0V$
		12	-	-	12	-	12	-		$V_{DD} = 5.0V$
$t_{DO}$	Clock delay time to data out	50	100	50	78	100	50	100	ns	$V_{DD} = 3.0V$
		15	40	15	30	40	15	40		$V_{DD} = 5.0V$
$t_{WCLR}$	Time width of CLR	55	-	55	-	-	55	-	ns	---
$t_{SU}$	Set up time data to clock	21	-	-	21	-	21	-	ns	$V_{DD} = 3.0V$
		7	-	-	7	-	7	-		$V_{DD} = 5.0V$
$t_H$	Hold time data from clock	2	-	2	-	-	2	-	ns	$V_{DD} = 3.0$ or $5.0V$
$f_{CLK}$	Clock frequency	-	8	-	-	8	-	8	MHz	$V_{DD} = 3.0V$
		-	20	-	-	20	-	20		$V_{DD} = 5.0V$
$t_R, t_F$	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
$T_{ON}$	Turn ON time*	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10k\Omega$
$T_{OFF}$	Turn OFF time*	-	5.0	-	-	5.0	-	5.0	$\mu s$	$V_{SIG} = V_{PP} - 10V$ , $R_{LOAD} = 10k\Omega$
dv/dt	Maximum $V_{SIG}$ slew rate	-	20	-	-	20	-	20	v/ns	$V_{PP} = +40V$ , $V_{NN} = -160V$
		-	20	-	-	20	-	20		$V_{PP} = +100V$ , $V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +160V$ , $V_{NN} = -40V$
$K_O$	OFF isolation*	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz$ , $1k\Omega//15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz$ , $50\Omega$ load
$K_{CR}$	Switch crosstalk*	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz$ , $50\Omega$ load
$I_{ID}$	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	OFF capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	ON capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike*	-	-	-	-	150	-	-	mV	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $R_{LOAD} = 50\Omega$
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		
$-V_{SPK}$		-	-	-	-	150	-	-		
QC	Charge injection*	-	-	-	820	-	-	-	pC	$V_{PP} = +40V$ , $V_{NN} = -160V$ , $V_{SIG} = 0V$
		-	-	-	600	-	-	-		$V_{PP} = +100V$ , $V_{NN} = -100V$ , $V_{SIG} = 0V$
		-	-	-	350	-	-	-		$V_{PP} = +160V$ , $V_{NN} = -40V$ , $V_{SIG} = 0V$

\* See Test Circuits on page 5

Test Circuits



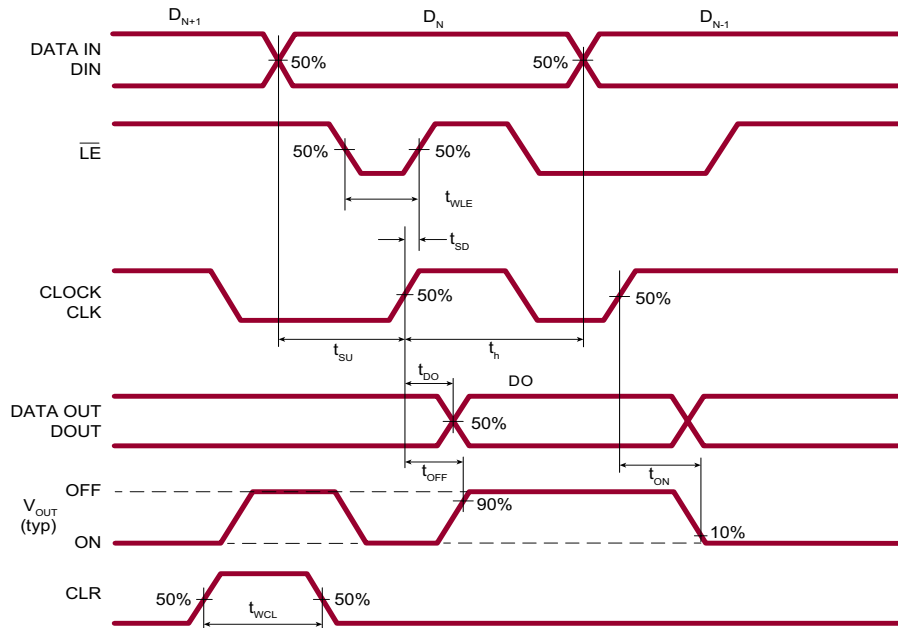
Logic Function Table

D0	D1	...	D7	D8	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW7	SW8	...	SW15
L	-		-	-		-	L	L	OFF	-		-	-		-
H	-		-	-		-	L	L	ON	-		-	-		-
-	L		-	-		-	L	L	-	OFF		-	-		-
-	H		-	-		-	L	L	-	ON		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		OFF	-		-
-	-		L	-		-	L	L	-	-		ON	-		-
-	-		H	-		-	L	L	-	-		-	OFF		-
-	-	...	-	L	...	-	L	L	-	-	...	-	ON	...	-
-	-		-	H		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		-	L	L	-	-		-	-		-
-	-		-	-		L	L	L	-	-		-	-		OFF
-	-		-	-		H	L	L	-	-		-	-		ON
X	X	X	X	X	X	X	H	L	HOLD PREVIOUS STATE						
X	X	X	X	X	X	X	X	H	ALL SWITCHES OFF						

Notes:

1. The 16 switches operate independently.
2. Serial data is clocked in on the L to H transition of the CLK.
3. All 16 switches go to a state retaining their latched condition at the rising edge of  $\overline{LE}$ . When  $\overline{LE}$  is low the shift registers data flow through the latch.
4.  $D_{OUT}$  is high when data in the shift register 15 is high.
5. Shift registers clocking has no effect on the switch states if  $\overline{LE}$  is high.
6. The CLR clear input overrides all other inputs.

Logic Timing Waveforms



**Ball Description**  
**42-Ball Bumped Die Package Outline (BD)**

Ball #	Ball Name	Ball Coordinates*	
		X	Y
1	NC	+2100.00	-2239.50
2	VPP	-1500.00	-2239.50
3	VNN	-2100.00	-2239.50
4	DOUT	+1200.00	-1719.75
5	CLR	+600.00	-1719.75
6	CLK	0.00	-1719.75
7	GND	-600.00	-1719.75
8	SW15A	+1500.00	-1200.00
9	SW15B	+900.00	-1200.00
10	$\overline{LE}$	+300.00	-1200.00
11	VDD	-300.00	-1200.00
12	SW0A	-900.00	-1200.00
13	SW0B	-1500.00	-1200.00
14	SW14A	+1500.00	-600.00
15	SW14B	+900.00	-600.00
16	DIN	0.00	-680.25
17	SW1A	-900.00	-600.00
18	SW1B	-1500.00	-600.00
19	SW13A	+1500.00	0.00
20	SW13B	+900.00	0.00
21	SW2A	-900.00	0.00

Ball #	Ball Name	Ball Coordinates*	
		X	Y
22	SW2B	-1500.00	0.00
23	SW12A	+1500.00	+600.00
24	SW12B	+900.00	+600.00
25	SW3A	-900.00	+600.00
26	SW3B	-1500.00	+600.00
27	SW11A	+2100.00	+1200.00
28	SW11B	+1500.00	+1200.00
29	SW9B	+900.00	+1200.00
30	SW8B	+300.00	+1200.00
31	SW7A	-300.00	+1200.00
32	SW6A	-900.00	+1200.00
33	SW4A	-1500.00	+1200.00
34	SW4B	-2100.00	+1200.00
35	SW10B	+2100.00	+1800.00
36	SW10A	+1500.00	+1800.00
37	SW9A	+900.00	+1800.00
38	SW8A	+300.00	+1800.00
39	SW7B	-300.00	+1800.00
40	SW6B	-900.00	+1800.00
41	SW5B	-1500.00	+1800.00
42	SW5A	-2100.00	+1800.00

**Note:**  
\* Referenced from center of package ( $\mu\text{m}$ ).

**Pin Description**  
**48-Lead LQFP (FG)**

Pin #	Function
1	NC
2	NC
3	SW4B
4	SW4A
5	SW3B
6	SW3A
7	SW2B
8	SW2A
9	SW1B
10	SW1A
11	SW0B
12	SW0A

Pin #	Function
13	VNN
14	NC
15	VPP
16	NC
17	GND
18	VDD
19	DIN
20	CLK
21	$\overline{LE}$
22	CLR
23	DOUT
24	NC

Pin #	Function
25	SW15B
26	SW15A
27	SW14B
28	SW14A
29	SW13B
30	SW13A
31	SW12B
32	SW12A
33	SW11B
34	SW11A
35	NC
36	NC

Pin #	Function
37	SW10B
38	SW10A
39	SW9B
40	SW9A
41	SW8B
42	SW8A
43	SW7B
44	SW7A
45	SW6B
46	SW6A
47	SW5B
48	SW5A

**Pin Configuration**  
**48-Ball fpBGA (GA)**

Ball #	Function
A1	SW5A
A2	SW5B
A3	SW7A
A4	SW7B
A5	SW9A
A6	SW9B
B1	SW6A
B2	SW6B
B3	SW8A
B4	SW8B
B5	SW10A
B6	SW10B

Ball #	Function
C1	SW4B
C2	SW3B
C3	SW2B
C4	SW13A
C5	SW12A
C6	SW11A
D1	SW4A
D2	SW3A
D3	SW2A
D4	SW13B
D5	SW12B
D6	SW11B

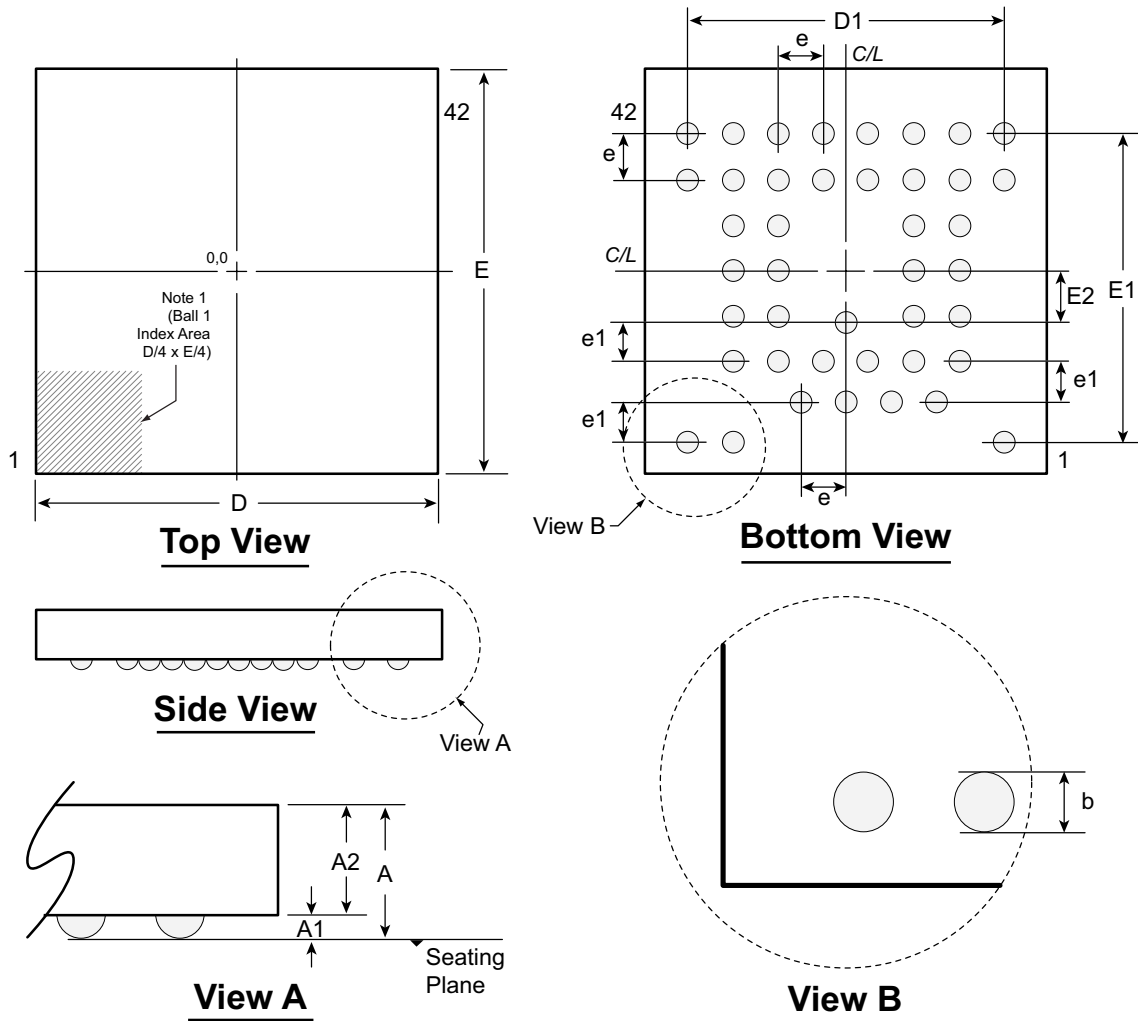
Ball #	Function
E1	SW1B
E2	SW0B
E3	SW15B
E4	SW15A
E5	SW14B
E6	SW14A
F1	SW1A
F2	SW0A
F3	NC
F4	NC
F5	VDD
F6	NC

Ball #	Function
G1	NC
G2	GND
G3	NC
G4	DIN
G5	CLK
G6	DOUT
H1	VNN
H2	NC
H3	VPP
H4	NC
H5	$\overline{LE}$
H6	CLR

NC = No Internal Connection

# 42-Ball Bumped Die Package Outline (BD)

5.29x5.30mm body, 1.01mm height (max), 0.52 / 0.60mm pitch



**Notes:**

- Ball 1 identifier must be located in the index area indicated. Ball 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

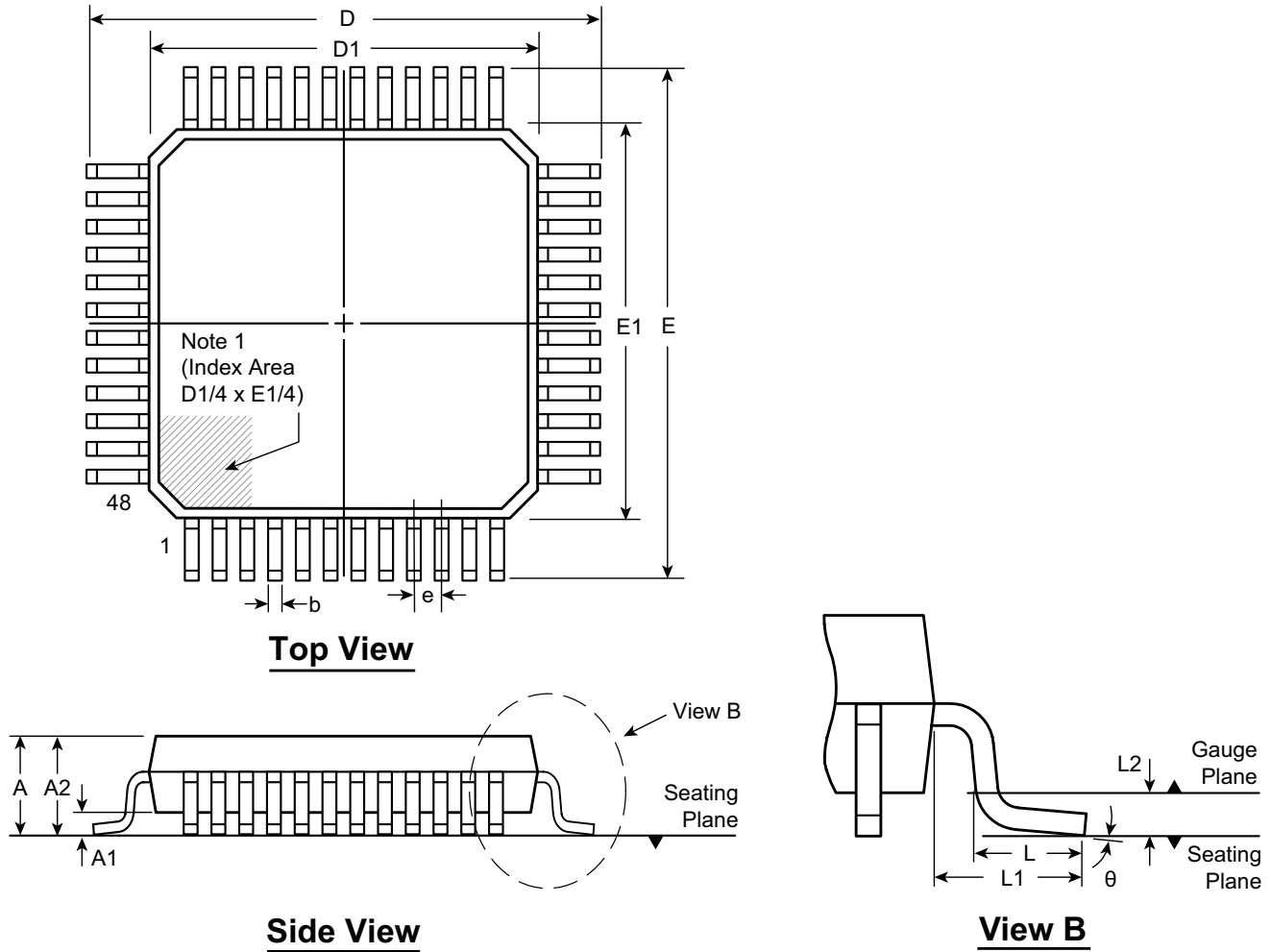
Symbol		A	A1	A2	b	D	D1	E	E1	E2	e	e1
Dimension (mm)	MIN	0.89	0.21	0.68	0.29	5.19	4.20 BSC	5.20	4.04 BSC	0.68 BSC	0.60 BSC	0.52 BSC
	NOM	0.95	0.24	0.71	0.32	5.29		5.30				
	MAX	1.01	0.27	0.74	0.35	5.39		5.40				

Drawings not to scale.

Supertex Doc. #: DSPD-42BumpedDieBD, Version A030211.

# 48-Lead LQFP Package Outline (FG)

7.00x7.00mm body, 1.60mm height (max), 0.50mm pitch



**Note:**  
1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	D1	E	E1	e	L	L1	L2	$\theta$	
Dimension (mm)	MIN	1.40*	0.05	1.35	0.17	8.80*	6.80*	8.80*	6.80*	0.50 BSC	0.45	1.00 REF	0.25 BSC	0°
	NOM	-	-	1.40	0.22	9.00	7.00	9.00	7.00		0.60		3.5°	
	MAX	1.60	0.15	1.45	0.27	9.20*	7.20*	9.20*	7.20*		0.75		7°	

JEDEC Registration MS-026, Variation BBC, Issue D, Jan. 2001.

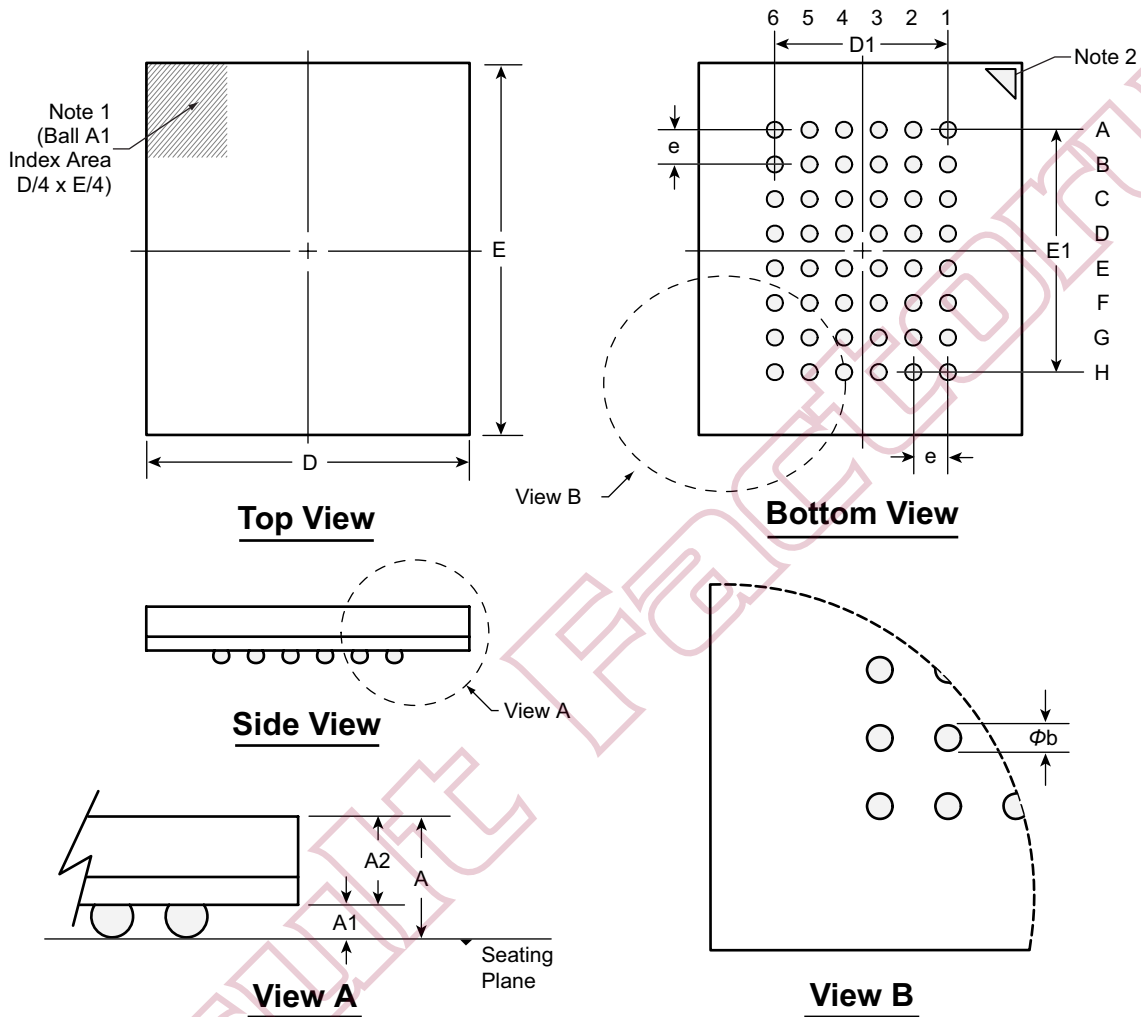
\* This dimension is not specified in the JEDEC drawing.

**Drawings are not to scale.**

**Supertex Doc. #: DSPD-48LQFPFG Version, D041309.**

# 48-Ball fpBGA Package Outline (GA)

7.00x8.00mm body, 1.16mm height (max), 0.75mm pitch



**Notes:**

- Ball A1 identifier must be located in the index area indicated. Ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
- Corner A1 identifier (actual shape may vary).

Symbol		A	A1	A2	b	D	D1	E	E1	e
Dimension (mm)	MIN	0.86	0.18	0.68	0.25	6.90	3.75 BSC	7.90	5.25 BSC	0.75 BSC
	NOM	1.01	0.23	0.78	0.30	7.00		8.00		
	MAX	1.16	0.28	0.88	0.35	7.10		8.10		

Drawings not to scale.

Supertex Doc. #: DSPD-48fpBGAGA, Version C020309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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