

Low Charge Injection 8-Channel High Voltage Analog Switch

Features

- ▶ HVCMOS® technology for high performance
- ▶ Very low quiescent power dissipation (-10µA)
- ▶ Output on-resistance typically 22Ω
- ▶ Low parasitic capacitances
- ▶ DC to 50MHz small signal frequency response
- ▶ -60dB typical output off isolation at 5.0MHz
- ▶ CMOS logic circuitry for low power
- ▶ Excellent noise immunity
- ▶ On-chip shift register, latch and clear logic circuitry
- ▶ Flexible high voltage supplies

Applications

- ▶ Medical ultrasound imaging
- ▶ Piezoelectric transducer drivers

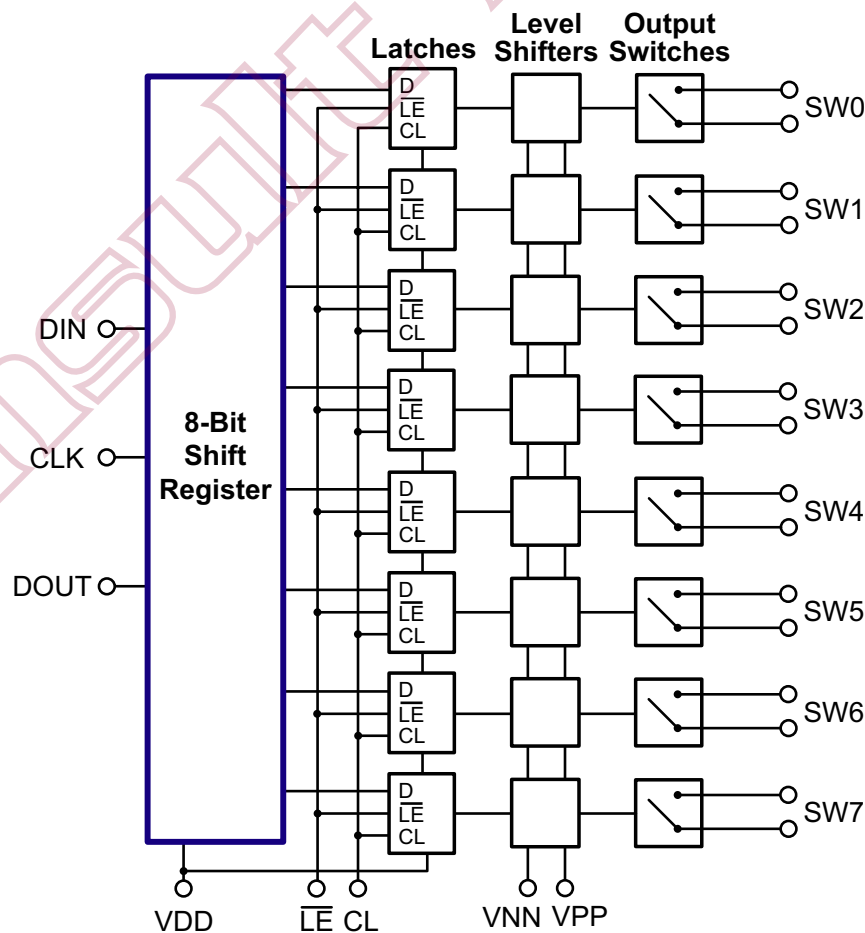
General Description

This device is a low charge injection, 8-channel, high-voltage analog switch integrated circuit (IC) intended for use in applications requiring high voltage switching controlled by low voltage control signals, such as ultrasound imaging and printers.

Input data is shifted into an 8-bit shift register which can then be retained in an 8-bit latch. To reduce any possible clock feed-through noise, Latch Enable Bar (\overline{LE}) should be left high until all bits are clocked in. Using HVCMOS® technology, this switch combines high voltage bilateral DMOS switches and low power CMOS logic to provide efficient control of high voltage analog signals.

These ICs are suitable for various combinations of high voltage supplies, e.g., V_{PP}/V_{NN} : +50V/-150V, or +100V/-100V.

Block Diagram



Ordering Information

Device	Package Option
	25-Ball fpBGA 5.70x5.00mm body 1.20mm height (max) 0.75mm pitch
HV220	HV220GA-G

-G indicates the part is RoHS compliant ('Green')

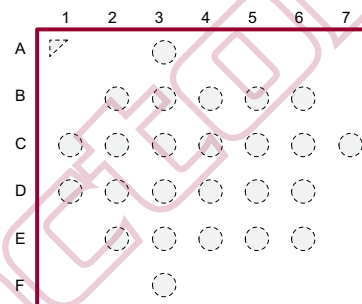


Absolute Maximum Ratings

Parameter	Value
V_{DD} logic power supply voltage	-0.5V to +15V
$V_{PP} - V_{NN}$ supply voltage	220V
V_{PP} positive high voltage supply	-0.5V to $V_{NN} + 200V$
V_{NN} negative high voltage supply	+0.5V to -200V
Logic input voltages	-0.5V to $V_{DD} + 0.3V$
Analog signal range	V_{NN} to V_{PP}
Peak analog signal current/channel	3.0A
Storage temperature	-65°C to +150°C
Power dissipation	1.0W

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



25-Ball fpBGA (GA)
(top view)

Product Marking



YY = Year Sealed
 WW = Week Sealed
 L = Lot Number
 = "Green" Packaging

Package may or may not include the following marks: Si or

25-Ball fpBGA (GA)

Operating Conditions

Sym	Parameter	Value
V_{DD}	Logic power supply voltage ^{1,3}	4.5 to 13.2V
V_{PP}	Positive high voltage supply ^{1,3}	40 to $V_{NN} + 200V$
V_{NN}	Negative high voltage supply ^{1,3}	-40 to -160V
V_{IH}	High level input voltage	$V_{DD} - 1.5V$ to V_{DD}
V_{IL}	Low-level input voltage	0 to 1.5V
V_{SIG}	Analog signal voltage peak-to-peak	$V_{NN} + 10V$ to $V_{PP} - 10V$ ²
T_A	Operating free air temperature	0°C to 70°C

Notes:

- Power up/down sequence is arbitrary except GND must be powered -up first and powered down last.
- V_{SIG} must be $V_{NN} \leq V_{SIG} \leq V_{PP}$ or floating during power up/down transition.
- Rise and fall times of power supplies V_{DD} , V_{PP} and V_{NN} should not be less than 1.0msec.

DC Electrical Characteristics

(Over operating conditions unless otherwise specified)

Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions	
		Min	Max	Min	Typ	Max	Min	Max			
R _{ONS}	Small signal switch on-resistance	-	30	-	26	38	-	48	Ω	I _{SIG} = 5.0mA	V _{PP} = +40V
		-	25	-	22	27	-	32		I _{SIG} = 200mA	V _{NN} = -160V
		-	25	-	22	27	-	30		I _{SIG} = 5.0mA	V _{PP} = +100V
		-	18	-	18	24	-	27		I _{SIG} = 200mA	V _{NN} = -100V
		-	23	-	20	25	-	30		I _{SIG} = 5.0mA	V _{PP} = +160V
		-	22	-	16	25	-	27		I _{SIG} = 200mA	V _{NN} = -40V
ΔR _{ONS}	Small signal switch on-resistance matching	-	20	-	5.0	20	-	20	%	I _{SIG} = 5.0mA, V _{PP} = +100V, V _{NN} = -100V	
R _{ONL}	Large signal switch on-resistance	-	-	-	15	-	-	-	Ω	V _{SIG} = V _{PP} -10V, I _{SIG} = 1.0A	
I _{SOL}	Switch off leakage per switch	-	5.0	-	1.0	10	-	15	μA	V _{SIG} = V _{PP} -10V, V _{NN} +10V	
V _{OS}	DC offset switch off	-	300	-	100	300	-	300	mV	R _L = 100kΩ	
	DC offset switch on	-	500	-	100	500	-	500	mV	R _L = 100kΩ	
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches off	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-	μA	All switches off	
I _{PPQ}	Quiescent V _{PP} supply current	-	-	-	10	50	-	-	μA	All switches on, I _{SW} = 5.0mA	
I _{NNQ}	Quiescent V _{NN} supply current	-	-	-	-10	-50	-	-	μA	All switches on, I _{SW} = 5.0mA	
I _{SW}	Switch output peak current	-	3.0	-	3.0	2.0	-	2.0	A	V _{SIG} duty cycle < 0.1%	
f _{SW}	Output switching frequency	-	-	-	-	50	-	-	kHz	Duty cycle = 50%	
I _{PP}	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V _{PP} = +40V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V _{NN} = -160V	
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +100V V _{NN} = -100V	
I _{NN}	Supply current	-	6.5	-	-	7.0	-	8.0	mA	V _{PP} = +160V	All output switches are turning On and Off at 50kHz with no load
		-	4.0	-	-	5.0	-	5.5		V _{NN} = -40V	
		-	4.0	-	-	5.0	-	5.5		V _{PP} = +100V V _{NN} = -100V	
I _{DD}	Logic supply average current	-	4.0	-	-	4.0	-	4.0	mA	f _{CLK} = 5.0MHz, V _{DD} = 5.0V	
I _{DDQ}	Logic supply quiescent current	-	10	-	-	10	-	10	μA	---	
I _{SOR}	Data out source current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = V _{DD} -0.7V	
I _{SINK}	Data out sink current	0.45	-	0.45	0.70	-	0.40	-	mA	V _{OUT} = 0.7V	
C _{IN}	Logic input capacitance	-	10	-	-	10	-	10	pF	---	

AC Electrical Characteristics

(Over recommended operating conditions: $V_{DD} = 5.0V$, unless otherwise specified)

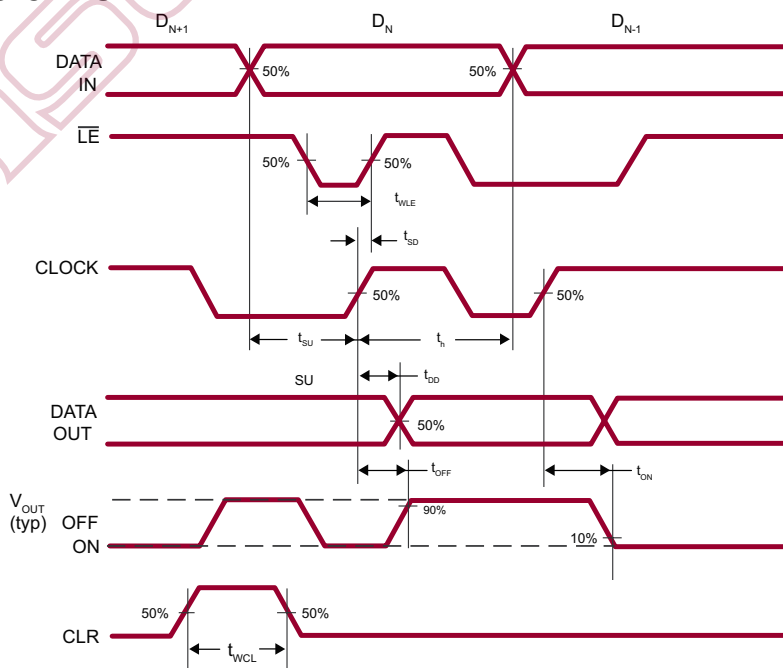
Sym	Parameter	0°C		+25°C			+70°C		Units	Conditions
		Min	Max	Min	Typ	Max	Min	Max		
t_{SD}	Set up time before \overline{LE} rises	150	-	150	-	-	150	-	ns	---
t_{WLE}	Time width of \overline{LE}	150	-	150	-	-	150	-	ns	---
t_{DO}	Clock delay time to data out	-	150	-	-	150	-	150	ns	---
t_{WCL}	Time width of CL	150	-	150	-	-	150	-	ns	---
t_{SU}	Set up time data to clock	15	-	15	8.0	-	20	-	ns	---
t_H	Hold time data from clock	35	-	35	-	-	35	-	ns	---
f_{CLK}	Clock frequency	-	5.0	-	-	5.0	-	5.0	MHz	50% Duty cycle, $f_{DATA} = f_{CLK}/2$
t_R, t_F	Clock rise and fall times	-	50	-	-	50	-	50	ns	---
t_{ON}	Turn on time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
t_{OFF}	Turn off time	-	5.0	-	-	5.0	-	5.0	μs	$V_{SIG} = V_{PP} - 10V, R_{LOAD} = 10k\Omega$
dv/dt	Maximun V_{SIG} slew rate	-	20	-	-	20	-	20	V/ns	$V_{PP} = +160V, V_{NN} = -40V$
		-	20	-	-	20	-	20		$V_{PP} = +100V, V_{NN} = -100V$
		-	20	-	-	20	-	20		$V_{PP} = +40V, V_{NN} = -160V$
K_O	Off isolation	-30	-	-30	-33	-	-30	-	dB	$f = 5.0MHz, 1.0k\Omega/15pF$ load
		-58	-	-58	-	-	-58	-		$f = 5.0MHz, 50\Omega$ load
K_{CR}	Switch crosstalk	-60	-	-60	-70	-	-60	-	dB	$f = 5.0MHz, 50\Omega$ load
I_{ID}	Output switch isolation diode current	-	300	-	-	300	-	300	mA	300ns pulse width, 2.0% duty cycle
$C_{SG(OFF)}$	Off capacitance SW to GND	5.0	17	5.0	12	17	5.0	17	pF	0V, $f = 1.0MHz$
$C_{SG(ON)}$	On capacitance SW to GND	25	50	25	38	50	25	50	pF	0V, $f = 1.0MHz$
$+V_{SPK}$	Output voltage spike	-	-	-	-	150	-	-	mV	$V_{PP} = +40V, V_{NN} = -160V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +100V, V_{NN} = -100V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
$+V_{SPK}$		-	-	-	-	150	-	-		$V_{PP} = +160V, V_{NN} = -40V, R_{LOAD} = 50\Omega$
$-V_{SPK}$		-	-	-	-	150	-	-		
QC	Charge injection	-	-	-	820	-	-	-	pC	$V_{PP} = +40V, V_{NN} = -160V, V_{SIG} = 0V$
		-	-	-	600	-	-	-		$V_{PP} = +100V, V_{NN} = -100V, V_{SIG} = 0V$
		-	-	-	350	-	-	-		$V_{PP} = +160V, V_{NN} = -40V, V_{SIG} = 0V$

Truth Table

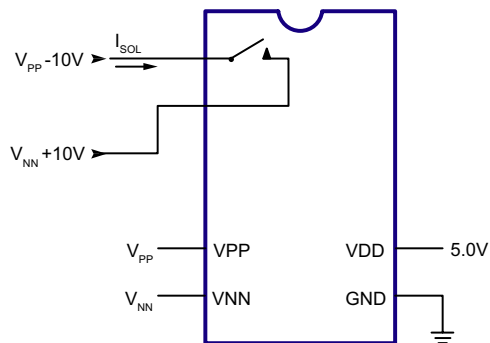
D0	D1	D2	D3	D4	D5	D6	D7	\overline{LE}	CLR	SW0	SW1	SW2	SW3	SW4	SW5	SW6	SW7
L								L	L	Off							
H								L	L	On							
	L							L	L		Off						
	H							L	L		On						
		L						L	L			Off					
		H						L	L			On					
			L					L	L				Off				
			H					L	L				On				
				L				L	L					Off			
				H				L	L					On			
					L			L	L						Off		
					H			L	L						On		
						L		L	L							Off	
						H		L	L							On	
							L	L	L								Off
							H	L	L								On
X	X	X	X	X	X	X	X	H	L	Hold Previous State							
X	X	X	X	X	X	X	X	X	H	All Switches Off							

- Notes:
1. The eight switches operate independently.
 2. Serial data is clocked in on the L to H transition of the CLK.
 3. The switches go to a state retaining their present condition at the rising edge of \overline{LE} . When \overline{LE} is low the shift register data flow through the latch.
 4. D_{OUT} is high when data in the shift register 7 is high.
 5. Shift register clocking has no effect on the switch states if \overline{LE} is high.
 6. The CLR clear input overrides all other inputs.

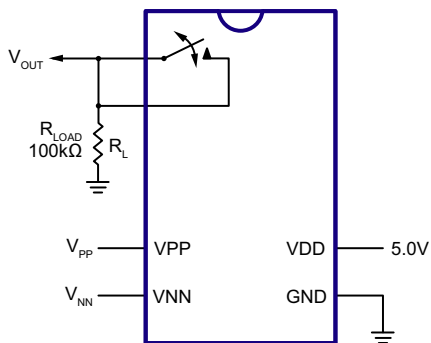
Logic Timing Waveforms



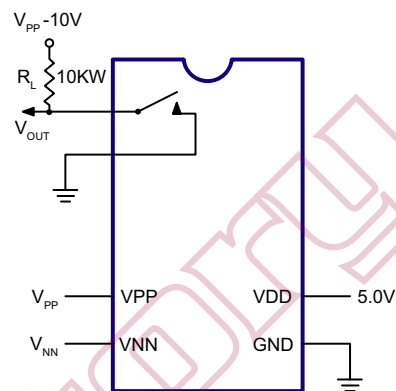
Test Circuits



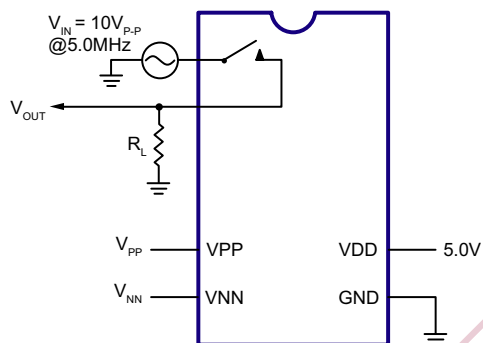
Switch OFF Leakage



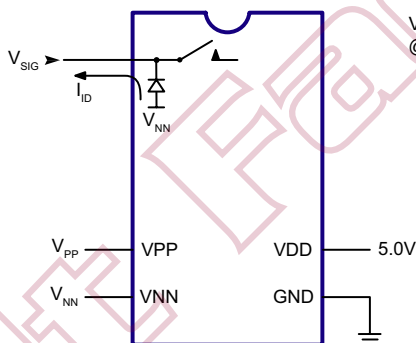
DC Offset ON/OFF



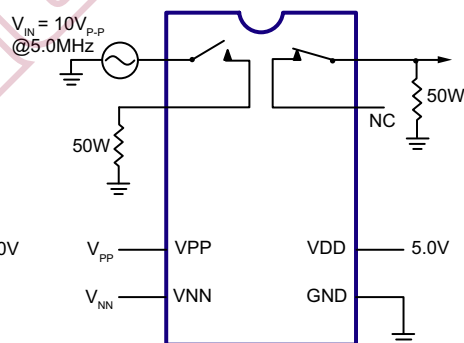
T_{ON}/T_{OFF} Test Circuit



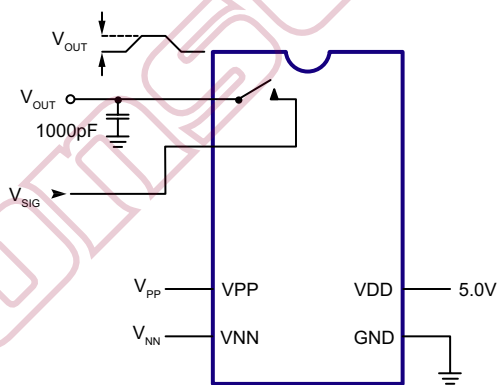
$K_o = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$
OFF Isolation



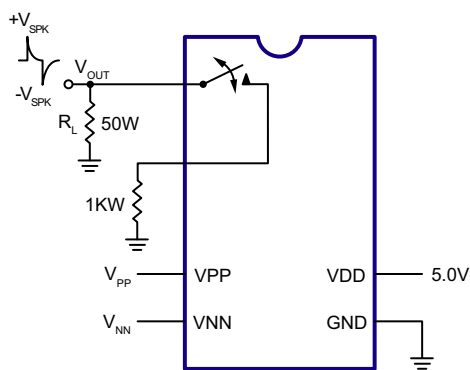
Isolation Diode Current



$K_{CR} = 20 \text{Log} \frac{V_{OUT}}{V_{IN}}$
Crosstalk

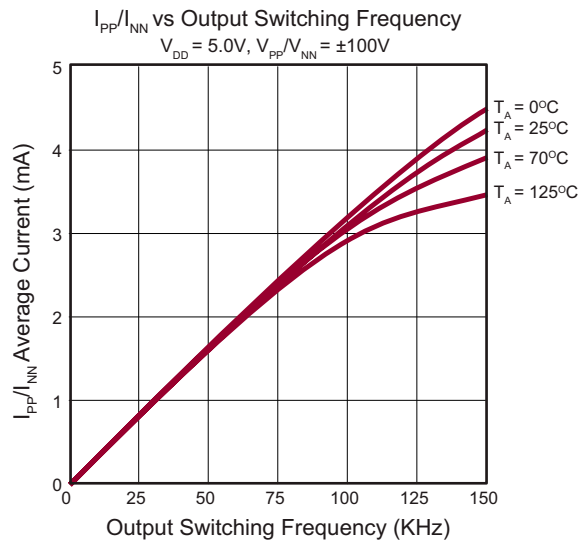
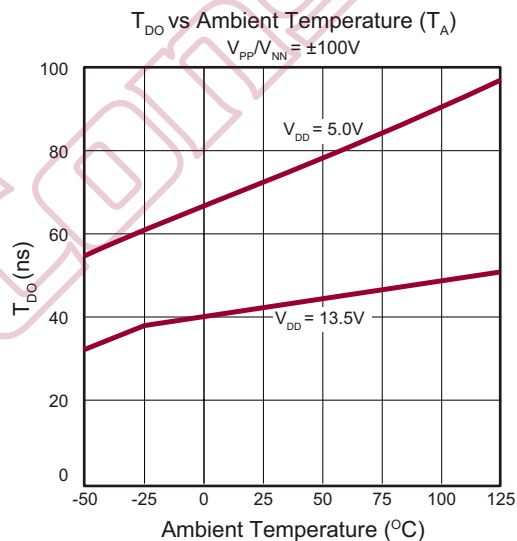
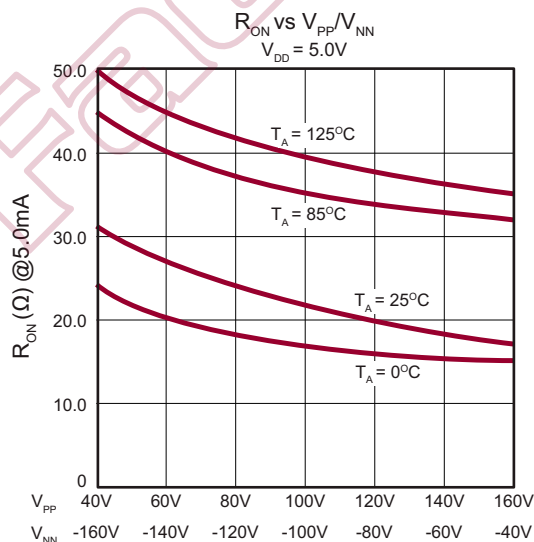
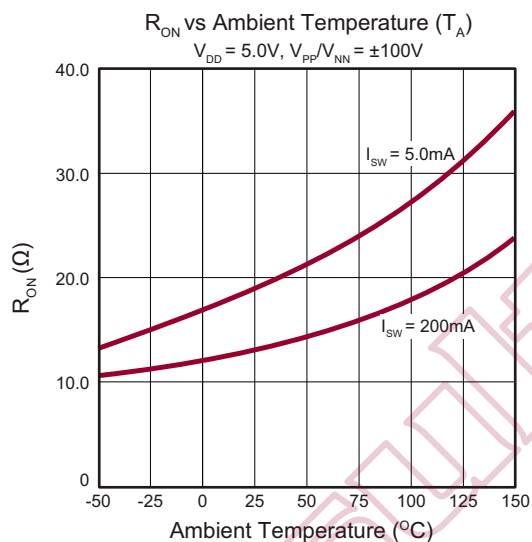
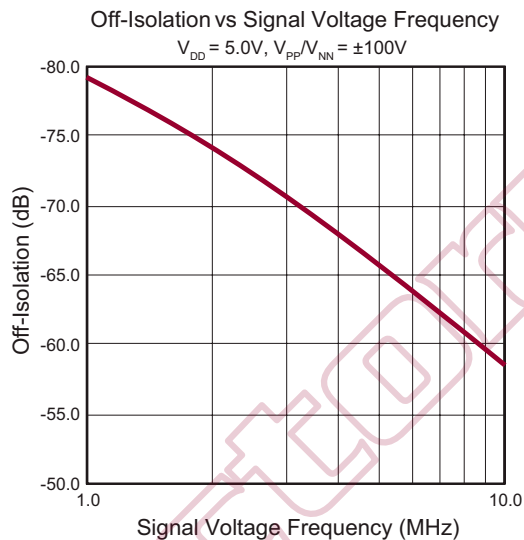
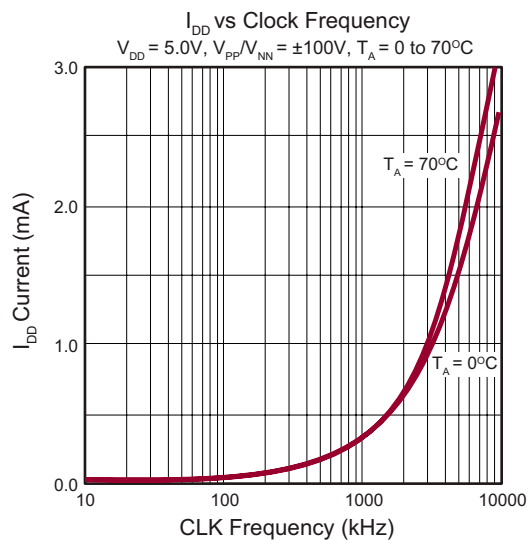


$Q = 1000 \text{pF} \times V_{OUT}$
Charge Injection



Output Voltage Spike

Typical Performance Curves



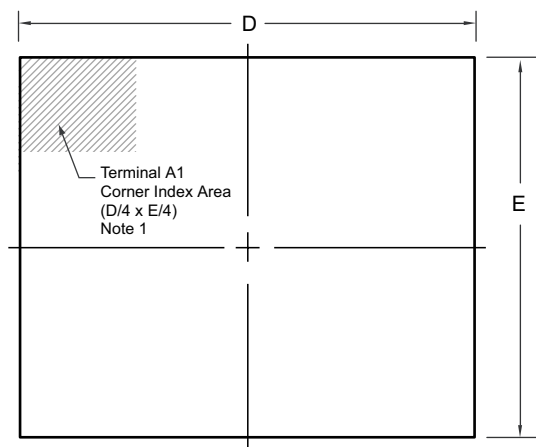
Pin Description

Ball Location	Function
A3	SW1
B2	SW2
B3	SW1
B4	SW0
B5	SW0
B6	VNN
C1	SW3
C2	SW3
C3	SW2
C4	VPP
C5	GND
C6	DIN
C7	VDD

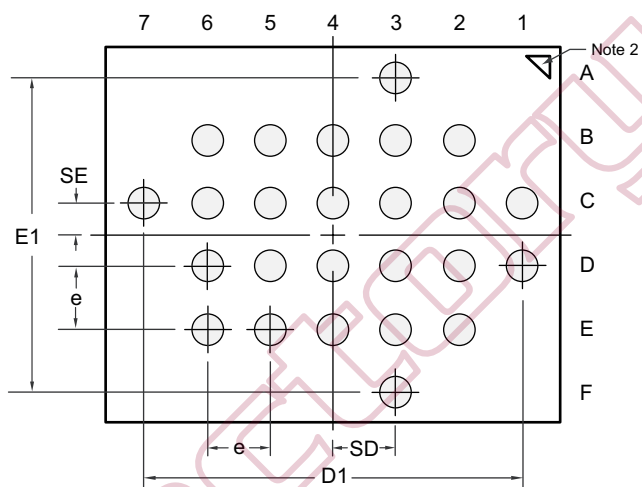
Ball Location	Function
D1	SW4
D2	SW4
D3	SW5
D4	SW7
D5	$\overline{\text{LE}}$
D6	CLK
E2	SW5
E3	SW6
E4	SW7
E5	DOOUT
E6	CLR
F3	SW6

25-Ball fpBGA Package Outline (GA)

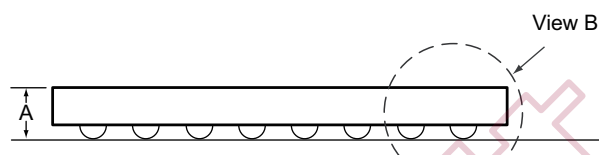
5.70x5.00mm body, 1.20mm height (max), 0.75mm pitch



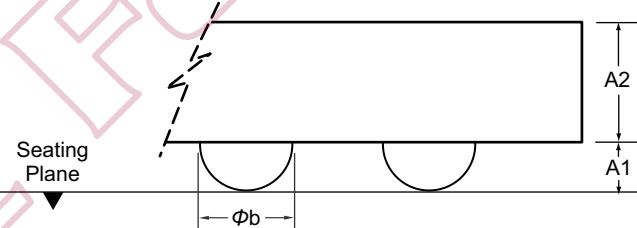
Top View



Bottom View



Side View



View B

Notes:

1. A ball A1 identifier must be located in the index area indicated. The ball A1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Corner A1 identifier (actual shape may vary).

Symbol		A	A1	A2	Φb	D	D1	E	E1	e	SD	SE
Dimension (mm)	MIN	0.844	0.18	0.664	0.25	5.60	4.50 BSC	4.90	3.75 BSC	0.75 BSC	0.75 BSC	0.375 BSC
	NOM	0.994	0.23	0.764	0.30	5.70		5.00				
	MAX	1.200	0.28	0.864	0.35	5.80		5.10				

Drawings not to scale.

Supertex Doc. #: DSPD-25fpBGAGA, Version B092208.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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