

Low Noise Dual EL Lamp Driver

Features

- ▶ Low audible noise
- ▶ Independent input control for lamp selection
- ▶ 180V_{pp} output voltage
- ▶ Split supply capability
- ▶ Patented output timing
- ▶ One miniature inductor to power both lamps
- ▶ Low shutdown current
- ▶ Wide input voltage range 2.0 to 5.8V
- ▶ Output voltage regulation
- ▶ No SCR output
- ▶ Available in 10-Lead DFN package

Applications

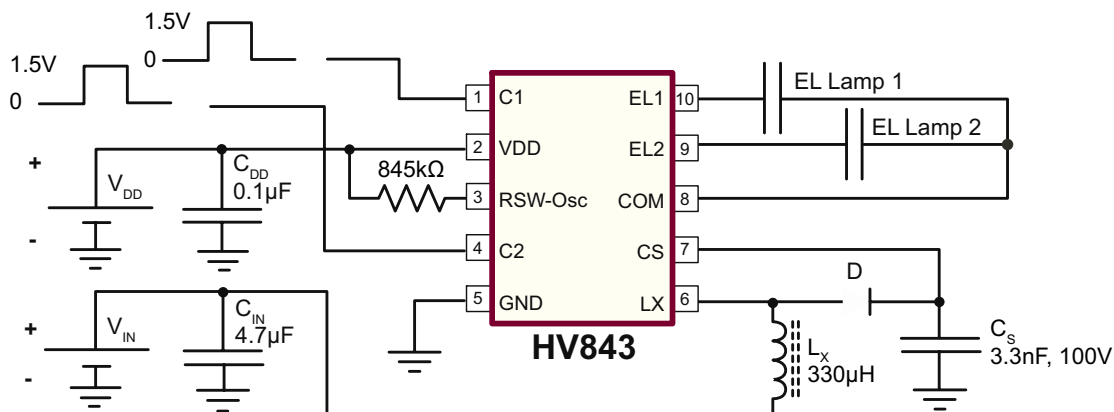
- ▶ Dual display cellular phones
- ▶ Keypad and LCD backlighting
- ▶ Portable instrumentation
- ▶ Dual segment lamps
- ▶ Hand held wireless communication devices

General Description

The Supertex HV843 is a low noise, high voltage driver designed for driving two EL lamps with a combined area of 3.5 square inches. The input supply voltage range is from 2.0V to 5.8V. The device is designed to reduce the amount of audible noise emitted by the lamp. This device uses a single inductor and a minimum number of passive components to drive two EL lamps. The nominal regulated output voltage of ±90V is applied to the EL lamps. The two EL lamps can be turned ON and OFF by the two logic input control pins, C1 and C2. The device is disabled when both C1 and C2 (pins 1 and 4) are at logic low.

The HV843 has an internal oscillator, a switching MOSFET, and two high voltage EL lamp drivers. Each driver has its own half bridge common output (COM1 and COM2) connected to a single pin called COM which minimizes the DC offset seen by the EL lamp. An external resistor connected between the RSW-Osc pin and the voltage supply pin, VDD, sets the frequency for the switching MOSFET. The EL lamp driver frequency is set by dividing the MOSFET switching frequency by 512. An external inductor is connected between the LX and the VDD pins. Depending on the EL lamp size, a 1.0 to 10.0nF, 100V capacitor is connected between CS and Ground. The switching MOSFET charges the external inductor and discharges it into the capacitor at CS. The voltage at CS increases. Once the voltage at CS reaches a nominal value of 90V, the switching MOSFET is turned OFF to conserve power.

Typical Application Circuit



Ordering Information

Device	10-Lead DFN 3.00x3.00mm body 0.80mm height (max) 0.50mm pitch
HV843	HV843K7-G

-G indicates package is RoHS compliant ("Green")



Absolute Maximum Ratings

Parameter	Value
Supply Voltage, V_{DD}	-0.5V to 7.5V
Output Voltage, V_{CS}	-0.5V to 120V
Operating Temperature Range	-40°C to 85°C
Storage temperature	-65°C to 150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Thermal Resistance

Package	θ_{ja}
10-Lead DFN (K7)	60°C/W

Note:

Mounted on FR4 board, 25mm x 25mm x 1.57mm

Recommended Operating Conditions

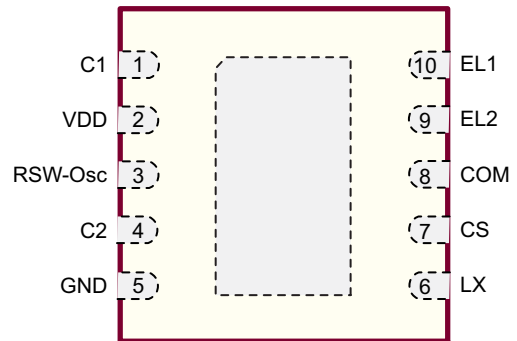
Symbol	Parameter	Min	Typ	Max	Units	Conditions
V_{DD}	Supply voltage	2.0	-	5.8	V	---
T_A	Operating temperature	-40	-	+85	°C	---

Electrical Characteristics

(Over recommended operating conditions unless otherwise specified. $V_{IN} = V_{DD} = 3.3V$, $T_A = 25^\circ C$)

Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	-	10	Ω	$I = 100mA$
V_{DD}	Input voltage range	2.0	-	5.8	V	---
V_{CS}	Output regulation voltage	80	90	100	V	$V_{DD} = 2.0V$ to $5.8V$
V_{DIFF}	Differential output peak to peak voltage (EL1 to COM, EL2 to COM)	160	180	200	V	$V_{DD} = 2.0V$ to $5.8V$
I_{DDQ}	Quiescent V_{DD} supply current	-	-	150	nA	$C_1 = C_2 = 0.1V$
		-	-	250	nA	$C_1 = C_2 = 0.3V$
I_{DD}	Input current into the VDD pin	-	-	250	μA	$V_{DD} = 5.8V$

Pin Configuration

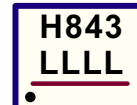


Note:

Pads are on the bottom of the package.
Back-side heat slug is at ground potential.

Product Marking

Top Marking



L = Lot Number

YY = Year Sealed

WW = Week Sealed

— = "Green" Packaging

Bottom Marking



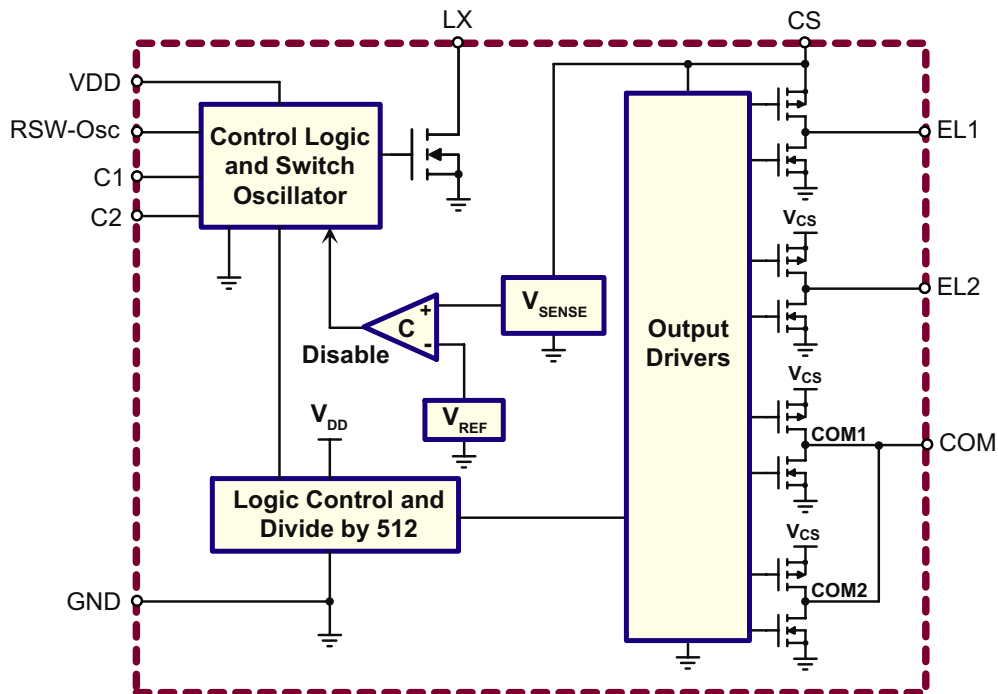
Package may or may not include the following marks: Si or

10-Lead DFN (K7)

Electrical Characteristics (cont.)

Sym	Parameter	Min	Typ	Max	Units	Conditions
I_{IN}	Average input current including inductor current when driving both lamps	-	20	30	mA	$V_{IN} = 5.5V$ (See Fig. 1)
V_{CS}	Output voltage on V_{CS} when driving both lamps	-	87	-	V	$V_{IN} = 5.5V$ (See Fig. 1)
V_{DIF}	Differential output peak to peak voltage across each lamp (EL ₁ to COM1, EL ₂ to COM2)	160	180	200	V	$V_{IN} = 5.5V$ (See Fig. 1)
f_{EL}	V_{DIFF} output drive frequency	170	200	230	Hz	$R_{SW} = 845k\Omega$
f_{SW}	Switching transistor frequency	87	102	118	kHz	$R_{SW} = 845k\Omega$
$f_{SW temp}$	Switching transistor frequency tempco	-	15	-	%	$T_A = -40^\circ C$ to $+85^\circ C$
D	Switching transistor duty cycle	-	85	-	%	$T_A = -40^\circ C$ to $+85^\circ C$
I_{IL}	Input logic low current	-	-	1.0	μA	$V_{DD} = 2.0$ to $5.8V$
I_{IH}	Input logic high current	-	-	1.0	μA	$V_{DD} = 2.0$ to $5.8V$
V_{IL}	Logic input low voltage	0	-	0.3	V	---
V_{IH}	Logic input high voltage	1.5	-	V_{DD}	V	---

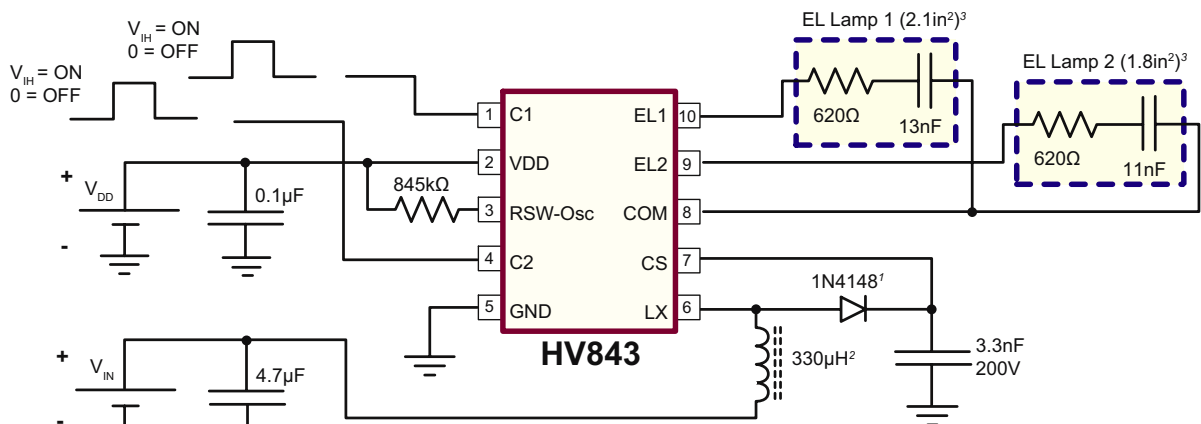
Functional Block Diagram



Function Table

Logic Inputs		Outputs			Device
C ₁	C ₂	EL ₁	EL ₂	COM	
0	0	Hi Z	Hi Z	Hi Z	OFF
0	1	Hi Z	ON	ON	ON
1	0	ON	Hi Z	ON	ON
1	1	ON	ON	ON	ON

Fig. 1 - Test Circuit



1. or any (equivalent or better) >90V, fast recovery diode
2. Cooper LPO6610-334MLB
3. The bigger sized lamp should be tied to EL1 and the smaller sized lamp to EL2 terminals (pins 10 and 9 respectively)

Typical Performance

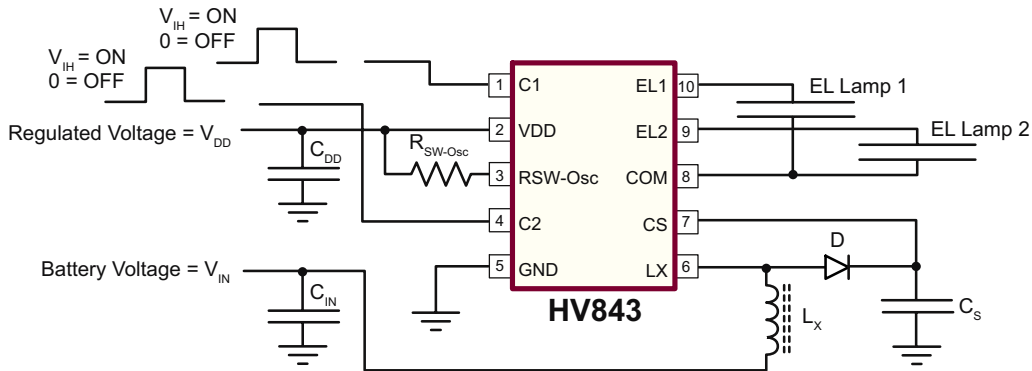
Lamp	V _{DD} (V)	V _{IN} (V)	I _{IN} (mA)	V _{CS} (V _{PEAK})	f _{EL} (Hz)	Lamp Brightness (cd/m ²)	
						EL ₁	EL ₂
EL ₁ ON	3.0V	5.2V	7.96	88	195	13.89	-
EL ₂ ON			6.91			-	12.89
Both EL ₁ and EL ₂ ON			13.93			13.02	11.24
EL ₁ ON		5.5V	7.47			13.93	-
EL ₂ ON			6.42			-	13.22
Both EL ₁ and EL ₂ ON			13.42			13.30	12.05
EL ₁ ON		5.8V	7.04			14.03	-
EL ₂ ON			6.01			-	13.30
Both EL ₁ and EL ₂ ON			12.94			13.55	12.51

Split Supply Configuration

The HV843 can be used in applications operating from a battery where a regulated voltage is available. This is shown in Fig. 2. The regulated voltage can be used to drive the internal logic of HV843. The amount of current used to drive

the internal logic is less than 200µA. Therefore, the regulated voltage could easily provide the current without being loaded down.

Fig. 2 - Split Supply Configuration

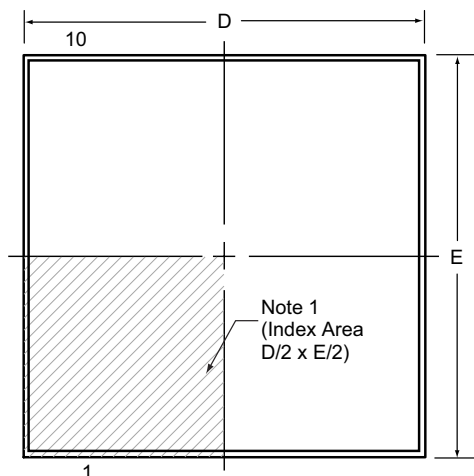


Pin Configuration and Description

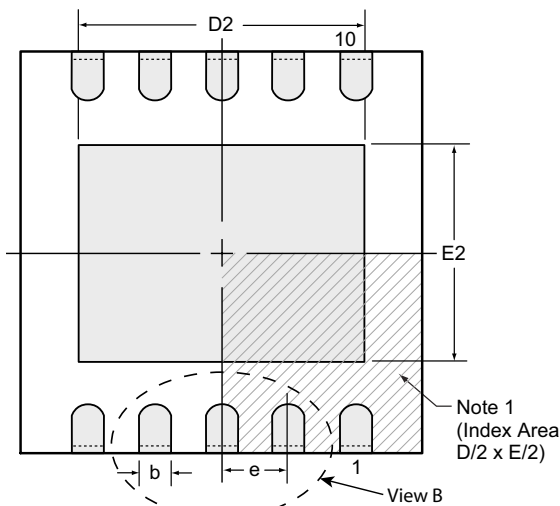
Pin #	Function	Description
1	C1	Enable input signal for EL Lamp 1. Logic high will turn ON the EL lamp 1 and logic low will turn it OFF. Refer to the function table.
2	VDD	Input voltage supply pin.
3	RSW-Osc	External resistor connection to set both the switching MOSFET frequency and EL Lamp frequency. The external resistor should be connected between VDD and this pin. The EL lamp frequency is the switching frequency divided by 512. The switching frequency is inversely proportional to the resistor value. A 845kΩ resistor will provide a nominal switching frequency of 102kHz and an EL lamp frequency of 200Hz. To change the frequency to f_{EL1} , the value of the resistor $R_{SW-Osc1}$ can be determined as $R_{SW-Osc1} = (845 \times 200) / f_{EL1}$ kΩ.
4	C2	Enable input signal for EL Lamp 2. Logic high will turn ON the EL lamp 2 and logic low will turn it OFF. Refer to the function table.
5	GND	Device ground.
6	LX	Drain of internal switching MOSFET. Connection for an external inductor. When the switching MOSFET is turned ON, the inductor is being charged. When the MOSFET is turned OFF, the energy stored in the inductor is transferred to the high voltage capacitor connected at the CS pin.
7	CS	Connect a 100V capacitor between this pin and GND. This capacitor stores the energy transferred from the inductor.
8	COM	Common lamp connection for both EL1 and EL2. Connect one end of both the lamps to this pin.
9	EL2	EL lamp 2 connection. For optimum performance, the smaller of the two lamps should be connected to this pin.
10	EL1	EL lamp 1 connection. For optimum performance, the larger of the two lamps should be connected to this pin.

10-Lead DFN Package Outline (K7)

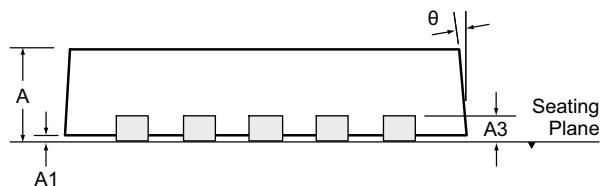
3.00x3.00mm body, 0.80mm height (max), 0.50mm pitch



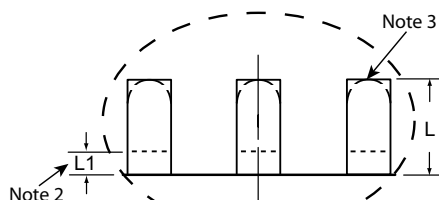
Top View



Bottom View



Side View



View B

Notes:

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.18	2.85*	2.20	2.85*	1.40	0.50 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.25	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.30	3.15*	2.70	3.15*	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEED-5, Issue C, Aug. 2003.

* This dimension is not specified in the JEDEC drawing.

Drawings not to scale.

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(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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