

## High Voltage EL Lamp Driver for Low Noise Applications

### Features

- ▶ Patented audible noise reduction
- ▶ Patented lamp aging compensation
- ▶ 210 V<sub>PP</sub> output voltage for higher brightness
- ▶ Patented output timing for high efficiency
- ▶ Single cell lithium ion compatible
- ▶ 150nA shutdown current
- ▶ Wide input voltage range 1.8 to 5.0V
- ▶ Separately adjustable lamp and converter frequencies
- ▶ Output voltage regulation
- ▶ Split supply capability

### Applications

- ▶ LCD backlighting
- ▶ Mobile Cellular Phone keypads
- ▶ PDAs
- ▶ Handheld wireless communication products
- ▶ Global Positioning Systems (GPS)

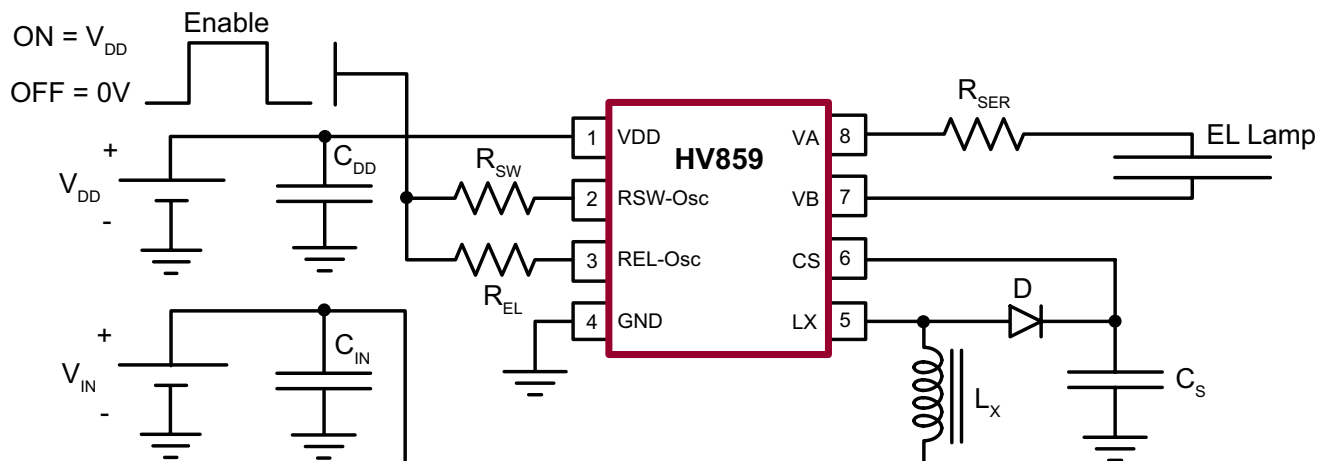
### General Description

The Supertex HV859 is a high voltage driver designed for driving Electroluminescent (EL) lamps of up to 5.0 square inches. The input supply voltage range is from 1.8 to 5.0V. The device uses a single inductor and a minimum number of passive components. The nominal regulated output voltage that is applied to the EL lamp is  $\pm 105V$ . The chip can be enabled/disabled by connecting the resistor on RSW-Osc to VDD/ground.

The HV859 has two internal oscillators, a switching MOSFET, and a high voltage EL lamp driver. The frequency for the switching MOSFET is set by an external resistor connected between the RSW-Osc pin and the supply pin VDD. The EL lamp driver frequency is set by an external resistor connected between REL-Osc pin and the VDD pin. An external inductor is connected between the LX and VDD pins or VIN for split supply applications. A 0.003-0.1 $\mu F$  capacitor is connected between CS and ground. The EL lamp is connected between VA and VB.

The switching MOSFET charges the external inductor and discharges it into the capacitor at CS. The voltage at CS will start to increase. Once the voltage at CS reaches a nominal value of 105V, the switching MOSFET is turned OFF to conserve power. The outputs VA and VB are configured as an H bridge and are switching in opposite states to achieve  $\pm 105V$  across the EL lamp.

### Typical Application Circuit



## Ordering Information

Device	Package Options	
	8-Lead DFN 3.00x3.00mm body 0.80mm height (max) 0.65mm pitch	8-Lead MSOP 3.00x3.00mm body 1.10mm height (max) 0.65mm pitch
HV859	HV859K7-G	HV859MG-G

-G indicates package is RoHS compliant ('Green')



## Absolute Maximum Ratings

Parameter	Value
$V_{DD}$ , Supply voltage	-0.5V to 6.5V
Operating temperature	-40°C to +85°C
Storage temperature	-65°C to +150°C
Power dissipation: 8-Lead DFN (K7)	1.6W
Power dissipation: 8-Lead MSOP (MG)	300mW
$V_{CS}$ , Output voltage	-0.5V to +130V

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

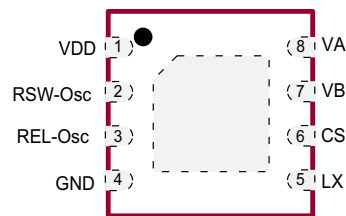
## Thermal Resistance

Package	$\theta_{ja}$
8-Lead DFN (K7)	60 °C/W
8-Lead MSOP (MG)	330 °C/W

## Recommended Operating Conditions

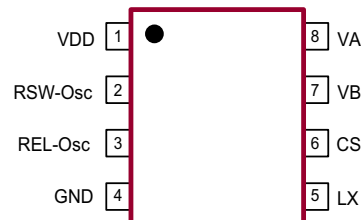
Sym	Parameter	Min	Typ	Max	Units	Conditions
$V_{DD}$	Supply voltage	1.8	-	5.0	V	---
$f_{EL}$	Output drive frequency	-	-	1.0	KHz	---
$T_A$	Operating temperature	-40	-	+85	°C	---

## Pin Configurations



8-Lead DFN (K7)  
(top view)

(Pads are on the bottom of the package)



8-Lead MSOP (MG)  
(top view)

## Product Marking

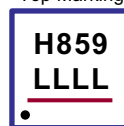


Y = Last Digit of Year Sealed  
W = Code for Week Sealed  
L = Lot Number  
— = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead DFN (K7)

Top Marking



Bottom Marking



L = Lot Number  
YY = Year Sealed  
WW = Week Sealed  
— = "Green" Packaging

Package may or may not include the following marks: Si or

8-Lead MSOP (MG)

### Enable/Disable Function Table

Sym	Parameter	Min	Typ	Max	Units	Conditions
EN-L	Logic input low voltage	0	-	0.2	V	$V_{DD} = 1.8$ to $5.0V$
EN-H	Logic input high voltage	$V_{DD} - 0.2$	-	$V_{DD}$	V	$V_{DD} = 1.8$ to $5.0V$

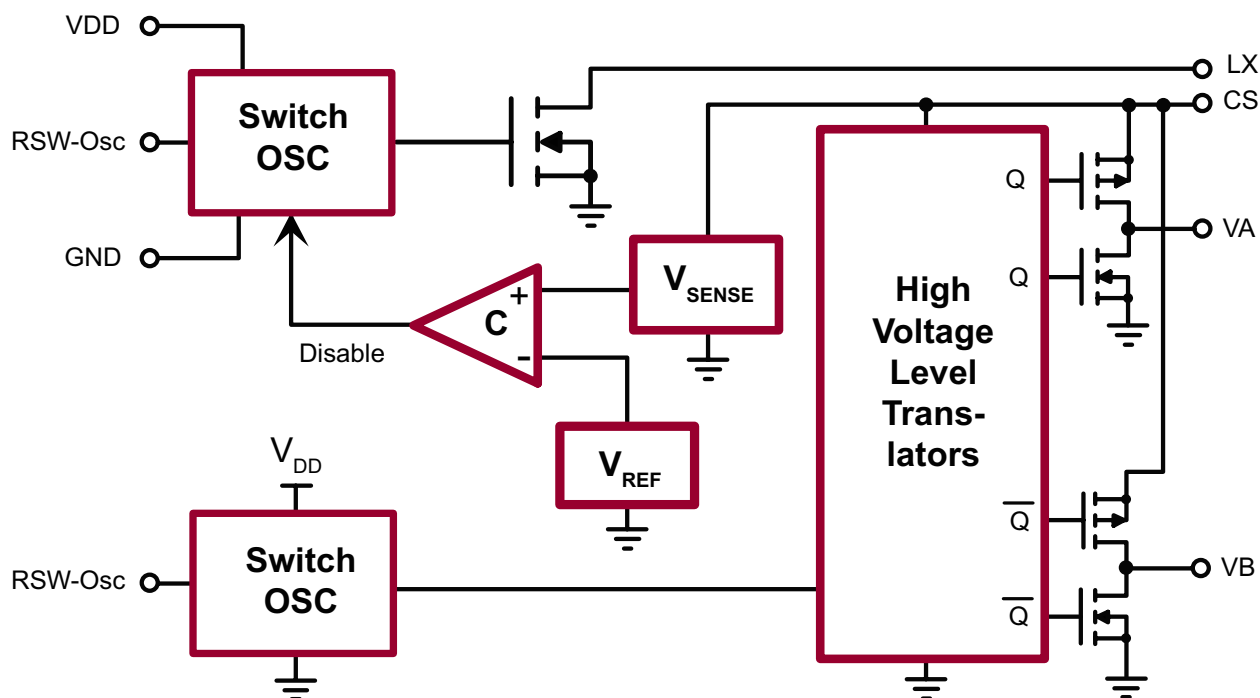
### Electrical Characteristics

**DC Characteristics** (Over recommended operating conditions unless otherwise specified  $V_{IN} = V_{DD} = 3.3V$ ,  $T_A = 25^\circ C$ )

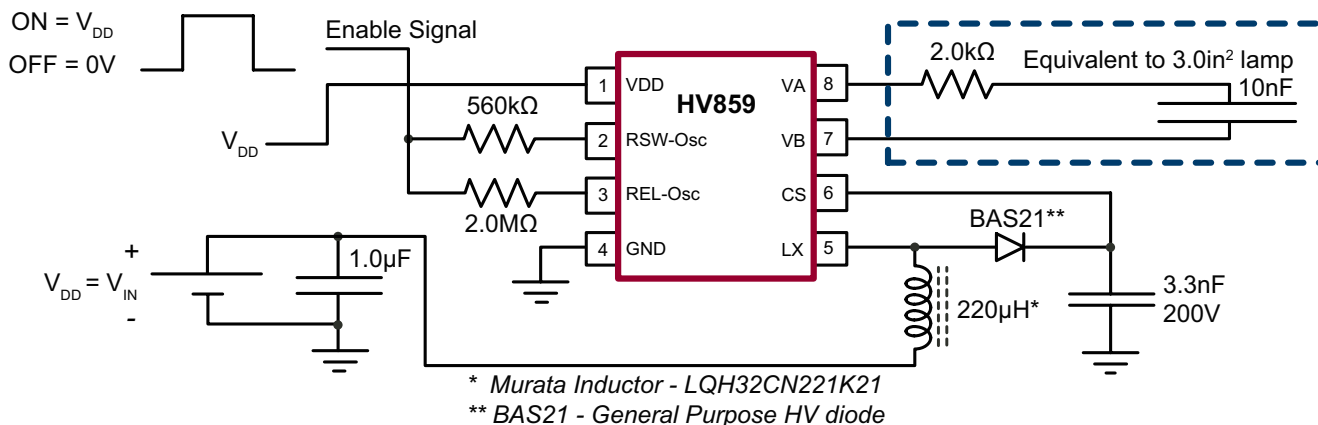
Sym	Parameter	Min	Typ	Max	Units	Conditions
$R_{DS(ON)}$	On-resistance of switching transistor	-	-	6.0	$\Omega$	$I = 100mA$
$V_{CS}$	Max. output regulation voltage	95	105	115	V	$V_{DD} = 1.8$ to $5.0V$
$V_A - V_B$	Peak to peak output voltage	190	210	230	V	$V_{DD} = 1.8$ to $5.0V$
$I_{DDQ}$	Quiescent $V_{DD}$ supply current	-	-	150	nA	$R_{SW-Osc} = Low$
$I_{DD}$	Input current going into the VDD pin	-	-	150	$\mu A$	$V_{DD} = 1.8$ to $5.0V$ . See Fig. 1.
$I_{IN}$	Input current including inductor current	-	26	35	mA	See Fig. 1.*
$V_{CS}$	Output voltage on VCS	-	90	-	V	See Fig. 1.
$F_{EL}$	EL lamp frequency	175	205	235	Hz	See Fig. 1.
$F_{SW}$	Switching transistor frequency	-	77	-	kHz	---
D	Switching transistor duty cycle	-	88	-	%	See Fig. 1.

\*The inductor used is a 220 $\mu H$  Murata inductor, max DC resistance of 8.4 $\Omega$ , part # LQH32CN221K21.

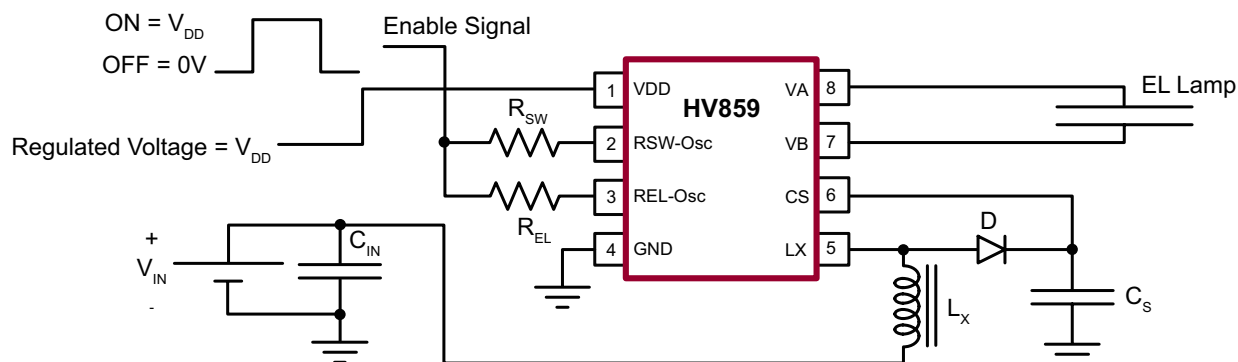
### Functional Block Diagram



**Fig. 1: Typical Application/Test Circuit**



**Fig. 2: Split Supply and Enable/Disable Configuration**

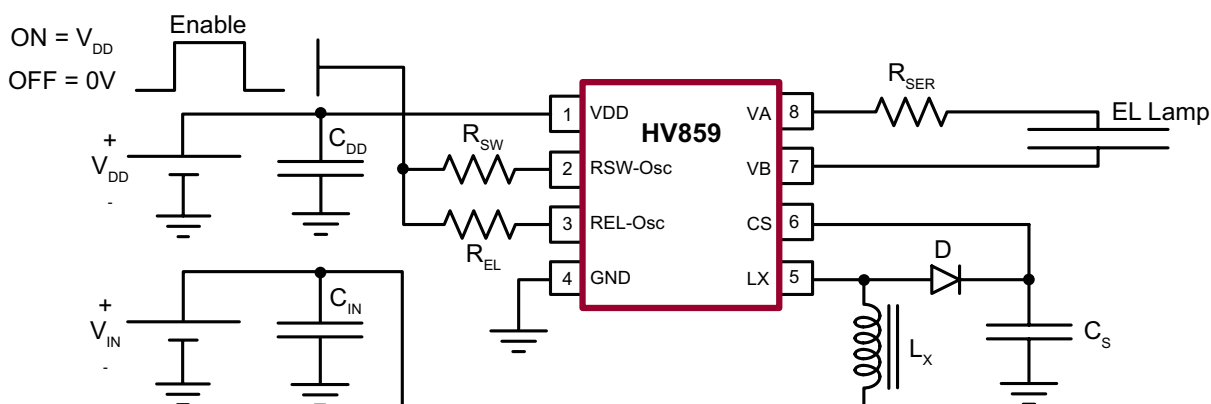


## Split Supply Configuration

The HV859 can also be used for handheld devices operating from a battery where a regulated voltage is available. This is shown in Fig. 2. The regulated voltage can be used to run the internal logic of the HV859. The amount of current necessary to run the internal logic is 150µA max at a  $V_{DD}$  of 3.0V. Therefore, the regulated voltage could easily provide the current without being loaded down.

The HV859 can be easily enabled and disabled via a logic control signal on the  $R_{SW}$  and  $R_{EL}$  resistors as shown in Fig. 2 below. The control signal can be from a microprocessor.  $R_{SW}$  and  $R_{EL}$  are typically very high values. Therefore, only 10's of microamperes will be drawn from the logic signal when it is at a logic high (enable) state. When the microprocessor signal is high the device is enabled, and when the signal is low, it is disabled.

**Fig. 3: Typical Application Circuit for Audible Noise Reduction**



## Audible Noise Reduction

This section describes a method (patented) developed at Supertex to reduce the audible noise emitted by the EL lamps used in application sensitive to audible noise. Fig. 3 shows a general circuit schematic that uses the resistor,  $R_{SER}$ , connected in series with the EL lamp.

### How to Minimize EL Lamp Audible Noise:

The EL lamp, when lit, emits an audible noise. This is due to EL lamp construction and it creates a major problem for applications where the EL lamp can be close to the ear such as cellular phones. The noisiest waveform is a square wave and the quietest waveform has been assumed to be a sine wave.

After extensive research, Supertex has developed a waveform that is quieter than a sine wave. The waveform takes the shape of approximately  $2RC$  time constants for rising and  $2RC$  time constants for falling, where  $C$  is the capacitance of the EL lamp, and  $R$  is the external resistor,  $R_{SER}$ , connected in series with the EL lamp. This waveform has been proven to generate less noise than a sine wave.

The audible noise from the EL lamp can be set at a desired level based on the series resistor value used with the lamp.

It is important to note that use of this resistor will reduce the voltage across the lamp. Reduction of voltage across the lamp will also have another effect on the overall performance of the Supertex EL drivers, age compensation (patented). This addresses a very important issue, EL lamp life that most mobile phone manufacturers are concerned about.

As EL lamp ages, its brightness is reduced and its capacitance is diminished. By using the RC model to reduce the audible noise emitted by the EL lamp, the voltage across the lamp will increase as its capacitance diminishes. Hence the increase in voltage will compensate for the reduction of the brightness. As a result, it will extend the EL lamp's half-life (half the original brightness).

### Effect of Series Resistor on EL Lamp Audible Noise and Brightness:

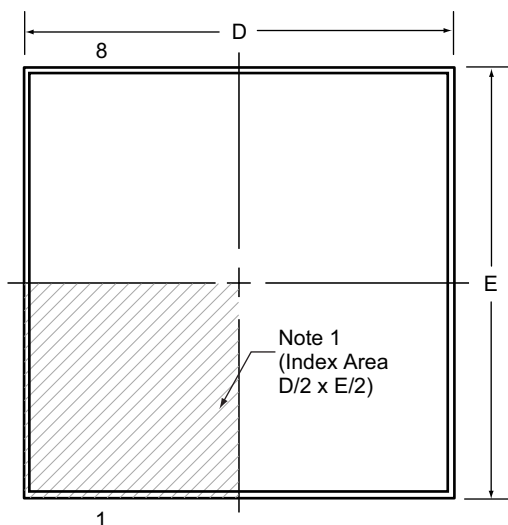
Increasing the value of the series resistor with the lamp will reduce the EL lamp audible noise as well as its brightness. This is due to the fact that the output voltage across the lamp will be reduced and the output waveform will have rounder edges.

## External Component Description

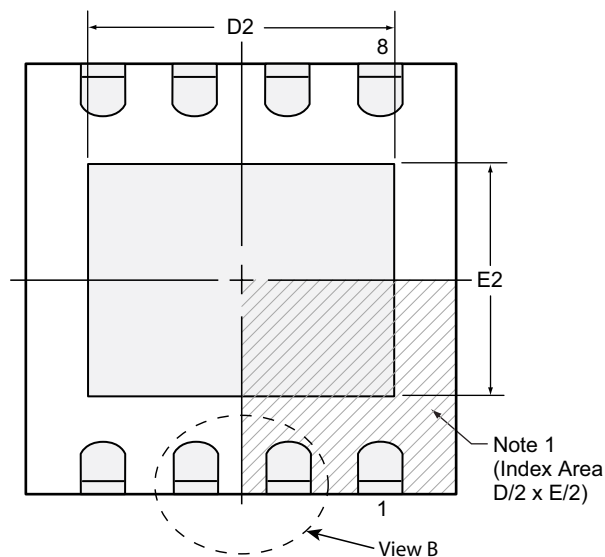
External Component	Selection Guide Line
Diode	Fast reverse recovery diode, BAS21 diode or equivalent.
$C_s$ Capacitor	0.003 $\mu$ F to 0.1 $\mu$ F, 200V capacitor to GND is used to store the energy transferred from the inductor.
$R_{EL}$ Resistor	<p>The EL lamp frequency is controlled via an external <math>R_{EL}</math> resistor connected between REL-Osc and VDD of the device. The lamp frequency increases as <math>R_{EL}</math> decreases. As the EL lamp frequency increases, the amount of current drawn from the battery will increase and the output voltage <math>V_{CS}</math> will decrease. The color of the EL lamp is dependent upon its frequency.</p> <p>A 2M<math>\Omega</math> resistor would provide lamp frequency of 175 to 235Hz. Decreasing the <math>R_{EL}</math> resistor by a factor of 2 will increase the lamp frequency by a factor of 2.</p>
$R_{SW}$ Resistor	The switching frequency of the converter is controlled via an external resistor, $R_{SW}$ between RSW-Osc and VDD of the device. The switching frequency increases as $R_{SW}$ decreases. With a given inductor, as the switching frequency increases, the amount of current drawn from the battery will decrease and the output voltage, $V_{CS}$ , will also decrease.
$L_x$ Inductor	<p>The inductor <math>L_x</math> is used to boost the low input voltage by inductive flyback. When the internal switch is on, the inductor is being charged. When the internal switch is off, the charge stored in the inductor will be transferred to the high voltage capacitor <math>C_s</math>. The energy stored in the capacitor is connected to the internal H-bridge, and therefore to the EL lamp. In general, smaller value inductors, which can handle more current, are more suitable to drive larger size lamps. As the inductor value decreases, the switching frequency of the inductor (controlled by <math>R_{SW}</math>) should be increased to avoid saturation.</p> <p>A 220<math>\mu</math>H Murata (LQH32CN221) inductor with 8.4<math>\Omega</math> series DC resistance is typically recommended. For inductors with the same inductance value, but with lower series DC resistance, lower <math>R_{SW}</math> resistor value is needed to prevent high current draw and inductor saturation.</p>
Lamp	As the EL lamp size increases, more current will be drawn from the battery to maintain high voltage across the EL lamp. The input power, ( $V_{IN} \times I_{IN}$ ), will also increase. If the input power is greater than the power dissipation of the package, an external resistor in series with one side of the lamp is recommended to help reduce the package power dissipation.

# 8-Lead DFN Package Outline (K7)

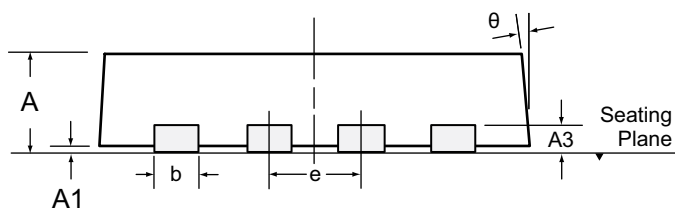
3.00x3.00mm body, 0.80mm height (max), 0.65mm pitch



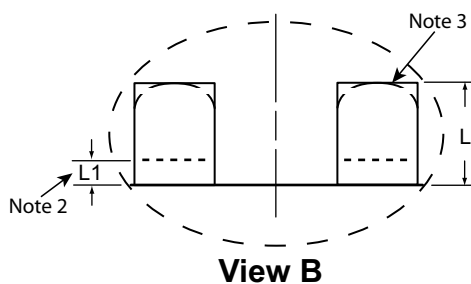
**Top View**



**Bottom View**



**Side View**



**View B**

**Notes:**

1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.
2. Depending on the method of manufacturing, a maximum of 0.15mm pullback (L1) may be present.
3. The inner tip of the lead may be either rounded or square.

Symbol	A	A1	A3	b	D	D2	E	E2	e	L	L1	θ	
Dimension (mm)	MIN	0.70	0.00	0.20 REF	0.25	2.85*	1.60	2.85*	1.35	0.65 BSC	0.30	0.00*	0°
	NOM	0.75	0.02		0.30	3.00	-	3.00	-		0.40	-	-
	MAX	0.80	0.05		0.35	3.15*	2.50	3.15*	1.75		0.50	0.15	14°

JEDEC Registration MO-229, Variation WEEC-2, Issue C, Aug. 2003.

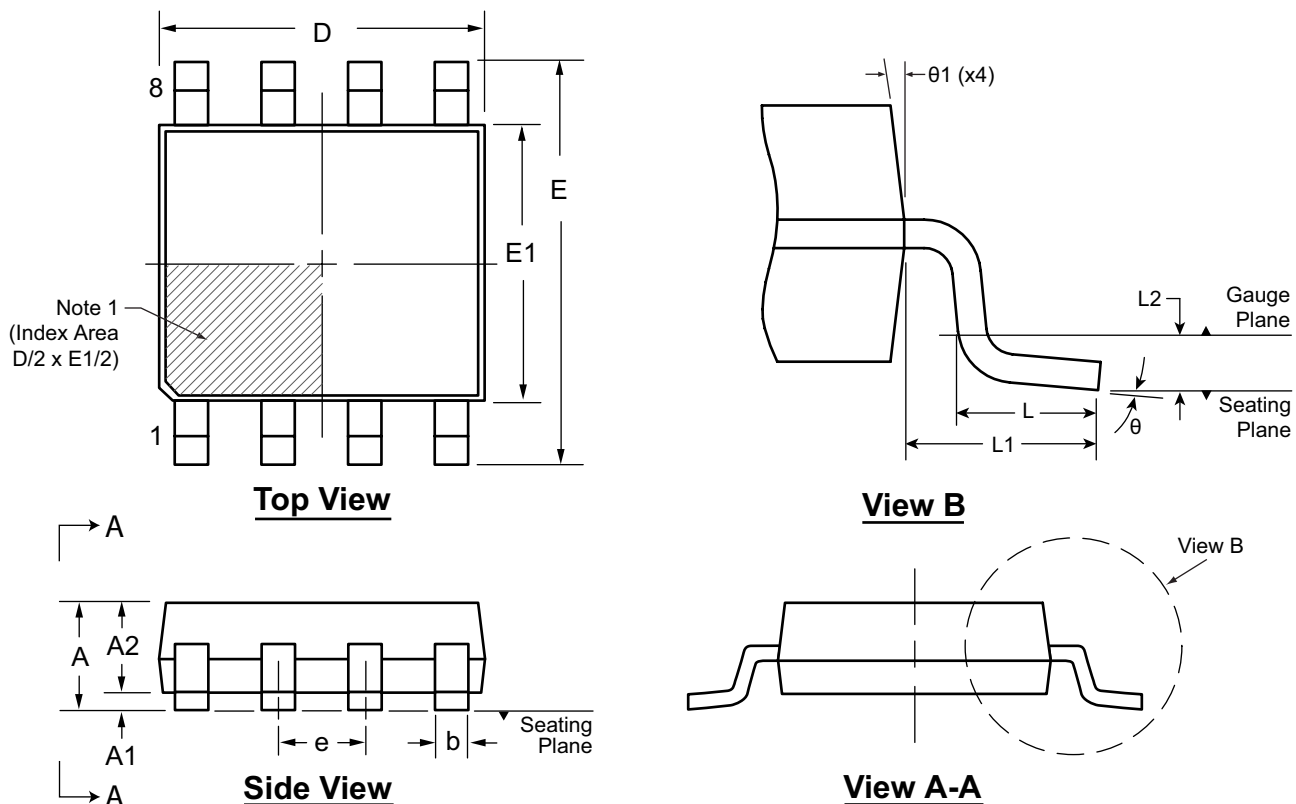
\* This dimension is not specified in the JEDEC drawing.

**Drawings not to scale.**

**Supertex Doc. #:** DSPD-8DFNK73X3P065, Version C081109.

# 8-Lead MSOP Package Outline (MG)

3.00x3.00mm body, 1.10mm height (max), 0.65mm pitch



**Note:**  
 1. A Pin 1 identifier must be located in the index area indicated. The Pin 1 identifier can be: a molded mark/identifier; an embedded metal marker; or a printed indicator.

Symbol	A	A1	A2	b	D	E	E1	e	L	L1	L2	θ	θ1
Dimension (mm)	MIN	0.75*	0.00	0.75	0.22	2.80*	4.65*	2.80*	0.40	0.95 REF	0.25 BSC	0°	5°
	NOM	-	-	0.85	-	3.00	4.90	3.00	0.60			-	-
	MAX	1.10	0.15	0.95	0.38	3.20*	5.15*	3.20*	0.80			8°	15°

JEDEC Registration MO-187, Variation AA, Issue E, Dec. 2004.

\* This dimension is not specified in the JEDEC drawing.

Drawings are not to scale.

Supertex Doc. #: DSPD-8MSOPMG, Version H041309.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to <http://www.supertex.com/packaging.html>.)

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