

AN221K04-v3 – AnadigmVortex Development Board

1.0 Overview

The AnadigmVortex development board is an easy-to-use platform designed to help you get started with implementing and testing your analog designs on the AnadigmVortex FPAA silicon devices.

While the device on this development platform is an AN221E04 device, you can use this board to implement all of your AN221E02, AN120E04, AN121E04, AN220E04 and AN221E04 designs. The design software - AnadigmDesigner[®]2 – can use the AN221E04 device on board to emulate any device in the Anadigmvortex device family.

This manual provides an overview on how to effectively use this board to implement your analog design. But first, here are some salient features of the AnadigmVortex development board:

- Small footprint – 4 inches square
- Large breadboard area around the AN221E04 device
- Header pins for all the FPAA device analog I/Os
- Ability to separate, electrically and physically, the digital section
- Daisy chain capability – that allows multiple boards to be connected to evaluate multi-chip systems
- Standard PC serial interface for downloading AnadigmDesigner[®]2 circuit files
- On-board 16-MHz oscillator module

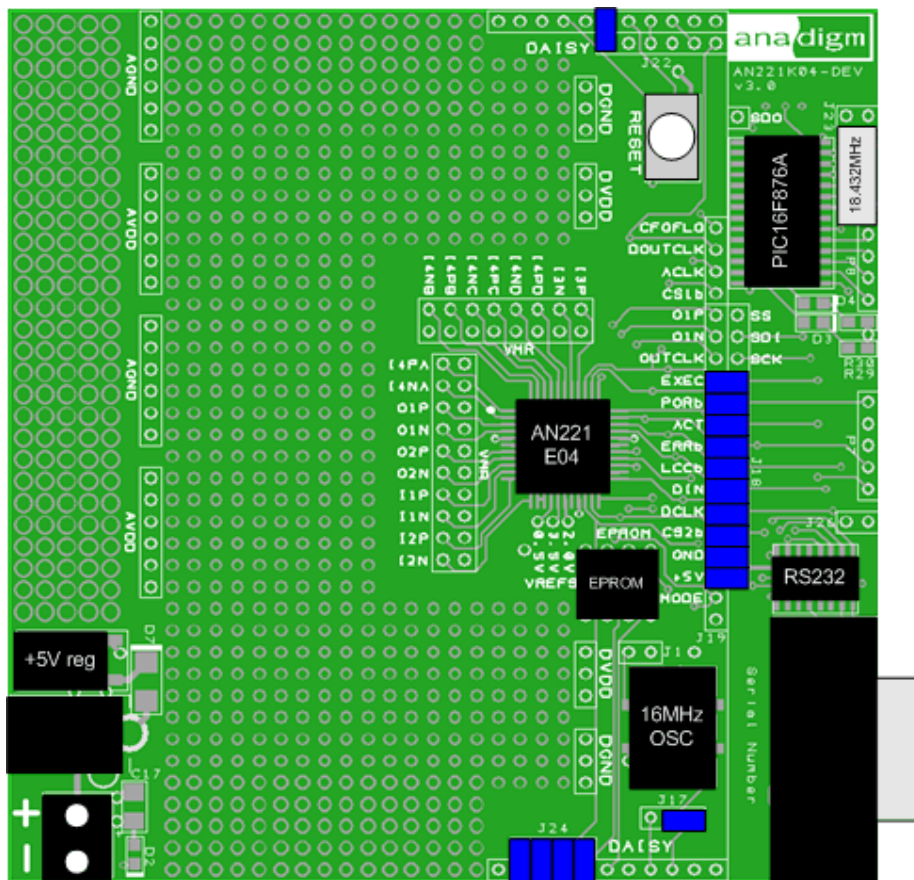


Figure 1: AnadigmVortex Development Board

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2.0 Layout

Figure 2 shows the layout of the board allowing easy location of all the components, power connections and jumpers.

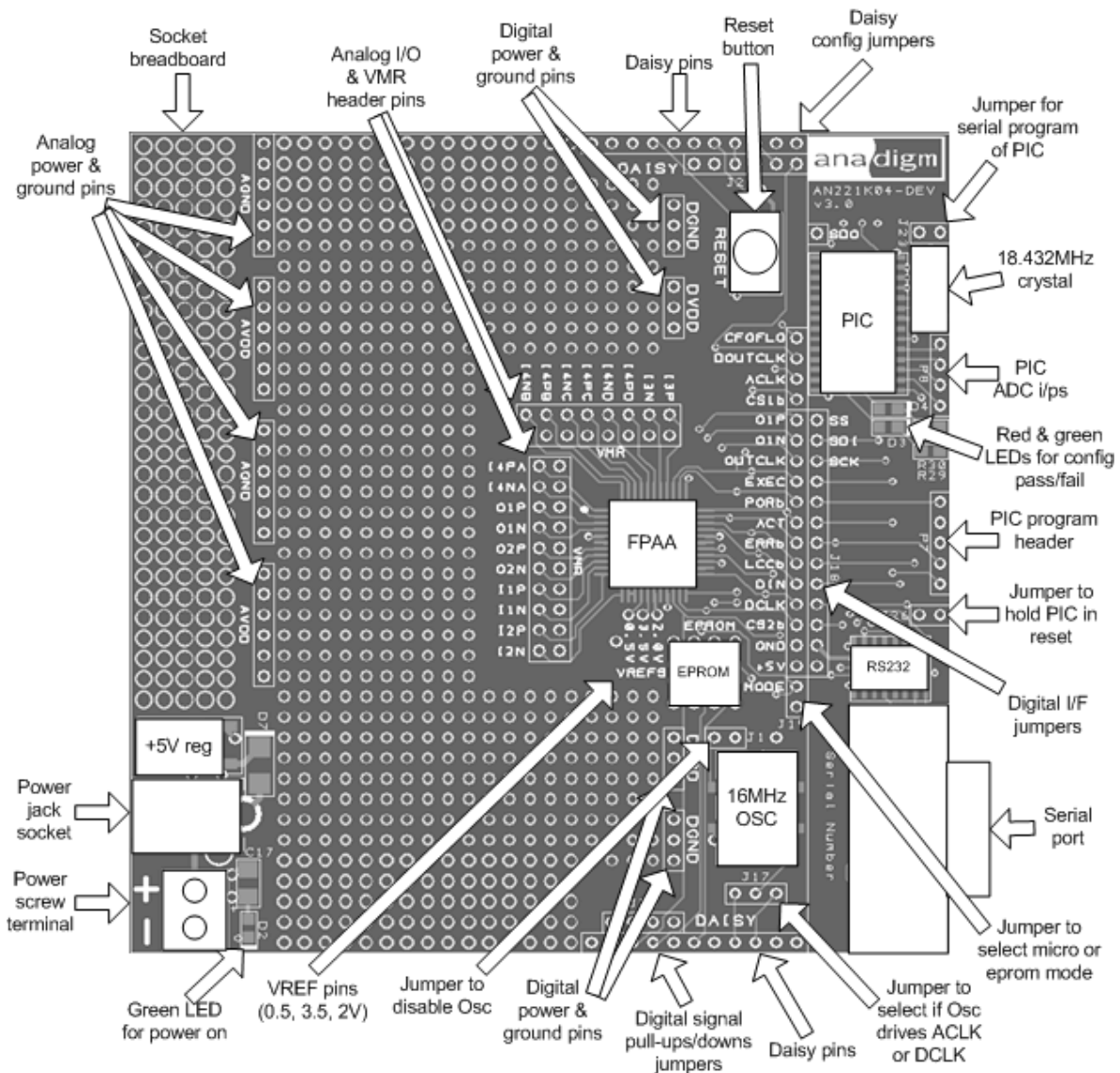


Figure 2: Top-level layout of the AnadigmVortex development board

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3.0 Powering up the AnadigmApex Development Board

The options for powering up the board are as follows:

- Connect a transformer with centre voltage between +5.5V and +20V to the jack socket input, OR
- Connect wires from a single precision, regulated supply to the on-board 2-way terminal with the voltage set to between 5.5V and 20V.
- Anadigm recommends the use of a standard supply regulator or d.c. power supply 6, 9, or 12 volt d.c. regulated output.

NOTE: the board is protected against connection to a supply with the wrong polarity

WARNING: the board should not be powered with more than 20V

There is a green LED to indicate that the board is successfully powered up. The board should take approximately 25mA when first powered up and before the FPAA is configured. The current after the FPAA is configured depends very much on the circuit programmed into the FPAA.

4.0 Programming the Board

Once the board has been powered up, simply connect the board to the serial port of a PC using a standard RS232 cable. Open AnadigmDesigner^{®2} on the PC, create a circuit and click on Configure. If configuration is successful, the green LED next to the PIC in the digital section will light. If the red LED lights then the configuration failed. If this happens then check the supply to the board and check that the pins marked AVDD have +5 V on them. Also check that the jumpers are in their default state (see figure 7 in section 7). Press the reset button and try again.

If configuration was successful then the circuit created in AnadigmDesigner^{®2} will be programmed into the FPAA. The analog inputs and outputs can be accessed via the header pins that surround the FPAA. Note that the outer pins are connected to the analog I/Os, the inner pins are all connected to VMR which is at analog signal ground (+2.0V).

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5.0 Evaluating Multi-chip Designs – Daisy Chaining

Use shorting jumpers to daisy chain two or more boards. Figure 3 shows how the daisy jumpers at the edge of the board are wired and figure 4 shows how the jumpers should be placed.

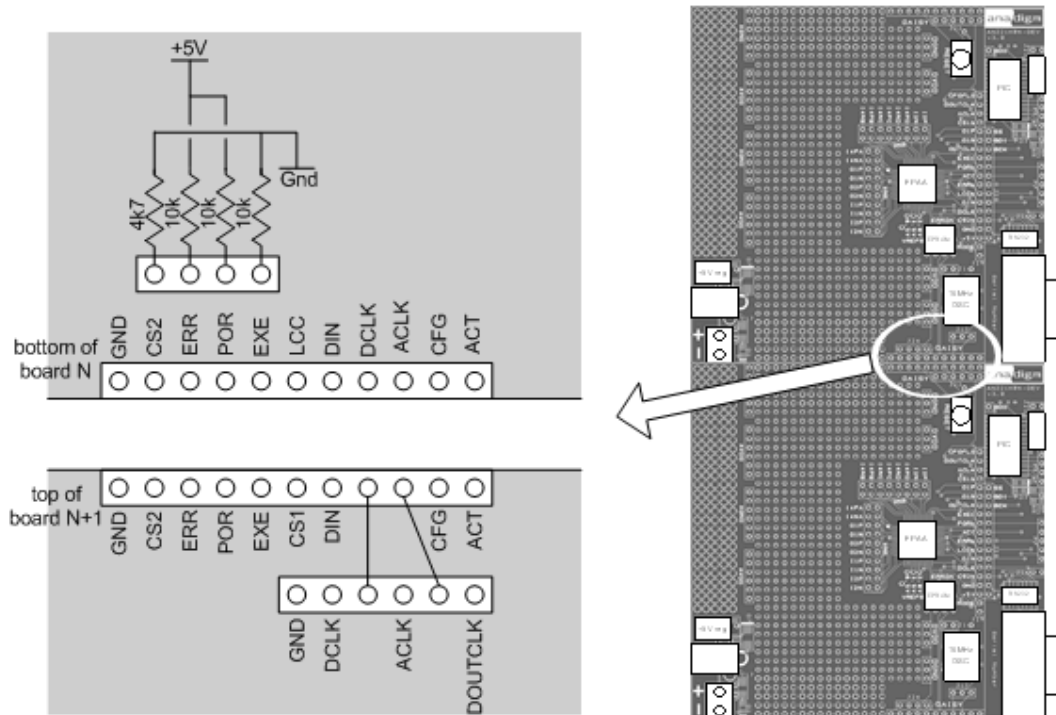


Figure 3: Position and Wiring of Daisy Jumpers

Note 1

When daisy chaining boards, each board should be powered separately using the normal supply input and with common grounds. It is good practice to make additional ground connections between boards.

Note 2

All jumpers should be removed from J17 and J18 on all boards in the chain except the last (the last board is connected to the PC serial port – see figure 5).

Note 3

The pull-ups and pull-downs described in figures 3 and 4 are required for 4 of the FPAA's digital pins. (CS2b, ERRb, PORb and EXECUTE). When chaining boards, only 1 set of pull-ups and pull-downs are required so they must be disconnected on all but one of the boards.

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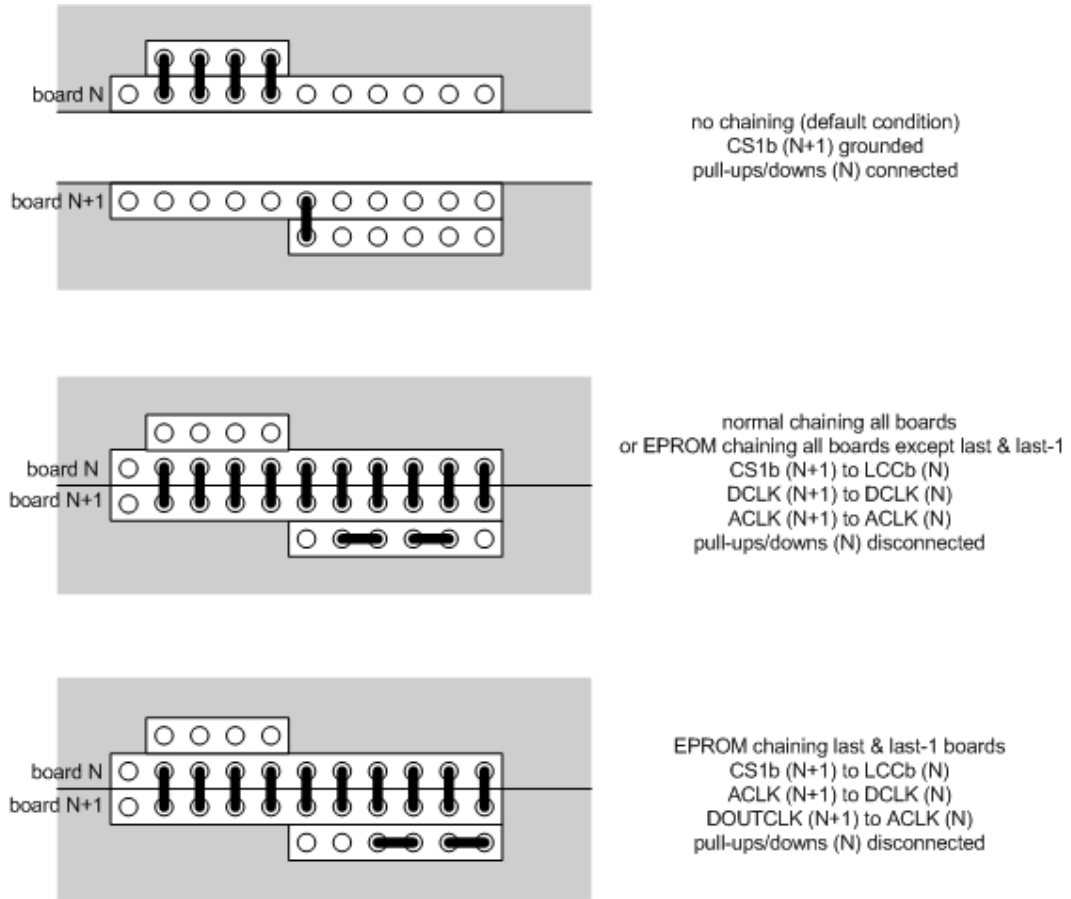


Figure 4: Jumper Settings for Daisy Chaining

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Figure 5 shows a system of 3 boards chained together with the correct jumper settings and load order as relating to the AnadigmDesigner² circuit.

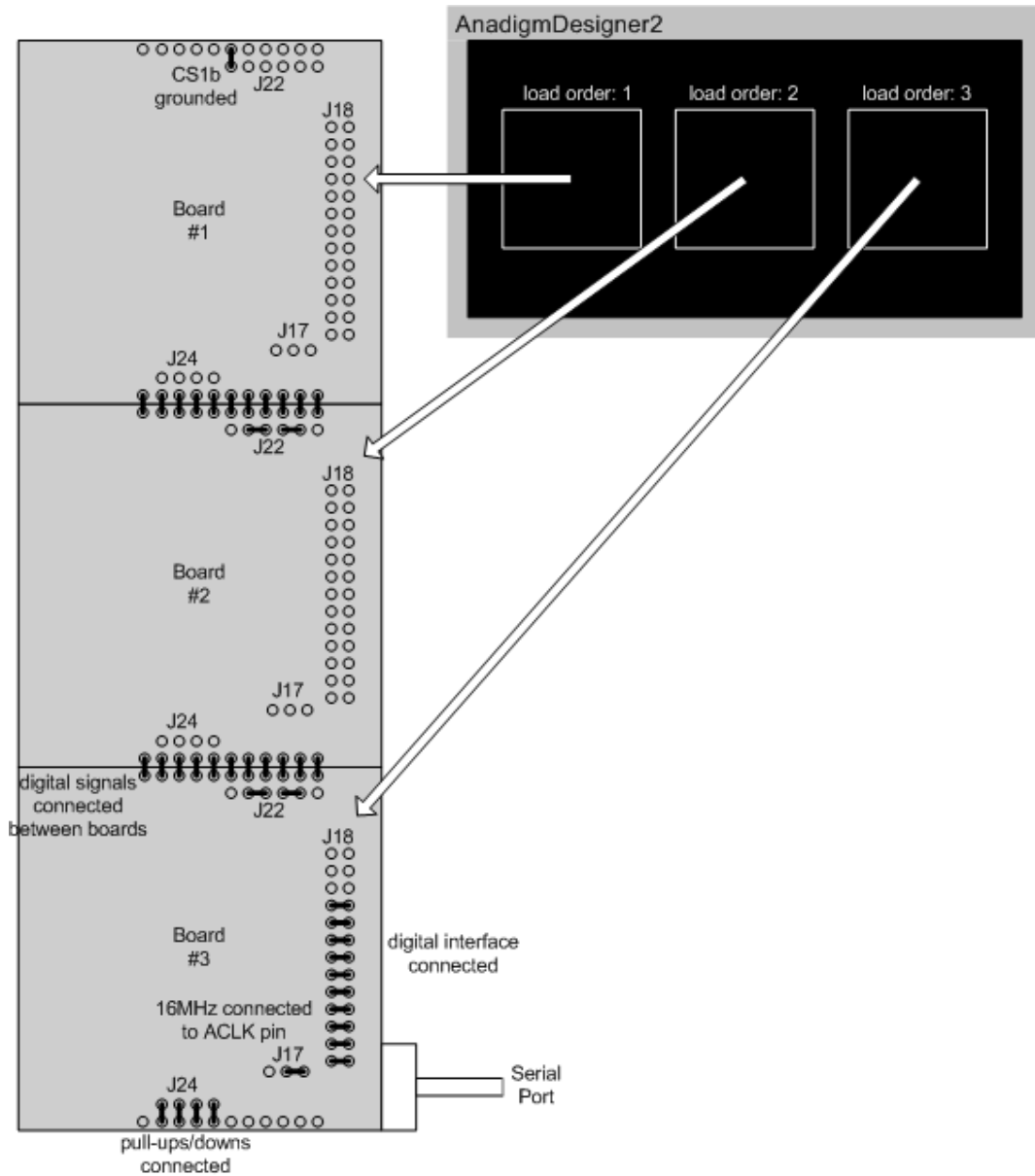


Figure 5: Jumper Settings and Load Order for 3 Chained Boards in Normal Mode

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Figure 6 shows another system of 3 boards chained together but this time configured from an EPROM.

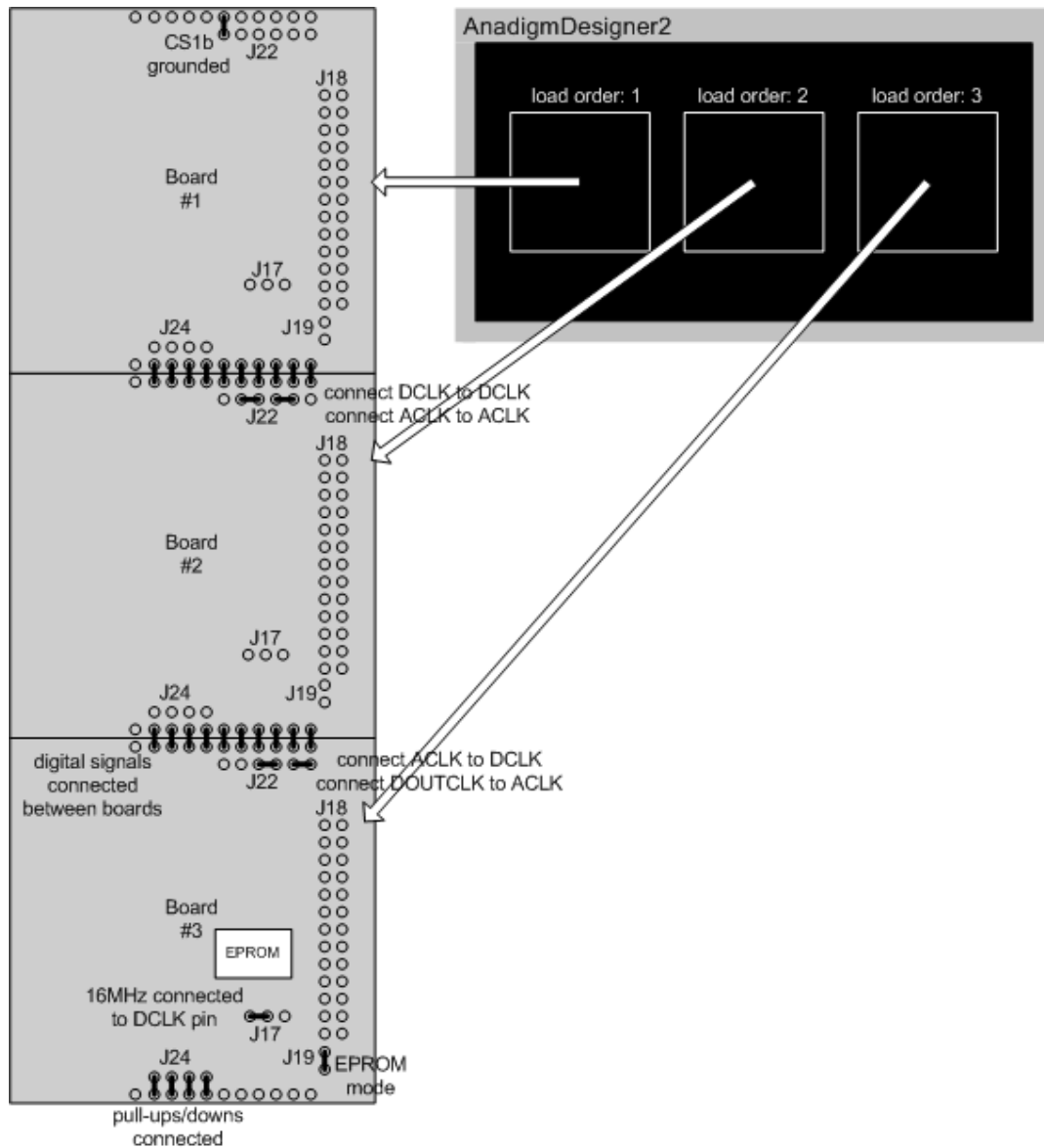


Figure 6: Jumper Settings and Load Order for 3 Chained Boards in EPROM Mode

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6.0 Other Features

V_{REF} Pins

The 3 reference pins on the FPAA device – VMR (+2.0V), VREFP (+3.5V) and VREFN (+0.5V) – have been connected via the p.c.b. tracks to the 3 holes below the FPAA. In addition, VMR is available on 2 rows of pins that are adjacent to the analog I/Os. These reference voltages are not designed to provide current.

Header Pins

All of the analog I/Os of the FPAA are brought out to header pins for easy connection. Next to these header pins is a second row of header pins connected to buffered VMR (+2V). This allows the user to connect any FPAA analog I/O to VMR using shorting jumpers, resistor jumpers or capacitor jumpers.

EPROM

There is an SPI EEPROM socket on the board. To put the board into EPROM mode:

1. Put a jumper onto J19 which sits right next to the EPROM socket, and
2. Pull all of the jumpers from the digital interface J18.

In EPROM mode the 16MHz oscillator module drives the DCLK pin of the FPAA instead of the ACLK pin as normal (when daisy chaining boards, this only applies to the first board in the chain). Putting the jumper J17 in the left position allows the 16MHz oscillator module to drive the DCLK pin.

Reset Button

There is a reset button above the FPAA. This resets both the FPAA and the PIC (digital section). In EPROM mode, press the reset button to load the circuit from the EPROM into the FPAA.

Digital Section

The digital section of the evaluation board is provided only so that there is a convenient (serial) interface from the board to a PC to enable direct configuration of the FPAA from AnadigmDesigner^{®2}, normal use of the FPAA does not require this digital interface, the FPAA can be programmed directly from an SPI interface. It is convenient when first developing an analog circuit within the FPAA to have the direct interface to AnadigmDesigner^{®2}, when the circuit(s) are implemented into a final design either a host uP (or DSP) or an EEPROM is normally used to store and configure the FPAA.

The digital section of the board consists of a RS-232 transceiver, a PIC microcontroller (to perform serial ASCII to bit conversion),. It also includes a green LED (to indicate successful configuration), and a red LED (to indicate failed configuration)

The digital section sits along the right side of the board and is connected to the rest of the board by a set of jumpers J18. It is possible to cut away the digital section to leave a purely analog board with header pins on the edge to provide an external digital interface.

If the digital section of the development board is removed or ignored (by pulling jumpers J18), the FPAA can be configured directly using any processor with an SPI interface (or port configured with appropriate signals) by connecting signals directly to the FPAA side of J18. Fully dynamic control of the FPAA's analog circuitry can be realised under software control via this connection.

Note

Anadigm[®] does not recommend any specific processor/controllers – our products work with most processors.

Anadigm[®] recommends that our customers use their own processor development boards and connect via jumper 18 to Anadigm's FPAA for fully dynamic control of the FPAA, in preference to re-engineering the digital section of this development board.

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7.0 Jumpers

Table 1 shows a complete list of the jumpers on the board and figure 7 shows their positions.

Jumper	Function	Default State	Default Condition
J1	16MHz Oscillator Module Disable On – Oscillator disabled Off – Oscillator enabled	Jumper off	Oscillator enabled
J17	16MHz Oscillator Module Right position – ACLK driven by 16MHz Left position – DCLK driven by 16MHz No jumper – osc module disconnected	Jumper to right	16MHz connected to ACLK pin of FPAA
J18	Digital Interface Connects +5V, ground and digital signals between the analog and digital sections of the board. The top 3 jumpers connect the SAR ADC signals to the PIC	Bottom 10 jumpers should be populated	+5V, ground and digital signals connected between analog and digital sections. The SAR ADC signals are not connected to the PIC in the default state.
J19	EPROM Place a jumper on J19 to use the EPROM Note 1: an EPROM must be placed in the socket next to J19 as it is not provided by default. Note 2: remove all jumpers from J18 when using the EPROM. Note 3: J17 must be placed in the left position so that the DCLK pin is driven by 16MHz.	Jumper off	Not in EPROM mode
J22	Daisy chaining and CS1b to ground Note: when daisy chaining, CS1b is grounded on the first board only – see figures 10,11	Left jumper only populated	No daisy chaining and CS1b grounded
J23	Programming the PIC (factory use only)	Jumper off	Normal operating mode
J24	Daisy chaining and pull-ups/downs Note: when daisy chaining, the pull-ups/downs are connected on the last board only – see figures 10,11	All 4 jumpers populated	No daisy chaining and all pull-ups and pull-downs connected
J26	Holds the PIC in reset	Jumper off	PIC not held in reset

Table 1: Summary of Development Board Jumpers

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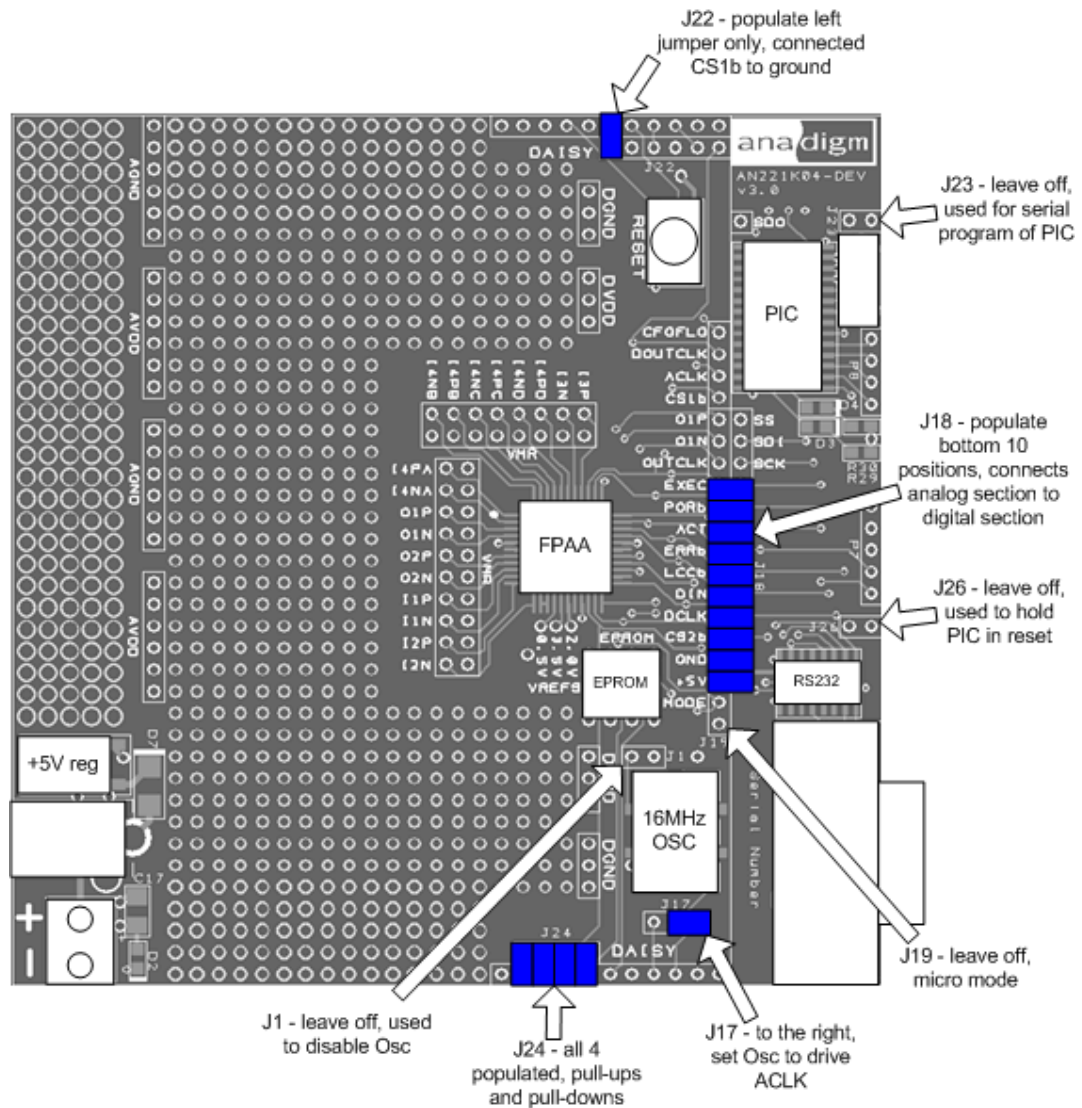


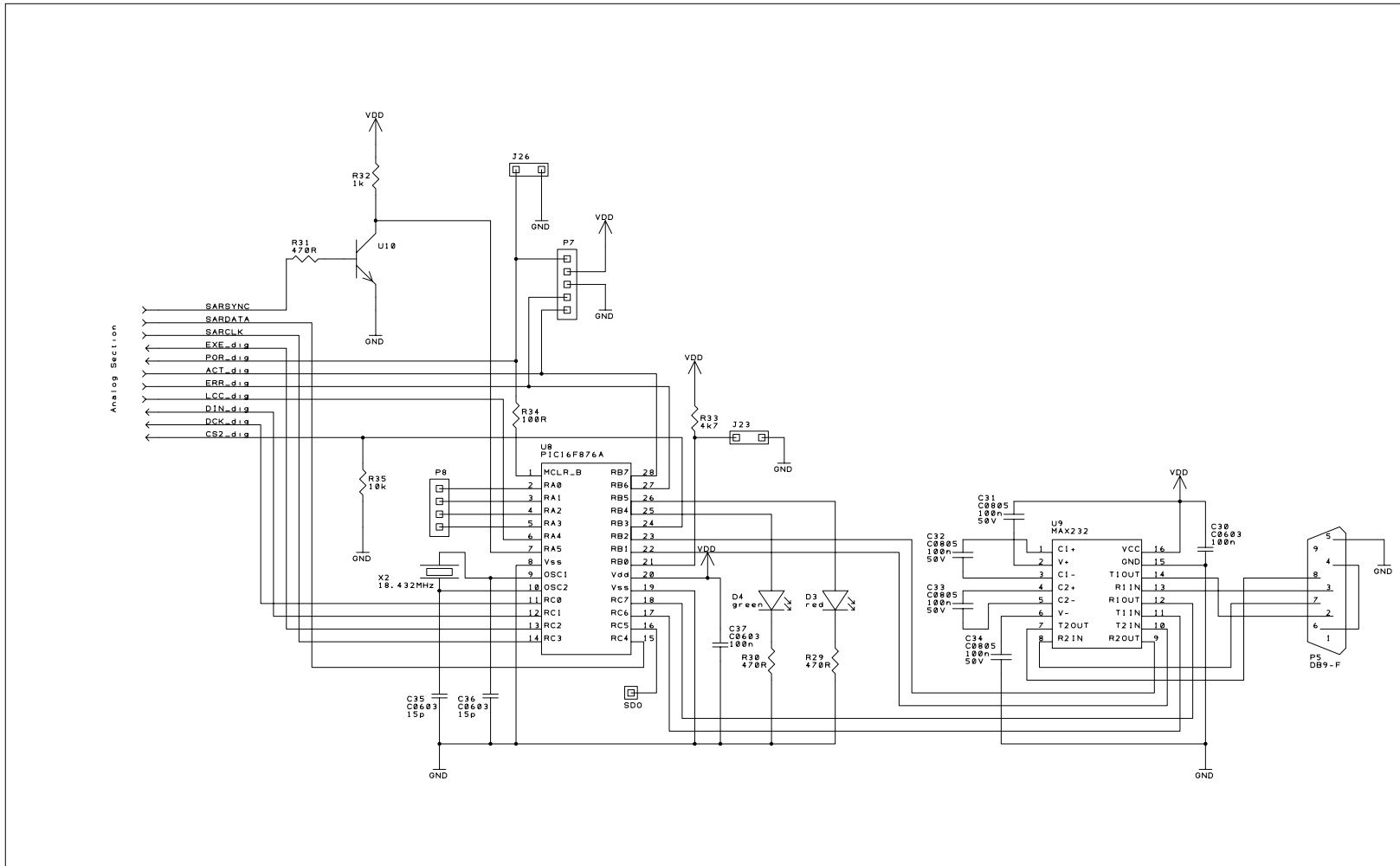
Figure 7: Positions of Jumpers and Default Settings

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8.0 Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supply 3.5mm jack socket	V_{jack}	10.5	12	20	V	DC voltage only, must be regulated Centre pole is positive, outer sleeve is ground
DC Power Supply screw terminal "+" post	V+	+5.5	+6	+10	V	DC voltage only, must be regulated Voltage is relative to "Gnd" post
DC Power Supply screw terminal "-" post	V-	-10	-6	0	V	DC voltage only, must be regulated Voltage is relative to "Gnd" post
FPAA Input Voltage	F_{in}	-0.5		+5.5	V	Direct input to FPAA on analog IO header pins or digital pins (J18)
FPAA Output Voltage	F_{out}	-0.5		+5.5	V	Direct output from FPAA on analog IO header pins or digital pins (J18)
Analog Interface Block Input Voltage	A_{in}	V-		V+	V	Power supply into screw terminal
Analog Interface Block Input Voltage	A_{in}	-4.75		$V_{\text{jack}} - 5.25$	V	Power supply into jack socket
Analog Interface Block Output Voltage	A_{out}	V-		V+	V	Power supply into screw terminal
Analog Interface Block Output Voltage	A_{out}	-4.75		$V_{\text{jack}} - 5.25$	V	Power supply into jack socket
RS-232 Input Voltage	R_{in}	-30	+/-10	+30	V	Standard RS-232 signal levels
RS-232 Output Voltage	T_{out}	-15	+/-10	+15	V	Standard RS-232 signal levels
Operating Temperature	T_{op}	10		50	°C	Ambient Operating Temperature
Storage Temperature	T_{stg}	-20		70	°C	Ambient Storage Temperature

AN231K04 – the AnadigmApex Development Board



						Anadigm AN221K04 Reference Board - Digital v3.0
					Dave Lovell July 19th 2004	

QTL2
A4

AN231K04 – the AnadigmApex Development Board

Notes:

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