RangeMaster Datasheet

Programmable Analog Signal Processor for a Universal RFID tag reader system

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RangeMaster Datasheet – Complete Solution for a Universal RFID tag reader system

PRODUCT OVERVIEW

The RangeMaster solution is based on the revolutionary analog programmable technology developed by Anadigm.

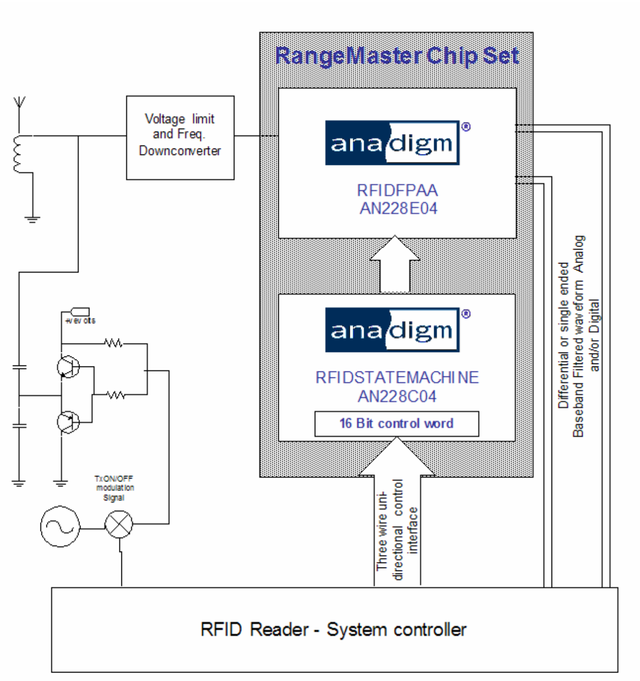
It allows for the development of a universal RFID tag reader that can read multiple tag types.

By allowing standardization around a single PCB to support multiple end products and markets, the RangeMaster promises to lower total cost of ownership and simplify product development

This solution enables customized signal processing using the system host controller. Some of the options that are user customizable are:

1. The signal processing circuit implemented in the RFID FPAA – choose between twin band-pass filter or a single wide-pass filter
2. The background frequency that is filtered out – select from 3 predefined values
3. The gain of the analog circuit – optimize the range and sensitivity of the reader
4. The upper and the lower sub carrier frequency – select from 15 predefined values
5. Digital and/or analog output

System level Overview of the RangeMaster solution



UHF CARD READER

PRODUCT FEATURES

- **Complete Solution for Universal RFID Reader**
- Full support for EPC Global Gen 1/Gen 2 (Class 0,1,2) and ISO18000-6 protocols
- User customizable signal processing – Choice of two different carrier baseband processing circuits
- Selectable sub carrier frequency
- Read range and sensitivity optimization with variable gain
- Ability to calibrate reader to filter out background interference (i.e. fluorescent lighting)
- Standby Mode for minimum power consumption
- Two-chip solution
- Supply voltage: 5v
- RFID FPAA Package: 44-pin QFP (10x10x2mm)
  - Lead pitch 0.8mm
- RFID State Machine:20-pin SSOP(5.3x7.2x1.75mm)
  - Lead pitch 0.8mm

BENEFITS

- Easy to use pre-defined Analog signal conditioning path.
- Design and maintain ONE reader than can be customized to read different tag types, with different modulation schemes and frequencies
- Dynamically change the filter frequencies and circuit architecture
- Supports transmit path signal suppression, avoid receiver saturation recovery time.
- Adjust the gain of the analog signal path to optimize for read range
- Standardize around a single PCB to support multiple end products and markets
- Calibrate the reader at customer site – to account for background interference
- Reduce the total number of system components and lower bill of materials cost

ORDERING CODE

The RangeMaster Chip set is sold in pairs of devices either in trays and tubes or in Tape And Reel format. Both devices will be available only in lead-free, green ROHS compliant material. Lead finish Matt tin (Sn).

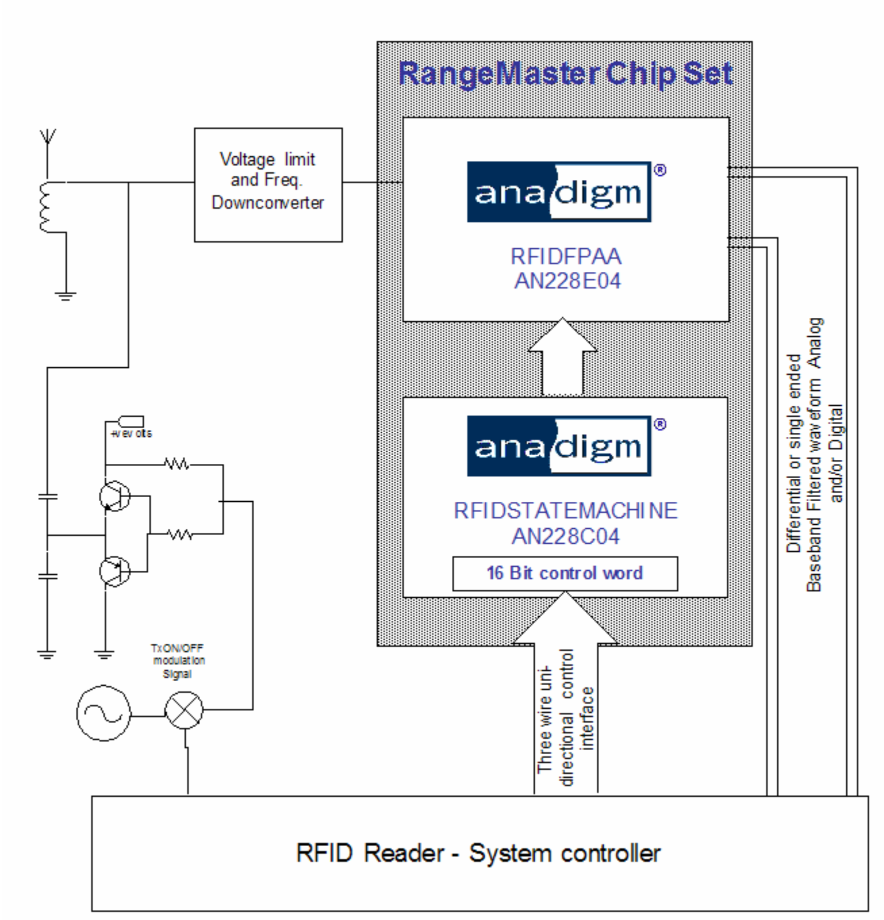
- AN228K04-SETSP (chipset pair) consists of :-
  - AN228E04-QFPTY (96/Tray)
  - AN228C04-SSOTY (66/Tube, 924/box)
- AN228K04-SETTR (chipset pair) consists of :-
  - AN228E04-QFPTR (1000/Tape & Reel)
  - AN228C04-SSOTR (1000/Tape & Reel)

RangeMaster Evaluation board

- AN228K04-EVAL1

[*For more detailed information on the features of the RangeMaster solution, please contact Anadigm Technical Support, support@anadigm.com*]

1. INTRODUCTION - ANALOG SIGNAL PROCESSING



UHF CARD READER

The RangeMaster chip set consists of an RFID FPAA integrated circuit and a RFID State Machine Circuit, together the devices offer sufficient flexibility to cover the Analog sub-carrier signal conditioning for a universal RFID reader unit.

RFID FPAA, is a variant of Anadigm's Field Programmable Analog Array, SRAM based programmable Analog circuitry.
RFID State Machine is a controller with the knowledge embedded to allow it to re-configure the RFID FPAA with one of two basic circuits, each of which has multiple programmable attributes, the user is exposed to the control of these circuit variations via a simple 16 bit control word within the RFID State Machine, which is written and re-written via a 3 wire (SPI compatible) interface.
The input signal to the RFID FPAA is ideally an ac coupled differential signal, however an ac coupled single ended signal can also be accommodated.
The RangeMaster solution lets users select between two analog signal processing circuits:

- the universal baseband processing circuit, (see section 1.1, Fig 1) and
- the EPC Gen2 baseband processing circuit (see section 1.2, Fig 2)

The signal path within the RFID FPAA is fully differential, both gain and filter corner frequencies are variable in each circuit.
Within the "RFID_wide" signal path there is an additional optional narrowband Notch filter with four preset center frequencies. Within the "RFID_twin" signal path the mixer element has variable gain in each input branch, three preset gain boosts are preconfigured for the lower frequency signal path (0,3 and 6dB), this allows for signal amplitude balancing before the summing stage.
Both signal paths offer a fully differential analog output signal, this can also be used single-ended in which case the signal has half the amplitude and a +2volt dc bias. Similarly both circuits paths offer a digital output, this is the result of feeding the analog signal through a comparator with differential hysterisis thresholds set to +/-570mV, the digital output is available as a complimentary pair (inverted or non-inverted).

The RangeMaster output signal requires the final stage of decoding to be performed in a "system controller" unit, extracting the data bit stream. Decoding of the FSK (or other encoding) from the digital output is a simple matter of timing sequential edges, final decode of the Analog bit stream can be more sophisticated and include special information (amplitude).

1.1 Universal Baseband Processing Circuit (RFID_wide).

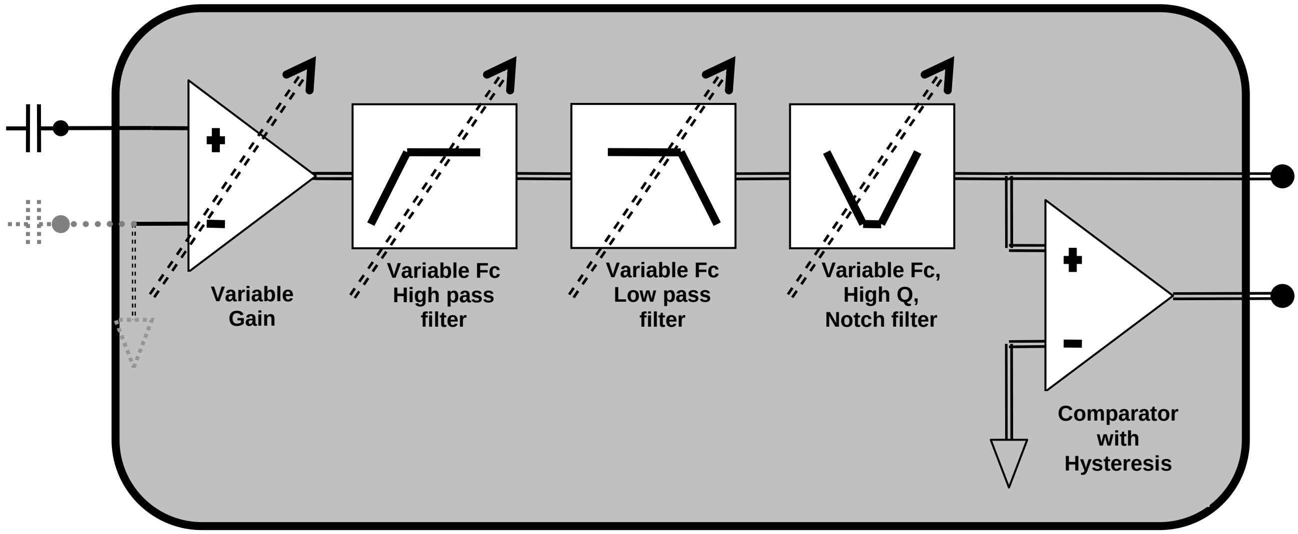


Fig 1: Universal analog baseband processing circuit

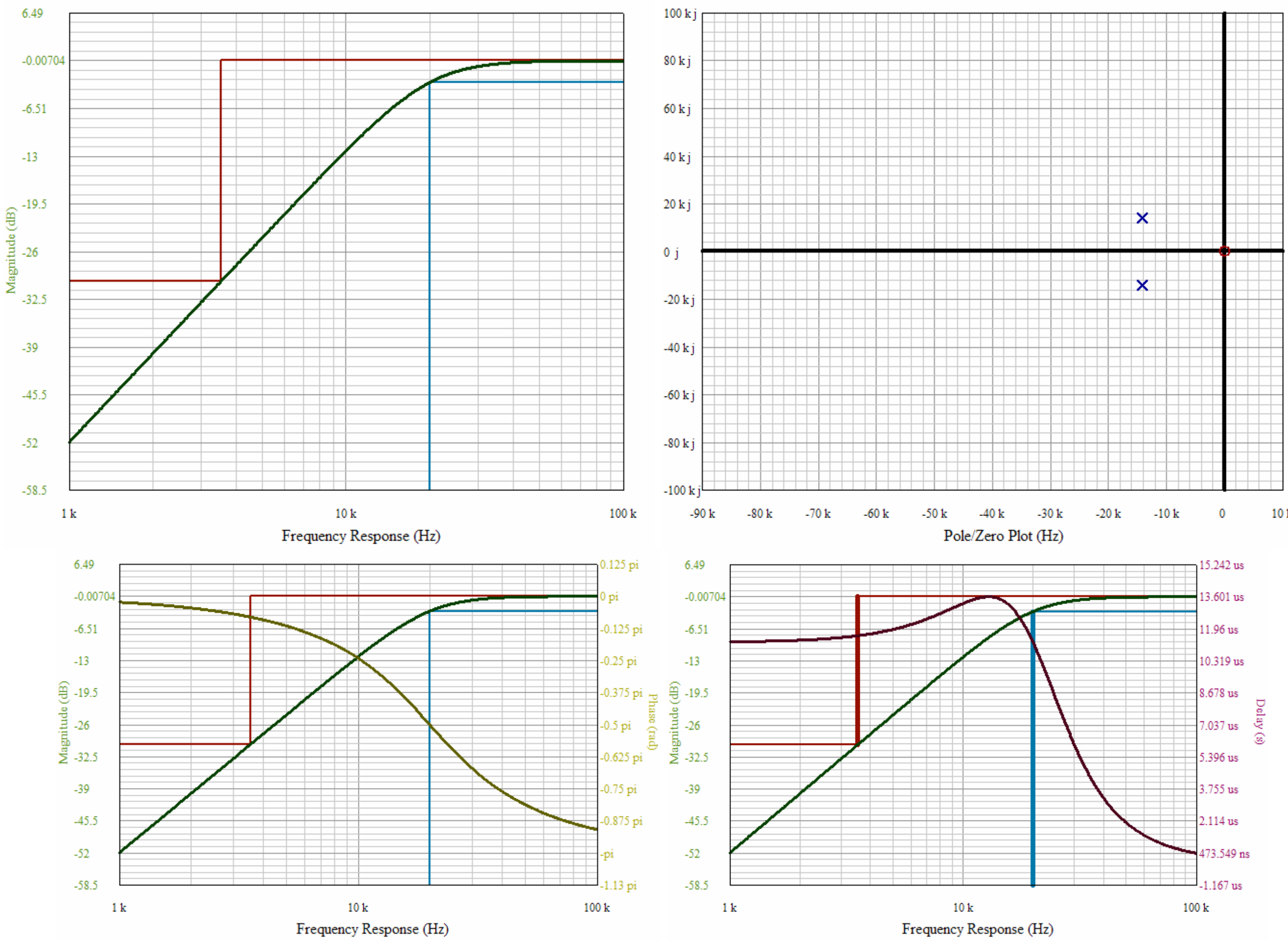
The universal circuit enables the extraction of all data frequencies (DC to 640kHz). It also features a user selectable notch filter for rejecting background interference (i.e. fluorescent lighting).

Gain stage	Gain (dB)	Gain	Tolerance	Comment
	0	1.00	0.10%	Inverting differential gain stage, See Note 2.
	6	2.00	0.18%	
	12	3.98	0.50%	
	18	7.94	1.45%	
	24	15.85	1.89%	
	30	31.62	3.03%	
Highpass filter	Fc (-3dB point, kHz)		Tolerance	Comment
	2, 4, 8,16 20, 32, 40, 64 80, 128, 160, 256 320, 640, 3300 Note1		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1 Quality factor = 0.707 Inverting architecture
Lowpass filter	Fc (-3dB point, kHz)			
	1, 2, 4, 8 16, 20, 32, 40 64, 80, 128, 160, 256, 320, 2200Note1		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1 Quality factor = 0.707 Inverting architecture
Notch filter	Fc (Notch center point, kHz)			
	0 (not in circuit) 50, 52, 54		Better than 1%	2nd Order Biquadratic Quality Factor = 20 Gain's 1.00. Inverting architecture
Comparator	Hysterisis	570mV	10%	Complimentary outputs available
See graphical data for filter response details (Next page).				

Notes

1) The upper most frequency pair (2200 kHz and 3300 kHz) do not apply to this circuit, this setting in the control word is not allowed, if used may result in a non functional circuit.

High pass filter, Chipset default setting 20 kHz.



At 20kHz, (default setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	20kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	3.55 kHz
Actual Corner Frequency	19.98kHz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (88752.2-88752.2j))·(S + (88752.2+88752.2j))]		

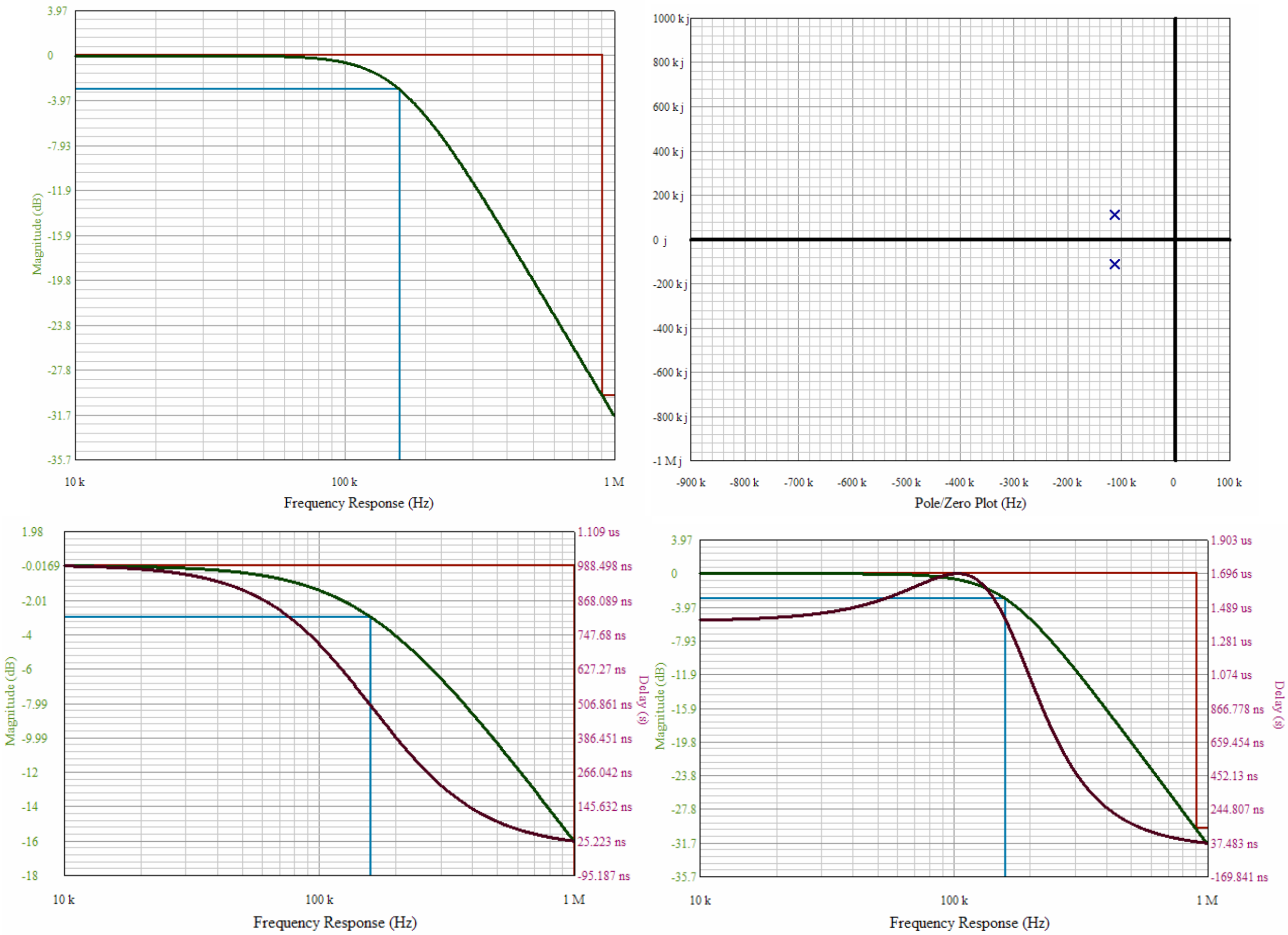
At 320kHz (maximum setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	320 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	56.5 kHz
Actual Corner Frequency	319.6 kHz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (1.42004e+006-1.42004e+006j))·(S + (1.42004e+006+1.42004e+006j))]		

At 1kHz (mimimum setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	1 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	177 Hz
Actual Corner Frequency	998.8 kHz		
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S)·(S) / [(S + (4437.61-4437.61j))·(S + (4437.61+4437.61j))]		

Low pass filter, chipset default setting 160 kHz.



At 160kHz (default setting)

Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	160 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	905 kHz
Actual Corner Frequency	160.2 kHz		
Filter Transfer Function (Pole/Zero Form)	1.01305e+012 **/** [(S + (711706-711706j))·(S + (711706+711706j))]		

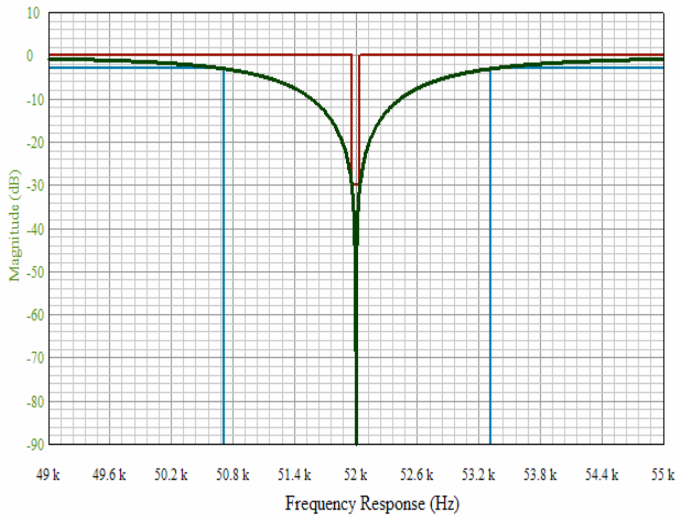
At 640 kHz

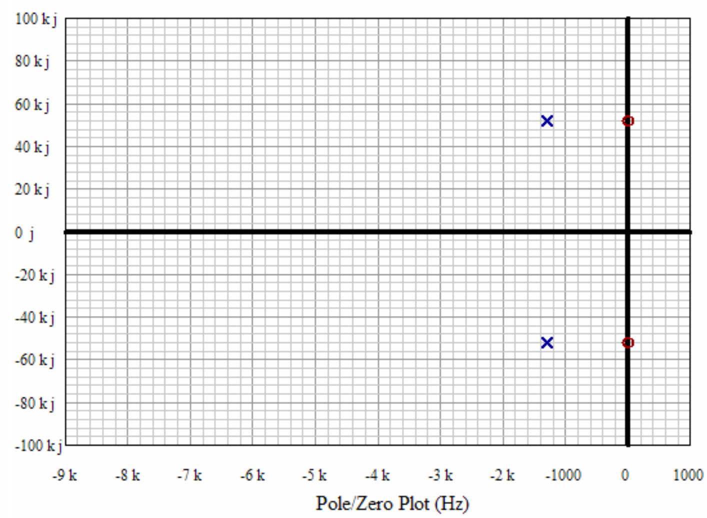
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	640 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	3.62 MHz
Actual Corner Frequency	640.8 kHz		
Filter Transfer Function (Pole/Zero Form)	1.62088e+013 **/** [((S + (2.84682e+006-2.84682e+006j))·(S + (2.84682e+006+2.84682e+006j)))]		

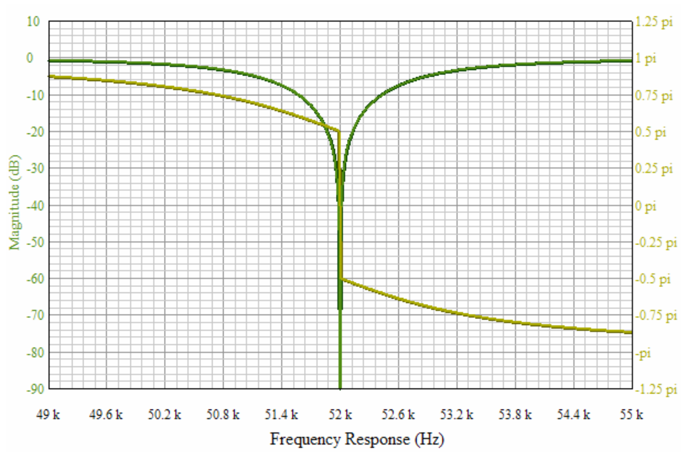
At 2 kHz

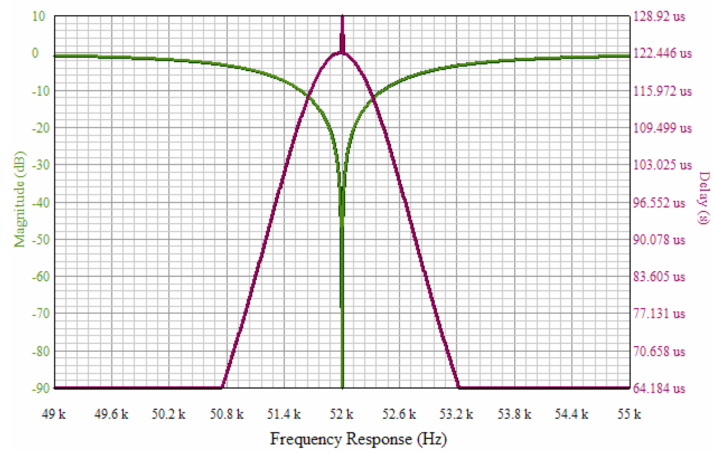
Filter Parameters			
Passband Gain	0 dB	Pass Band Frequency	2.00 kHz
Stop Band Attenuation	30 dB	Stop Band Frequency	11.3 kHz
Actual Corner Frequency	2.00 kHz		
Filter Transfer Function (Pole/Zero Form)	1.58289e+008 **/** [(S + (8896.32-8896.32j))·(S + (8896.32+8896.32j))]		

Notch filter,   Fc = 52 kHz









At 52 kHz (default setting)

Filter Parameters			
Passband Gain	0 dB	Center Frequency	52 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	52 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 326726j)·(S + 326726j) **/** [(S + (8180.11-326623j))·(S + (8180.11+326623j))]		

At 54 kHz

Filter Parameters			
Passband Gain	0 dB	Center Frequency	54 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	54 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 339292j)·(S + 339292j) / [(S + (8180.11-339193j))·(S + (8180.11+339193j))]		

At 50 kHz

Filter Parameters			
Passband Gain	0 dB	Center Frequency	50 kHz
Stop Band Attenuation	30 dB	Pass Band Width	2.61 kHz
Actual Center Frequency	50 kHz	Stop Band Width	70 Hz
Filter Transfer Function (Pole/Zero Form)	1.00238 · (S - 314159j)·(S + 314159j) / [(S + (8180.11-314053j))·(S + (8180.11+314053j))]		

1.2 EPC Gen2 baseband processing circuit (RFID_twin)

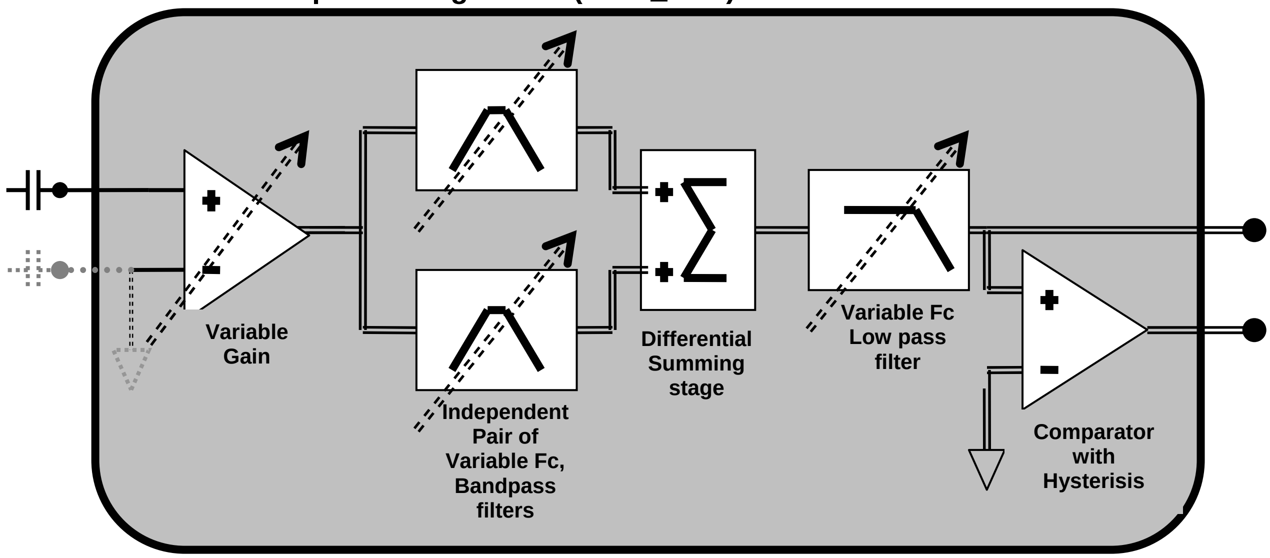


Fig 2: EPC Gen 2 analog baseband processing circuit

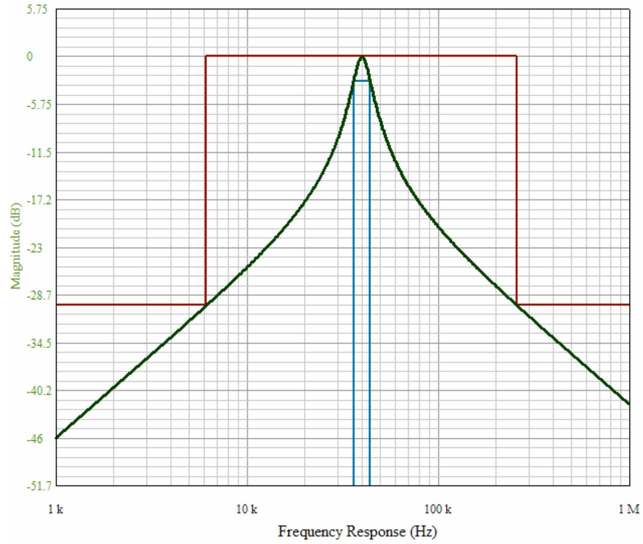
The EPC Gen 2 circuit enables the extraction of all data frequency pairs i.e. 2KHz & 4KHz, 32KHz & 64KHz, 320KHz & 640KHz. This circuit also supports extraction of data at 2.2MHz/3.3MHz for Class 0 operation.
The universal circuit enables the extraction of all data frequencies (DC to 640 KHz).
It also features a user selectable notch filter for rejecting background interference (i.e. fluorescent lighting).

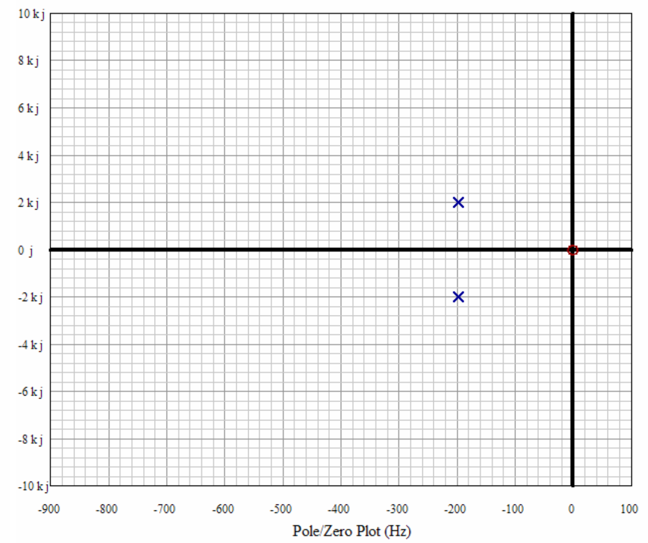
Gain stage	Gain (dB)	Gain	Tolerance	Comment
	0	1.00	0.10%	Inverting differential gain stage
	6	2.00	0.18%	
	12	3.98	0.50%	
	18	7.94	1.45%	
	24	15.85	1.89%	
	30	31.62	3.03%	
High bandpass filter	Fc (Center Frequency, kHz)			
	2, 4, 8 ,16, 20, 32, 40, 64, 80, 128, 160, 256, 320, 640, 3300 (Note3)		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1, Qf = 1.0
Low bandpass filter	Fc (Center Frequency, kHz)			
	1, 2, 4, 8, 16, 20, 32, 40 64, 80, 128, 160, 256, 320, 2200 (Note3)		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1, Qf = 1.0
Summing stage	Gain			
	Upper input branch Lower input branch	1.00 1.00 (0dB) 1.41(+3dB) 2.00(+6dB)	Better than 1% Better than 1% Default is +3dB	
Low pass filter	Fc (corner frequency) Note2	1.5kHz to 930kHz Note2	Better than 1%	1st order Bilinear. Fc is -6dB amplitude w.r.t zero dB passband.
Comparator	Hysterisis	570mV	10%	Complimentary outputs available
See graphical data for filter response details (Next page).				

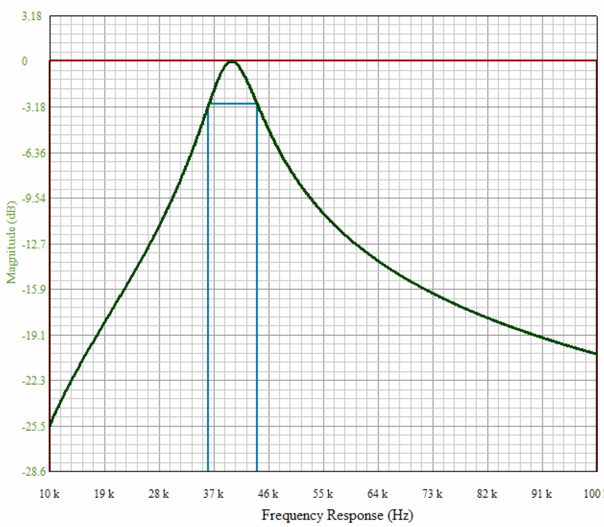
Notes
2. The corner frequency of this filter is set to be 50% higher than the frequency of the higher of the two bandpass filters.
3. When using the upper most frequency pair (2200 kHz and 3300 kHz), the input gain stage is removed from the circuit, thus the circuit gains are fixed at unity

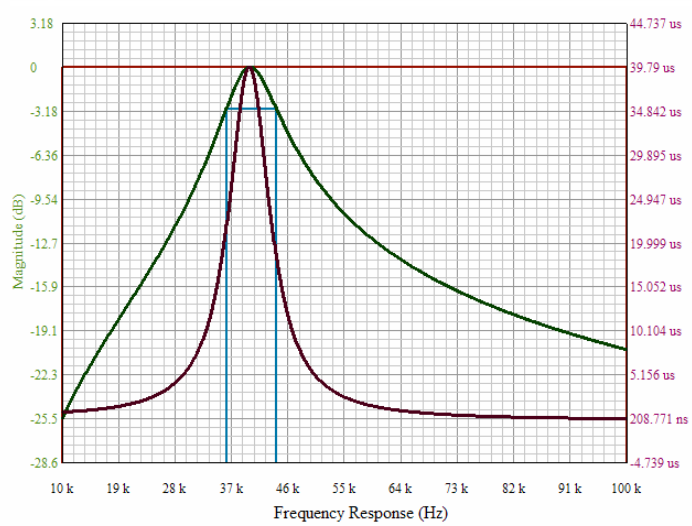
Bandpass filter characteristics, these apply to either the “high” or “low” bandpass filter, each has the same filter architecture and performance.

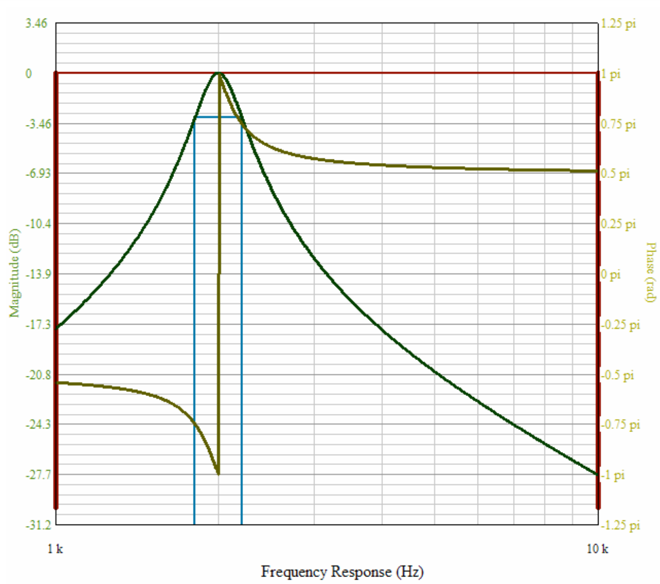
<u>40kHz, Bandpass filter.</u>





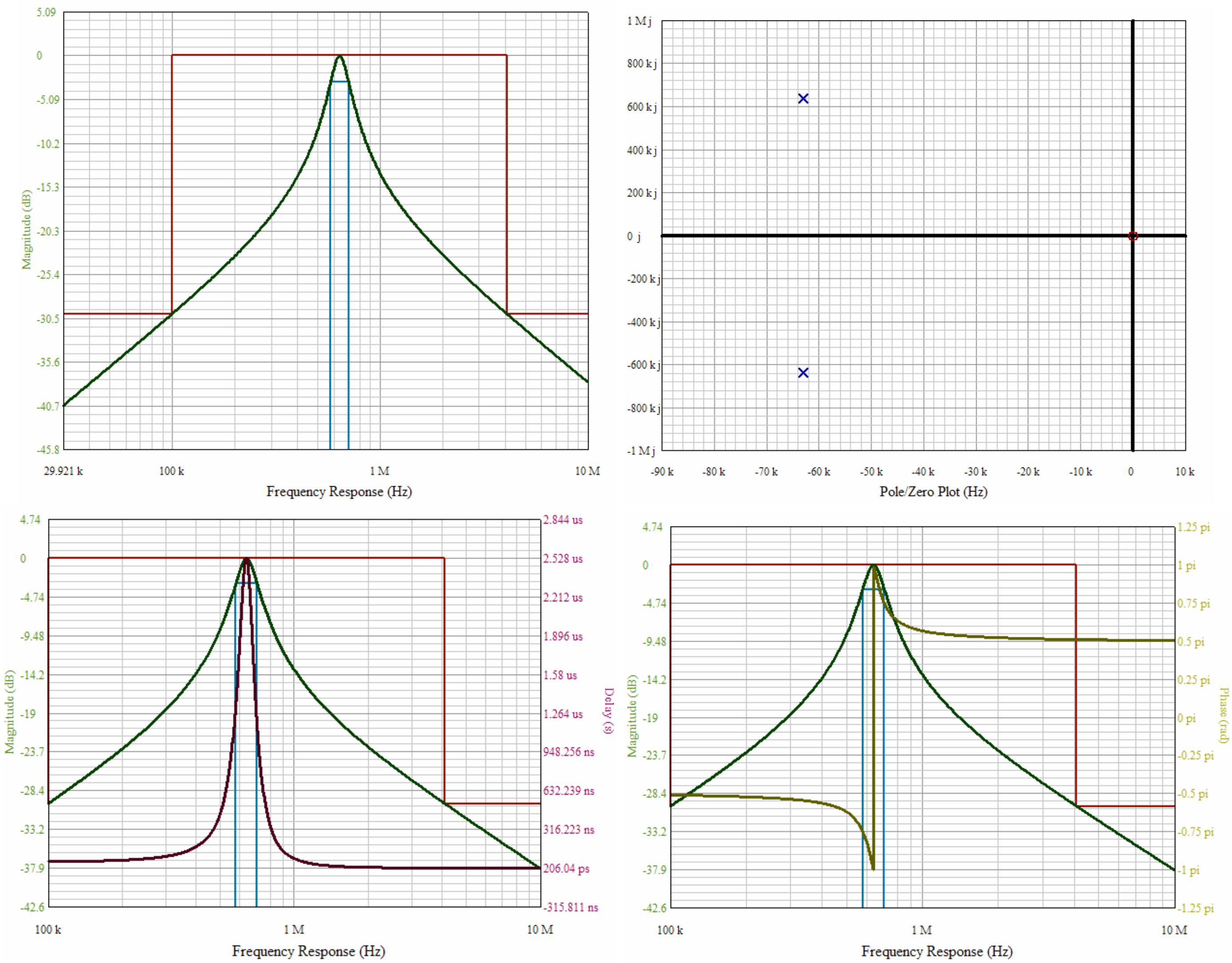






Filter Parameters	
Passband Gain	0 dB
Center Frequency	40 kHz
Stop Band Attenuation	30 dB
Pass Band Width	8 kHz
Stop Band Width	254 kHz
Quality Factor	4.99
Filter Transfer Function - (Pole/Zero Form) <u>50385 · (S)</u> [(S + (25192.5-250062j))·(S + (25192.5+250062j))]	

640kHz, Bandpass filter.

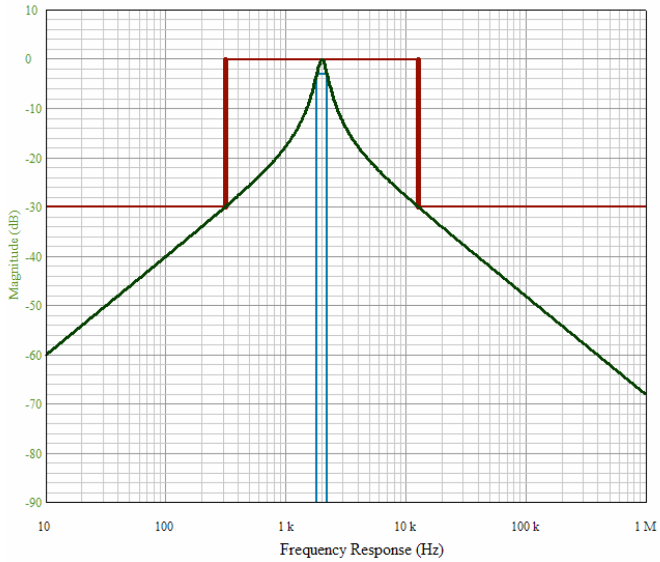


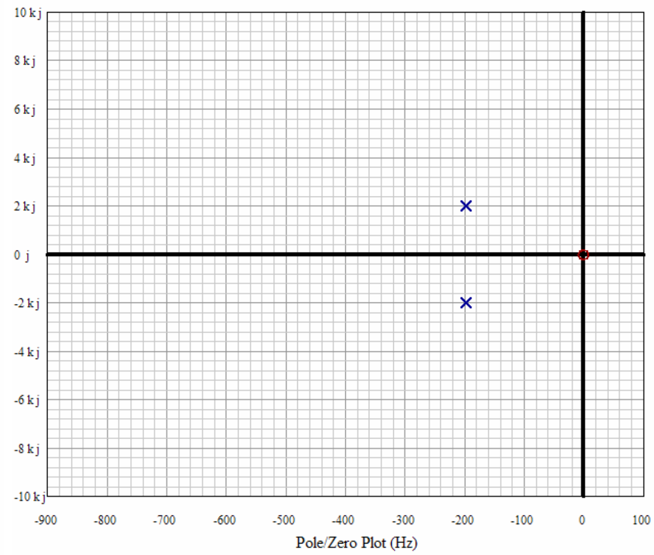
Filter Parameters	
Passband Gain	0 dB
Center Frequency	640 kHz
Stop Band Attenuation	30 dB
Pass Band Width	128 kHz
Stop Band Width	4 MHz
Quality Factor	5.07

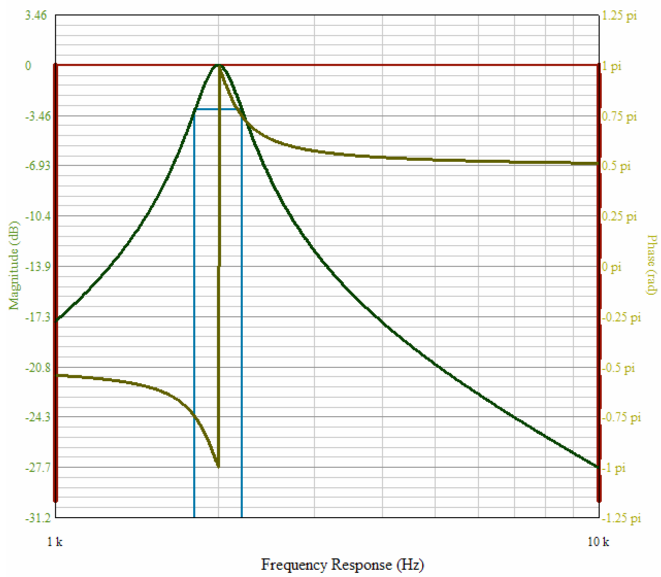
Filter Transfer Function - (Pole/Zero Form)

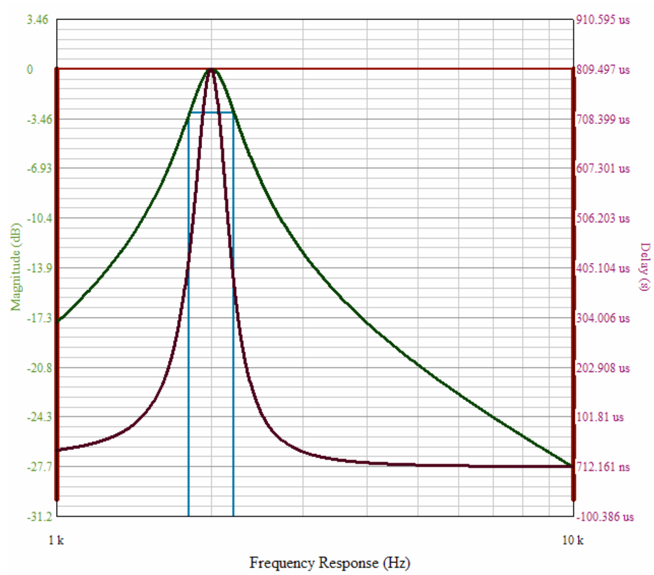
$$\frac{792442 \cdot (S)}{[(S + (396221-4.00167e+006j))\cdot(S + (396221+4.00167e+006j))]}$$

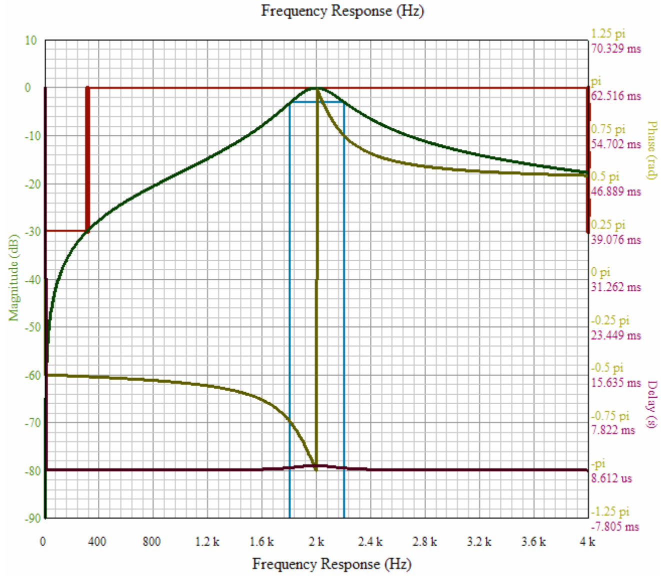
2kHz, Bandpass filter











Filter Parameters	
Passband Gain	0 dB
Center Frequency	2 kHz
Stop Band Attenuation	30 dB
Pass Band Width	400 Hz
Stop Band Width	12.5 kHz
Quality Factor	5.07

Filter Transfer Function - (Pole/Zero Form)

$$\frac{2476.38 \cdot (S)}{[(S + (1238.19-12505.2j))\cdot(S + (1238.19+12505.2j))]}$$

1.2.1 2.2MHz and 3.3MHz signal processing circuit (RFID_fast)

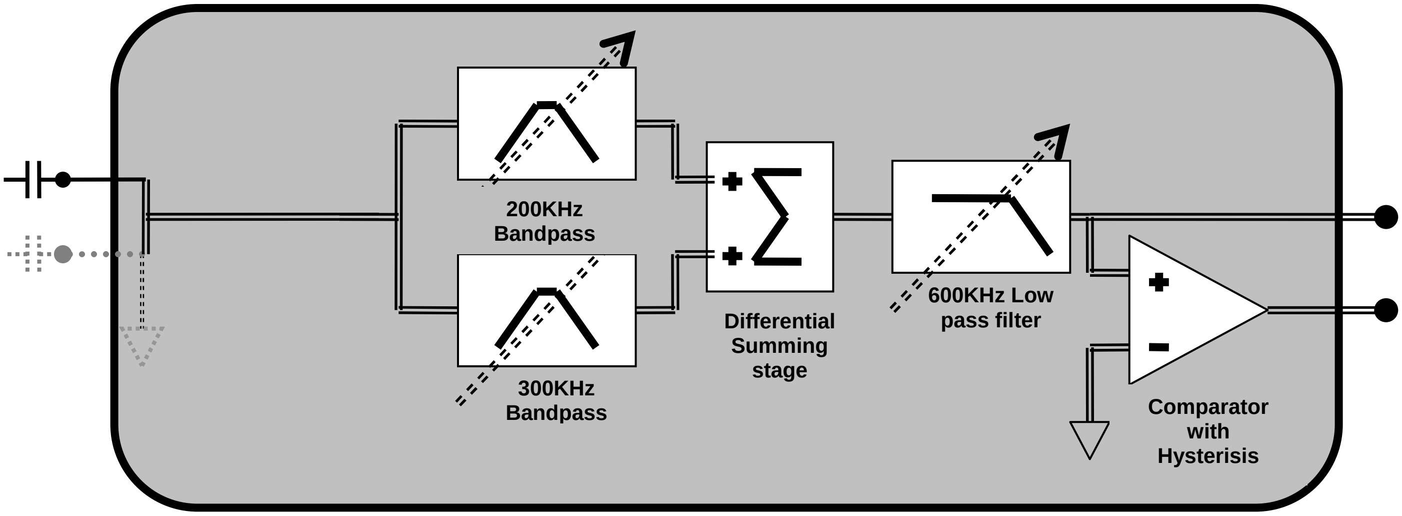
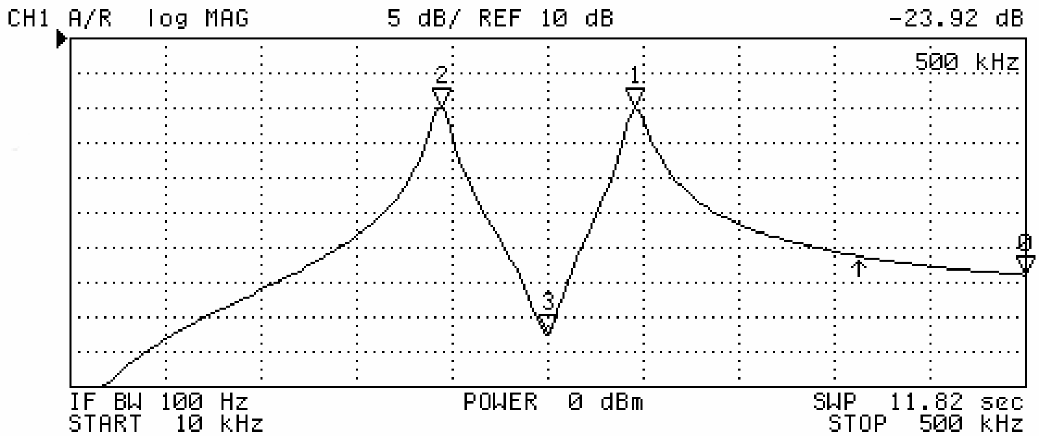


Fig 3: EPC Gen 2 analog baseband processing circuit

This circuit is specifically designed to filter and extract data from input sub-carrier signals at 2.2MHz/3.3MHz.
The operation of this circuit depends upon under-sampling of the input signal; therefore approximately 8 cycles of the sub carrier are required before a good quality signal is obtained. The two bandpass filters sample the input signal at 2MHz and 3MHz respectively and thus fold the 2.2 and 3.3MHz signal back to 200 and 300 kHz respectively.

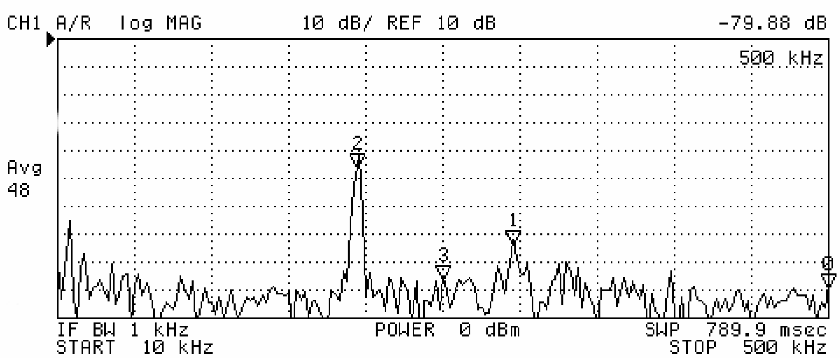
High bandpass filter	Fc (Center Frequency. kHz)			
	300.0		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1, Qf = 30
Low bandpass filter	Fc (Center Frequency, kHz)			
	200.0		Better than 1%	2nd Order Biquadratic, Butterworth approximation Highpass Gain=1, Qf = 20
Summing stage				
	Upper input branch (300KHz) Lower input branch	1.15 1.05	Better than 1% Better than 1%	
Low pass filter				
	Fc (corner frequency)	600kHz	Better than 5%	1st order Bilinear. Fc is -6dB amplitude w.r.t zero dB passband.
Comparator				
	Hysterisis	570mV	10%	Complimentary outputs available
See graphical date for filter response details (Next page).				

Signal path filter Characteristics at the summer output, before the 600kHz low pass.



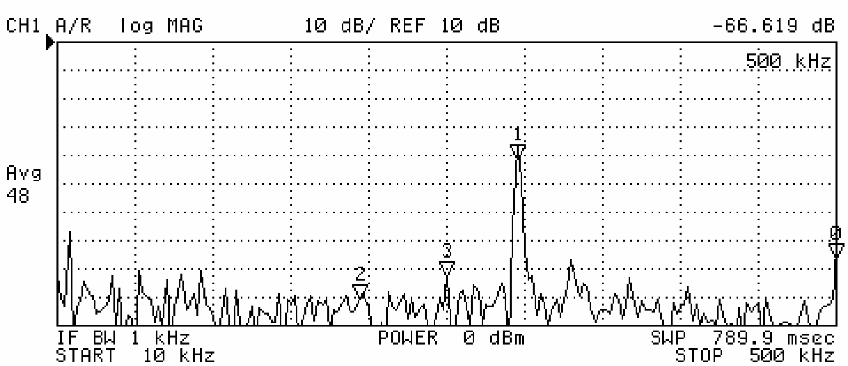
N	SWP PARAM	VAL
0	500 kHz	-23.92 dB
1	300.08 kHz	-.1495 dB
2	199.9975 kHz	.0455 dB
3	254.755 kHz	-32.415 dB

Spectrum response to a single 200 kHz input signal - Approx 30dB selectivity



N	SWP PARAM	VAL
0	500 kHz	-79.88 dB
1	300.08 kHz	-64.539 dB
2	199.9975 kHz	-37.117 dB
3	254.755 kHz	-76.876 dB

Spectrum response to a single 300 kHz input signal - Approx 30dB selectivity



N	SWP PARAM	VAL
0	500 kHz	-66.619 dB
1	300.08 kHz	-31.596 dB
2	199.9975 kHz	-81.496 dB
3	254.755 kHz	-73.275 dB

The exact circuit configuration which is active within the RFID FPAA is defined by the content of the 16 bit control word, within the AN228C04 State Machine.

ANADIGM RangeMaster Control Interface (16 Bit Control Byte)

anti-saturation control bit	Select circuit	EXECUTE Set Trigger	Notch filter center frequency		Gain control			Lower subcarrier frequency (this sets lower bandpass or Highpass filter)				Upper subcarrier frequency (this sets the upper bandpass or Lowpass filter)			
A1	**A2**	**X**	**B1**	**B2**	**G1**	**G2**	**G3**	**LF1**	**LF2**	**LF3**	**LF4**	**HF1**	**HF2**	**HF3**	**HF4**
0 = input off 1 = input on	0 = twin bandpass 1 = wideband filter	1 Sets trigger, Rising edge of external RFID FPAA implements	B1,B2	Freq (kHz)	G1,G2,G3		Gain	LF1,LF2,LF3,LF4		Freq (KHz)		HF1,HF2,HF3.HF4		Freq (KHz)	
			00	*Note8*	000		0dB	0000		-	Note4	0000		-	Note4
			01	50.0	001		+6dB	0001		1		0001		2	
			10	52.0	010		+12dB	0010		2		0010		4	
			11	54.0	011		+18dB	0011		4		0011		8	
					100		+24dB	0100		8		0100		16	
					101		+30dB	0101		16		0101		20	
					110		*Note5*	0110		20		0110		32	
					111		*Note6*	0111		32		0111		40	
								1000		40		1000		64	
								1001		64		1001		80	
								1010		80		1010		128	
								1011		128		1011		160	
								1100		160		1100		256	
								1101		256		1101		320	
								1110		320		1110		640	
								1111		2200	Note7	1111		3300	Note7

Notes

4 Control word 0000000000000000(binary), 0x00, 0x00 (Hex) sets the chipset into standby (low power mode)

5 Nominal gain = 0dB. +3dB higher gain for Lower bandpass v.s. higher bandpass

6 Nominal gain = 0dB. +6dB higher gain for Lower bandpass v.s. higher bandpass

7 "Class0", 2.2/3.3MHz Gain = 0dB. No gain control - Fixed circuit

8 The notch filter is removed from the signal path.

Examples

000 00 000 0000 0000	Input off Twin circuit No Trigger	Circuit Gain = 0dB	Note 4, Special case, circuit in power down mode.	
100 10 010 1000 1001	Input on Twin circuit No Trigger	Notch filter Not applicable in twin circuit Circuit Gain = +12dB	Lower bandpass filter center frequency 40KHz	Higher bandpass filter center frequency 80KHz
110 10 010 1000 1001	Input on Wideband circuit, No Trigger	Notch filter center frequency set to 52kHz Circuit Gain = +12dB	Highpass filter corner frequency 40KHz	Lowpass filter corner frequency 80KHz

INTERFACE BETWEEN SYSTEM CONTROLLER AND RFID STATE MACHINE

RangeMaster 16-bit Control Word - Input Specification

Introduction
This Section describes the interface used by RangeMaster to input the 16-bit control word.

Functional Description
The interface for inputting the 16-bit control word to the RangeMaster chipset is a 3-pin SPI type interface. The control word is entered as 2 bytes, the most significant byte first, each byte with the most significant bit first. An active low select signal is used to tell the interface to expect each byte. The interface must be deselected between the 2 bytes for a minimum period given in the timings below. The interface expects to receive 2 bytes and will hang until it sees the second byte. The user must ensure that 2 bytes are entered every time the control word is to be changed.

Hardware
Table 1 shows the pins used by this interface.

Pin name	Pin type	Description
SSb	Input	Slave select
SCK	Input	Serial clock
SDI	Input	Serial data in

Timings
Table 2 and figure 4 show the timings specifications.

Symbol	Description	Min	units
T1	SSb falling to SCK rising	500	ns
T2	SSb rising after SCK falling	790	ns
T3	SSb high period Note9	6.5	**us**
T4	SDI setup to SCK rising	100	ns
T5	SDI hold after SCK rising	100	ns
T6	SCK low period	520	ns
T7	SCK high period	520	ns

Notes
9. this is the minimum high period for SSb between the 2 bytes of the control word. There is no maximum time for this. The interface will wait indefinitely for the second byte before the software can continue.

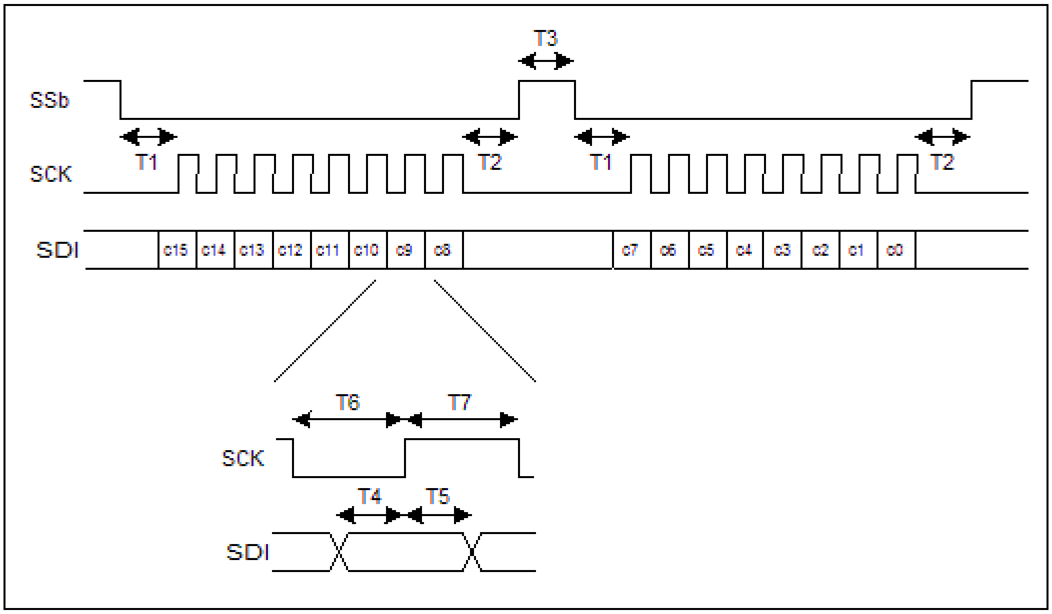


Figure 4: Control word input timings

Special functions - additional timing information

Standby and Wake-up

Standby
To put the chipset (AN228E04 and AN228C04) into standby mode, send the control word "00xh, 00xh" to the chipset state machine. Standby mode invokes the following actions;-
The state machine will configure the RFID FPAA so that each internal resource has its bias current removed.
The internal clocks are also disabled.
Thus current (power) consumption is reduced to a minimum. All SRAM configuration bits retain in their current state.
The RFID State Machine output OSCen, is pulled low to shut down the external 24MHz crystal oscillator module.
The RFID State Machine then puts itself into standby mode; it stops its internal clock.

Wake-up from standby.
To re-activate the chipset from its "standby" state one simply sends a "null" control word (Two bytes of any data). The data contained in the first word will be ignored.
The first byte (8bits) are used as an interrupt - to wake the State Machine an 8bit byte ensures there is sufficient time for the internal oscillator to start and stabilize.
The second byte is used to clear the control word buffer.
The State Machine will then configure the RFID FPAA, this requires data to transfer between the two ICs after which the RFID FPAA will become active again resuming filtering with the same circuit it was configured with before "standby".
The RFID FPAA will become active 1milli-second after the last bit of the Control word arrives at the State Machine.

Anti-saturation, RFID FPAA input control.

Anti-saturation feature of this chipset allows the user to isolate the RFID FPAA filter input stage from the input signal, whilst maintaining all circuit bias points. This provides the user with a mechanism which can be used to mask out the high energy transmit signal from the low energy receive signal within an RFID card reader unit; avoiding potential receiver saturation.

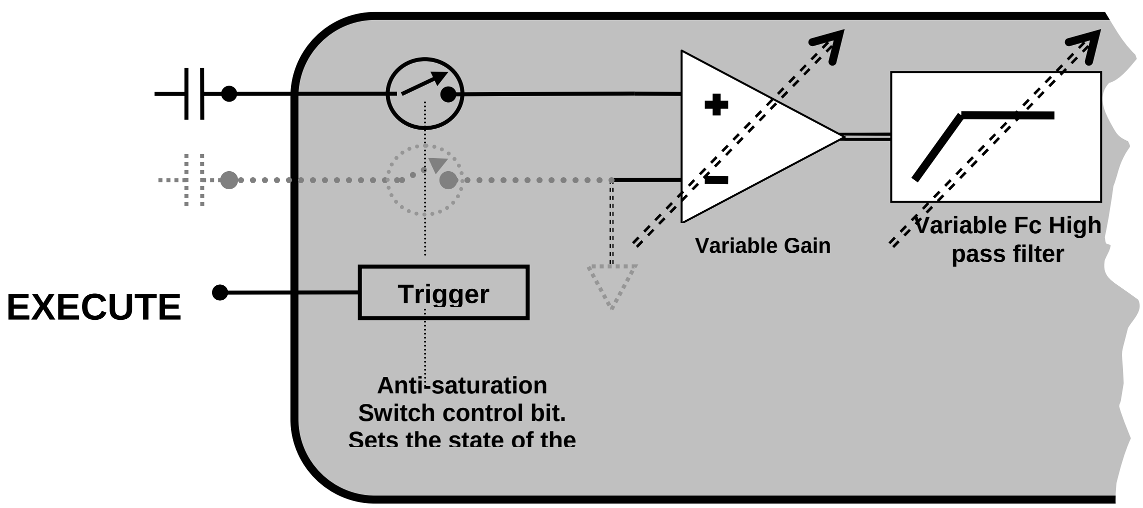


Fig 4, Anti-saturation feature

Timing control.

The state of the Input isolation switch is set by bit A1 of the RFID State Machine control word, the actual timing control is performed by control of a digital signal to the RFID FPAA EXECUTE pin.
Control word bit X is used to turn on (activate) the Trigger within the RFID FPAA, set bit X to 1 if the EXECUE trigger Pin will be used, otherwise set BitX to zero (software trigger of a new RFID FPAA state).
Anti-saturation switches should be used independently; no other control word bits should be changed when using this feature, only change bit A1 and X of the control word, maintain the same data in bit A2-HF4.
Final timing is controlled by the asynchronous EXECUTE pin on the FPAA, a rising edge on this pin triggers implementation of the state of the Anti-saturation switch, the switch will be closed in less than 10 nsec following a rising edge at the Execute pin.

RFID STATE MACHINE ELECTRICAL CHARACTERISTICS

Parameter	Absolute Maximum Ratings	Unit
Ambient temperature under bias	-40 to +125	°C
Storage temperature	-65 to +150	°C
Voltage on VDD with respect to VSS	-0.3 to +6.5	V
Voltage on any pin with respect to VSS	-0.3 to (VDD + 0.3)	V
Total power dissipation (Note 1)	0.8	W
Maximum current out of VSS pin	300	mA
Maximum current into VDD pin	250	mA
Input clamp current, (Vin < 0 or Vin > VDD)	±20	mA
Output clamp current, (Vout < 0 or Vout > VDD)	±20	mA
Maximum output current sunk by any I/O pin	25	mA
Maximum output current sourced by any I/O pin	25	mA

Note 1: Power dissipation is calculated as follows: Pdis = VDD x {IDD – ∑ IOH} + ∑ {(VDD – VOH) x IOH} + ∑(VOL x IOL)

Parameter	Typical	Unit
Typical Supply current	0.8	mA
The RFID State Machine has an internal 8MHz clock. Fosc	8.0 +/- 1%	MHz
CLRb Minimum pulse width	2	usec
Osc startup time	128	usec

RFID FPAA

Absolute Maximum Ratings

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	VDD	-0.5	-	5.5 V	V	AVSS, BVSS, DVSS and SVSS all held to 0.0 V [a]
xVDD to xVDD Offset		-0.5		0.5	V	Ideally all supplies have the same voltage
Package Power Dissipation	Pmax 25°C Pmax 85°C	-	-	1.8 0.73	W	Still air, No heatsink, 4 layer board, 44 pins. θja = 55°C/W
Analog and Digital Input Voltage	Vinmax	Vss-0.5	-	Vdd+0.5	V	
Ambient Operating Temperature	Top	-40	-	85	°C	
Storage Temperature	Tstg	-65		150	°C	

[a] Absolute Maximum DC Power Supply Rating - The failure mode is non-catastrophic for Vdd of up to 7 volts, but will cause reduced operating life time. The additional stress caused by higher local electric fields within the CMOS circuitry may induce metal migration, oxide leakage and other time/quality related issues.

Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	VDD	4.75	5.00	5.25	V	AVSS, BVSS, DVSS and SVSS all held to 0 V
Analog Input Voltage.	Vina	VMR-1.9	-	VMR+1.9	V	VMR is 2.0 volts above AVSS
Digital Input Voltage	Vind	0	-	DVDD	V	
Junction Temp	Tj	-40	-	125	°C	Assume a package θja = 55°C/W [b]

[b] In order to calculate the junction temperature you must first empirically determine the current draw (total Idd) for the design. Once the current consumption established then the following formula can be used; Tj = Ta + Idd x Vdd x 55 °C/W, where Ta is the ambient temperature. The worst-case θja of 55 °C/W assumes no air flow and no additional heatsink of any type.

Typical Operating

Parameter	Symbol	Min	Typ	Max	Unit	Comment
DC Power Supplies	VDD	-	5.00	-	V	AVSS, BVSS, DVSS and SVSS all held to 0 V
Power consumption	P1	-	430 330	-	mW	RFID_wide Without Notch filter
Power consumption	P2	-	380	-	mW	RFID_twin
Power consumption	P3	-	330	-	mW	RFID_fast
Power consumption	P4	-	1.0	-	mW	Standby mode

Analog Inputs General

All analog signal processing within the device is done with respect to Voltage Main Reference (VMR) which is nominally 2.0 V. The VMR signal is derived from a high precision, temperature compensated bandgap reference source.

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High Precision Input Range [c]	Vina	0.5	-	3.5	V	VMR +/- 1.5v
Standard precision Input Range [d]	Vina	0.1	-	3.9	V	VMR +/- 1.9v
High Precision Differential Input [c]	Vdiffina	0	-	+/-3.0	V	Common mode voltage = 2 V
Standard Precision Differential Input [d]	Vdiffina	0	-	+/-3.8	V	Common mode voltage = 2 V
Common Mode Input Range	Vcm	1.8	2.0	2.2	V	
Input Offset	Vos	-	5	15	mV	Non-chopper stabilized input
Input Frequency	Fain	0	<1	4	MHz	

[c] High precision operating range provides optimal linearity and dynamic range.

[d] Standard precision operating range provides maximum dynamic range and reduced linearity.

Analog Outputs

Parameter	Symbol	Min	Typ	Max	Unit	Comment
High Precision Output Range [c]	Vouta	0.5	-	3.5	V	VMR +/- 1.5v
Standard Precision Output Range [d]	Vouta	0.1	-	3.9	V	VMR +/- 1.9v
High Precision Differential Output [c]	Vdiffouta	-	-	+/-3.0	V	Common mode voltage = 2 V
Standard precision Differential Output [d]	Vdiffouta	-	-	+/-3.8	V	Common mode voltage = 2 V
Common Mode Voltage	Vcm	1.9	2.0	2.1	V	

[c]. High precision operating range provides optimal linearity and dynamic range.

[d]. Standard precision operating range provides maximum dynamic range and reduced linearity.

General Digital Output Characteristics (Vdd = 5v +/- 10%, -40 to 85 deg.C)

Parameter	Symbol	Min	Typ	Max	Unit	Comment
Output Voltage Low	Vol	0	-	20	-	% of DVDD
Output Voltage High	Voh	80	-	100	-	% of DVDD
Max. Capacitive Load	Cmax	-	-	10	pF	The maximum load for a digital output is 10 pF // 10 Kohm
Min. Resistive Load	Rmin	10	-	-	Kohm	The maximum load for a digital output is 10 pF // 10 Kohm
DCLK Frequency	Fmax	0	-	8	MHz	DCLK is fixed for the RFID chipset
ACLK Frequency	Fmax	24	-	24	MHz	The ACLK frequency is fixed for the RFID FPAA
Clock Duty Cycle	-	45	-	55	%	All clocks

RFID ACLK

The RFID FPAA device's on-chip oscillator automatically detects an attached crystal and uses it to establish self generated internal clock that can be used internally. The frequency of the attached crystal needs to be 24 MHz.

Alternatively an external 24Mhz 0-5volt digital clock signal from any source may be used,

MECHANICAL AND HANDLING

The RangeMaster is a two-chip solution. The RFID is packaged in industry standard 44 lead QFP package and the RFID state machine is packaged in an industry standard 20-pin SSOP. The following pages detail the Pin configuration and the mechanical package details.

Dry pack handling is recommended. The packages are qualified to MSL3 (JEDEC Standard, J-STD-020A, Level 3). Once the device is removed from dry pack, 30°C at 60% humidity for not longer than 168 hours is the maximum recommended exposure prior to solder reflow. If out of dry pack for longer than this recommended period of time, then the recommended bake out procedure prior to solder reflow is 24 hours at 125°C.

ESD Characteristics RFID FPAA, AN228E04

Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital Inputs	4000V	250V	4kV
Digital Outputs	4000V	250V	4kV
Digital Bidirectional	4000V	250V	4kV
Digital Open Drain	4000V	250V	4kV
Analog Inputs	2000V	200V	4kV
Analog Outputs	1500V	100V	4kV
Reference Voltages	1500V	100V	4kV

The AN228E04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN228E04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

ESD Characteristics RFID State Machine AN228C04

Pin Type	Human Body Model	Machine Model	Charged Device Model
Digital Inputs	4000V	250V	4kV
Digital Outputs	4000V	250V	4kV
Digital Bidirectional	4000V	250V	4kV
Digital Open Drain	4000V	250V	4kV

The AN228C04 is an ESD (electrostatic discharge) sensitive device. Electrostatic charges as high as 4000V readily accumulate on the human body and test equipment and can discharge without detection. Although the AN228C04 device features proprietary ESD protection circuitry, permanent damage may occur on devices subjected to high-energy electrostatic discharges. Therefore, proper ESD precautions are recommended to avoid performance degradation or loss of functionality.

RFID FPAA PINOUT, 44pin QFP.

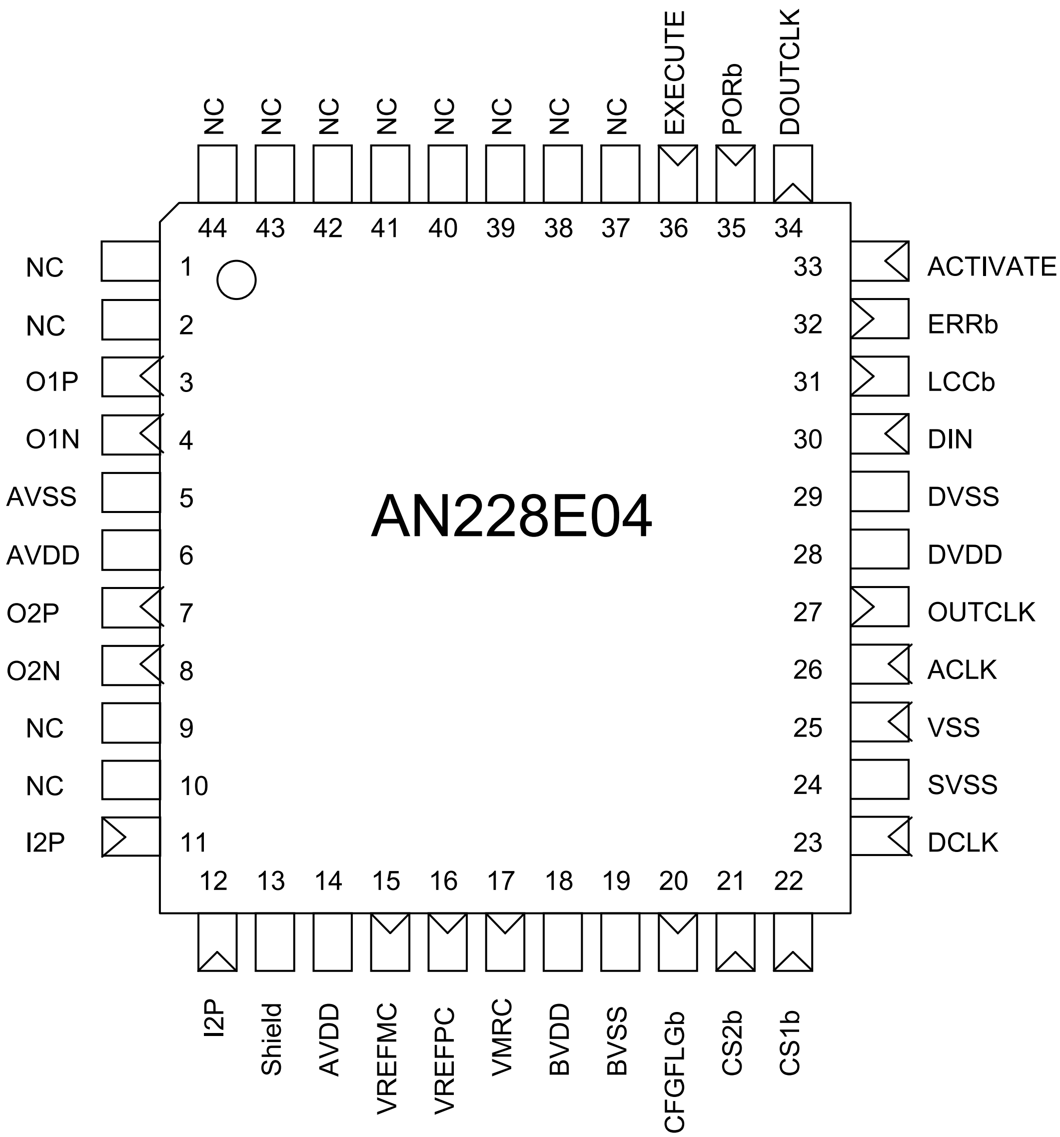
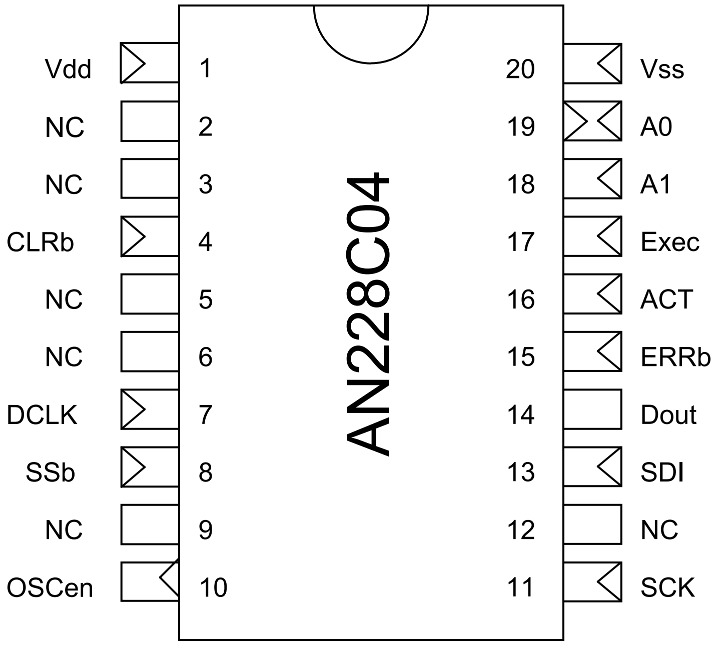


Fig 5, RFID FPAA Pin drawing

Pin	RFID FPAA Pin name	Generic Pin Name	Pin Type	Comments
1	*Not used*	I4PA	Analog I+	
2	*Not used*	I4NA	Analog I-	
3	O1P	O1P	Analog OUT+	
4	O1N	O1N	Analog OUT-	
5	AVSS	AVSS	Analog VSS	Analog Ground: 0 Volts
6	AVDD	AVDD	Analog VDD	Analog Power: +5 Volts ±5%
7	O2P	O2P	Analog OUT+	
8	O2N	O2N	Analog OUT-	
9	*Not used*	I1P	Analog I+	
10	*Not used*	I1N	Analog I-	
11	I2P	I2P	Analog I+	
12	I2N	I2N	Analog I-	
13	SHIELD	SHIELD	Analog VDD	Low noise VDD bias for capacitor array n-wells: +5 Volt
14	AVDD2	AVDD2	Analog VDD	Analog Power: +5 Volts ±5%
15	VREFMC	VREFMC	Vref	Attach filter capacitor for VREF-
16	VREFPC	VREFPC	Vref	Attach filter capacitor for VREF+
17	VMRC	VMRC	Vref	Attach filter capacitor for VMR (Voltage Main Reference)
18	BVDD	BVDD	Analog VDD	Analog Power for Bandgap Vref Generators: +5 Volts
19	BVSS	BVSS	Analog VSS	Analog Ground for Bandgap Vref Generators: 0 Volts
20	CFGFLGb	CFGFLGb	Digital IN/OUT (open drain)	Configuration flag. A low output indicates configuration is in progress.
21	CS2b	CS2b	Digital IN	Chip Select 2
22	CS1b	CS1b	Digital IN	Chip Select 1
23	DCLK	DCLK	Digital IN	Configuration data strobe and configuration state machine clock.
24	SVSS	SVSS	Digital VSS	Digital Ground - Substrate Tie: 0 Volts
25	DVSS	DVSS	Digital IN	0 Volts
26	ACLK	ACLK	Digital IN/OUT	Analog sample clock or EPROM clock
27	OUTCLK	OUTCLK	Digital OUT	Programmable Digital Output or EPROM MOSI data stream
28	DVDD	DVDD	Digital VDD	+5 Volts ±5%
29	DVSS	DVSS	Digital VSS	0 Volts
30	DIN	DIN	Digital IN	Serial Configuration Data Input
31	LCCb	LCCb	Digital OUT	Local configuration complete
32	ERRb	ERRb	Digital IN/OUT (open drain) (10 KOhm pull-up required)	Configuration error signal
33	ACTIVATE	ACTIVATE	Digital IN/OUT (open drain)	Indicates Shadow SRAM to Configuration SRAM transfer will occur on next DCLK edge.
34	DOUTCLK	DOUTCLK	Digital OUT	Buffered version of DCLK
35	PORb	PORb	Digital IN/OUT (open drain)	Power On Reset - The minimum pulse width required is 25 nS.
36	EXECUTE	EXECUTE	Digital IN	External trigger - Shadow SRAM to Configuration SRAM transfer
37	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
38	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
39	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
40	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
41	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
42	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
43	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected
44	*Not used*	NC	n/a	Do not make an electrical connection, leave Not Connected

Table 1, RFID FPAA Pin list

RFID STATE MACHINE PINOUT, 20 Pin SSOP,



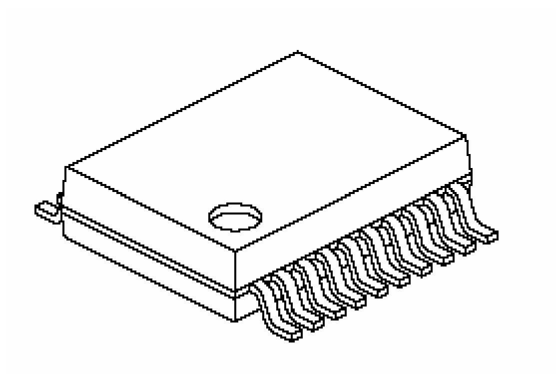
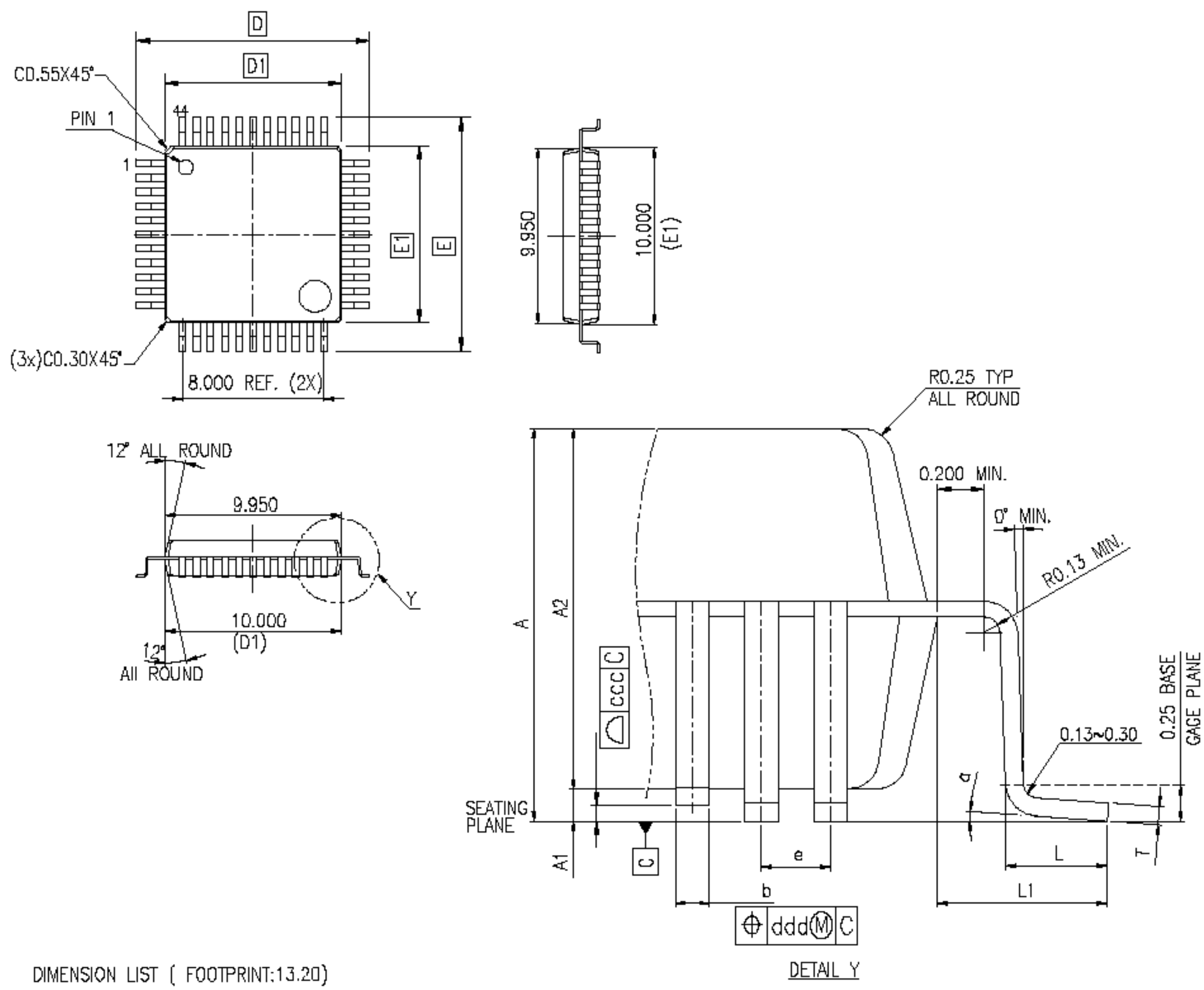


Fig 6, RFID State Machine Pin drawing

Pin Number	Pin Name	Pin Type	Description
1	Vdd	Supply	Positive 5v supply
2	NC	n/a	Do not make an electrical connection, leave Not Connected
3	NC	n/a	Do not make an electrical connection, leave Not Connected
4	CLRb	Input	CMOS level Schmitt trigger with internal Pull-up, State Machine Clear,
5	NC	n/a	Do not make an electrical connection, leave Not Connected
6	NC	n/a	Do not make an electrical connection, leave Not Connected
7	DCLK	Output	CMOS output, Data strobe Clock to RFID FPAA
8	SSb	Input	Slave Select Input
9	NC	n/a	Do not make an electrical connection, leave Not Connected
10	NC	n/a	Do not make an electrical connection, leave Not Connected
11	SCK	Input	SPI compatible Clock input, CMOS level.
12	NC	n/a	Do not make an electrical connection, leave Not Connected
13	SDI	Input	SPI compatible Serial Data In, CMOS level Schmitt trigger
14	Dout	Output	CMOS output, Data out to RFID FPAA
15	ERRb	Input	CMOS level Schmitt trigger,
16	ACT	I/O	CMOS level, RFID FPAA "Activate" control and monitor.
17	Exec	I/O	CMOS level, this pin is functionally disabled in this Device.
18	A1	n/a	Factory reserved, test pin, leave Not Connected
19	A0	n/a	Factory reserved, test pin, leave Not Connected
20	Vss	Supply	Power supply Ground (Zero Volts)

Table2, RFID State Machine Pin drawing

44 Lead Quad Flat Pack (QFP) – 10x10mm, 2mm body thickness, Lead finish Matt tin (Sn-Cu).



DIMENSION LIST (FOOTPRINT:13.20)

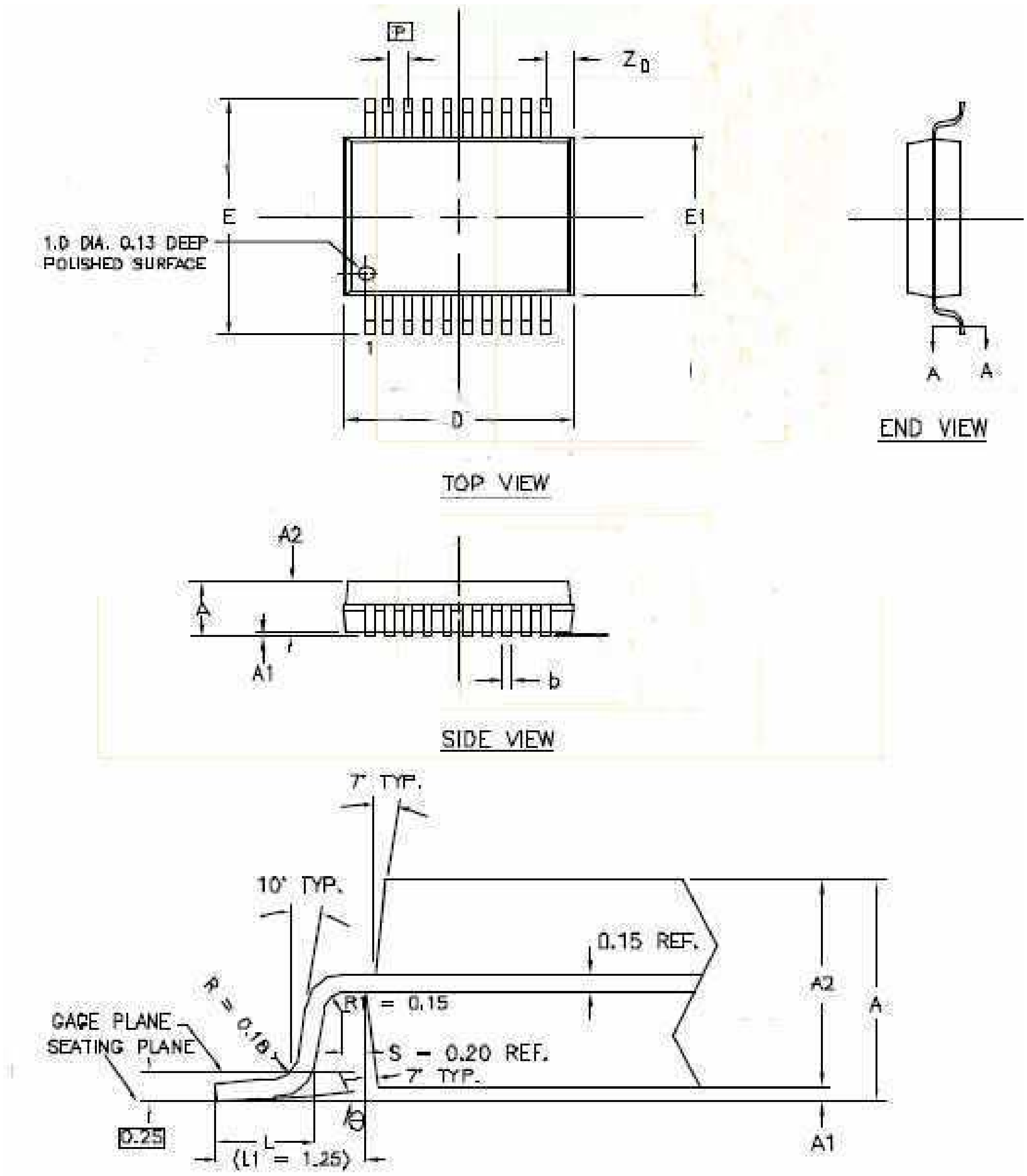
S/N	SYM	DIMENSIONS	REMARKS
1	A	MAX. 2.450	OVERALL HEIGTH
2	A1	MAX. 0.500	STANDOFF
3	A2	2.000±0.200	PKG THICKNESS
4	D	13.200±0.250	LEAD TIP TO TIP
5	D1	10.000±0.100	PKG LENGTH
6	E	13.200±0.250	LEAD TIP TO TIP
7	E1	10.000±0.100	PKG WIDTH
8	L	0.880±0.150	FOOT LENGTH
9	L1	1.600 REF.	LEAD LENGTH
10	T	0.130~0.230	FRAME THICKNESS
11	α	0~7°	LEAD FLAT ANGLE
12	b	0.300~0.450	LEAD WIDTH
13	e	0.800 BASE	LEAD PITCH
14	ccc	0.100	FOOT PLANARITY
15	ddd	0.100	FOOT POSITION

NOTES :

S/N	DESCRIPTION		SPECIFICATION
1	GENERAL TOLERANCE.	DISTANCE	±0.100
		ANGLE	±2.5°
2	MATTE FINISH ON PACKAGE BODY SURFACE EXPECT EJECTION AND PIN 1 MARKING.		Ra1.5~2.5um
3	ALL MOLDED BODY SHARP CORNER RADII UNLESS OTHERWISE SPECIFIED.		MAX. R0.200
4	PACKAGE/LEADFRAME MISALIGNMENT (X, Y):		MAX. 0.127
5	TOP/BTM PACKAGE MISALIGNMENT (X, Y):		MAX. 0.127
6	DRAWING DOES NOT INCLUDE PLASTIC OR METAL PROTRUSION OR CUTTING BURR.		
7	COMPLIANT TO JEDEC STANDARD: MS-022		

Figure 7: Package drawing for the RangeMaster RFID FPAA AN228E04

20-Lead Plastic Shrink Small Outline (SSOP) – 209 mil Body, 5.30 mm. Lead finish Matt tin (Sn).



	Units	INCHES			MILLIMETERS*		
Dimension Limits		MIN	NOM	MAX	MIN	NOM	MAX
Number of Pins	n		20			20	
Pitch	p		.026			0.65	
Overall Height	A	-	-	.079	-	-	2.00
Molded Package Thickness	A2	.065	.069	.073	1.65	1.75	1.85
Standoff	A1	.002	-	-	0.05	-	-
Overall Width	E	.291	.307	.323	7.40	7.80	8.20
Molded Package Width	E1	.197	.209	.220	5.00	5.30	5.60
Overall Length	D	.272	.283	.289	.295	7.20	7.50
Foot Length	L	.022	.030	.037	0.55	0.75	0.95

Figure 8: Package drawing for the RangeMaster RFID State Machine (AN228C04)

Figure 9, RangeMaster Evaluation Board Schematic diagram.