THC63LVD1027

85MHz 10Bits Dual LVDS Repeater

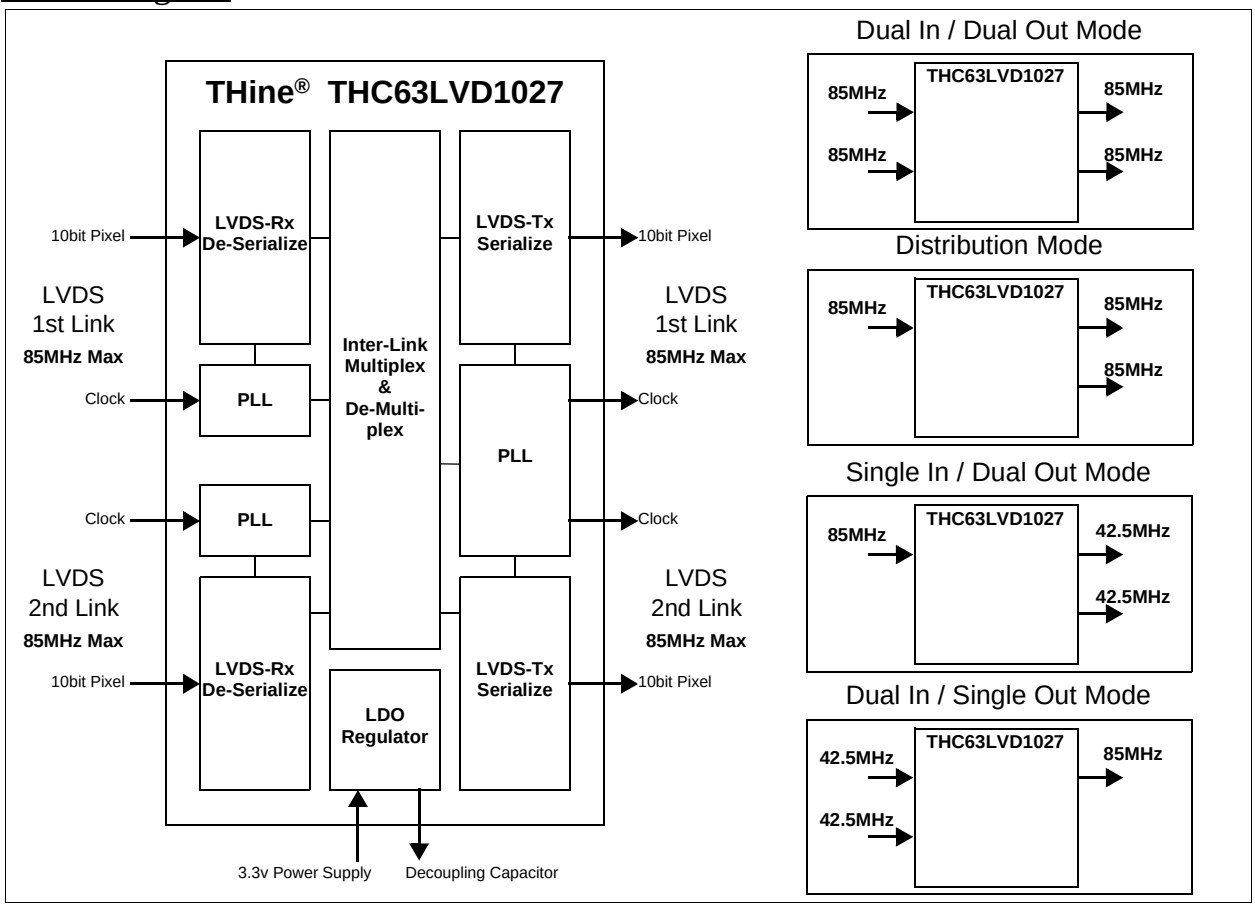
General Description

The THC63LVD1027 LVDS(Low Voltage Differential Signaling) repeater is designed to support pixel data transmission between Host and Flat Panel Display up to WUXGA resolution.
THC63LVD1027 receives the dual channel LVDS data streams and transmits the LVDS data through various line rate conversion modes, Dual Link Input / Dual Link Output, Single Link Input / Dual Link Output, and Dual Link Input / Single Link Output.
At a transmit clock frequency of 85MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE) are transmitted at an effective rate of 595Mbps per LVDS channel.

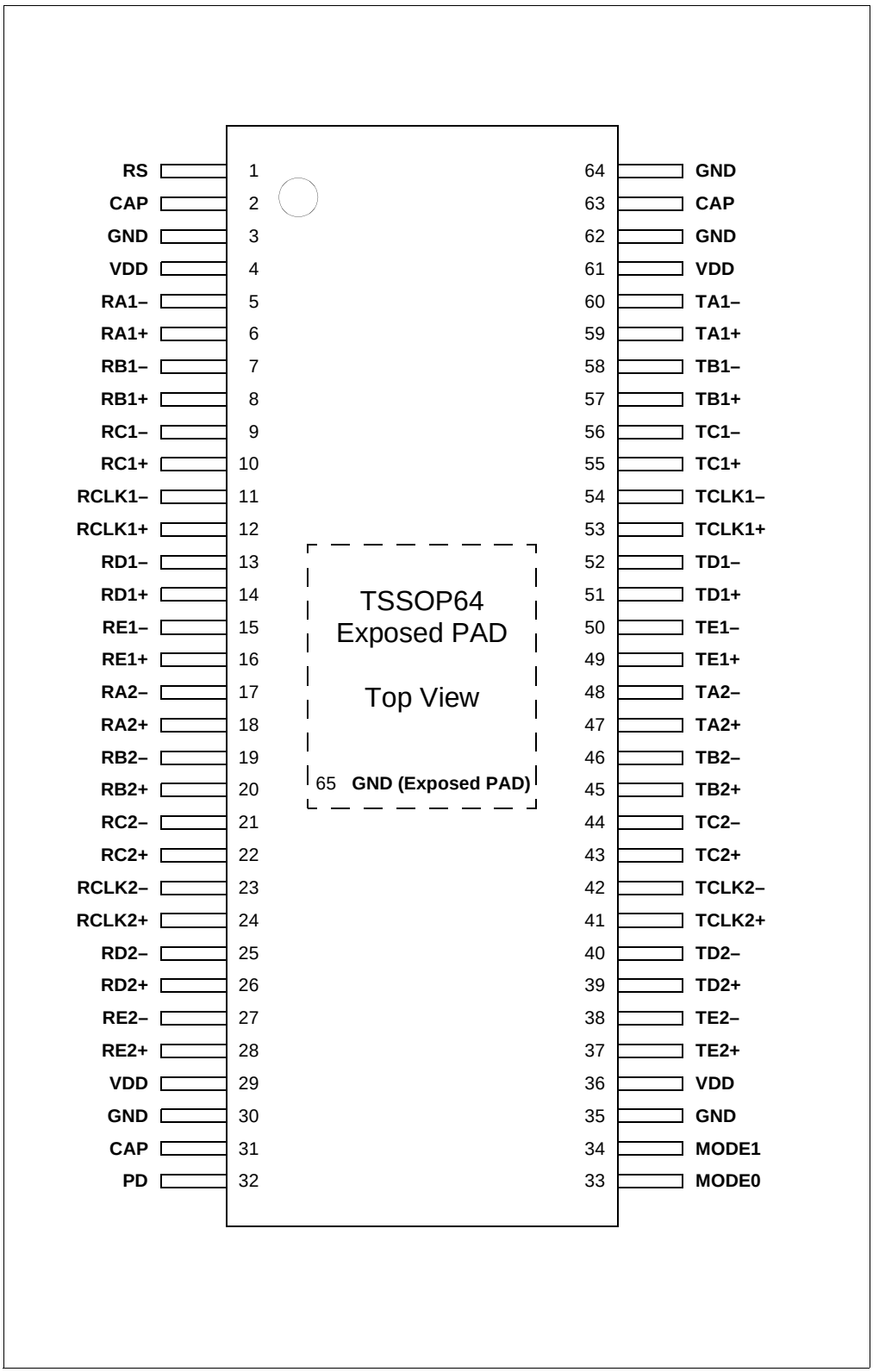
Features

- Up to 85MHz 10bit dual channel LVDS Receiver
- Up to 85MHz 10bit dual channel LVDS Transmitter
- Wide LVDS input skew margin: ± 480ps at 75MHz
- Accurate LVDS output timing: ± 250ps at 75MHz
- Reduced swing LVDS output mode supported to suppress the system EMI
- Various line rate conversion modes supported
  Dual link input / Dual link output [clkout=1x clkin]
  Single link input / Dual link output [clkout=1/2x clkin]
  Dual link input / Single link output [clkout=2x clkin]
- Distribution (signal duplication) mode supported
- Power down mode supported
- 3.3V single voltage power supply
- No external components required for PLLs
- 64pin TSSOP with Exposed PAD (0.5mm lead pitch)

Block Diagram



Pin Out



Pin Description

<table>
<tr><th>Pin Name</th><th>Direction</th><th>Type</th><th>Description</th></tr>
<tr><td>RA1+/–</td><td rowspan="12">Input</td><td rowspan="24">LVDS</td><td>LVDS data input for channel A of 1st Link</td></tr>
<tr><td>RB1+/–</td><td>LVDS data input for channel B of 1st Link</td></tr>
<tr><td>RC1+/–</td><td>LVDS data input for channel C of 1st Link</td></tr>
<tr><td>RD1+/–</td><td>LVDS data input for channel D of 1st Link</td></tr>
<tr><td>RE1+/–</td><td>LVDS data input for channel E of 1st Link</td></tr>
<tr><td>RCLK1+/–</td><td>LVDS clock input for 1st Link</td></tr>
<tr><td>RA2+/–</td><td>LVDS data input for channel A of 2nd Link</td></tr>
<tr><td>RB2+/–</td><td>LVDS data input for channel B of 2nd Link</td></tr>
<tr><td>RC2+/–</td><td>LVDS data input for channel C of 2nd Link</td></tr>
<tr><td>RD2+/–</td><td>LVDS data input for channel D of 2nd Link</td></tr>
<tr><td>RE2+/–</td><td>LVDS data input for channel E of 2nd Link</td></tr>
<tr><td>RCLK2+/–</td><td>LVDS clock input for 2nd Link
In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z.
(see “Mode selection” below in this page.)</td></tr>
<tr><td>TA1+/–</td><td rowspan="12">Output</td><td>LVDS data output for channel A of 1st Link</td></tr>
<tr><td>TB1+/–</td><td>LVDS data output for channel B of 1st Link</td></tr>
<tr><td>TC1+/–</td><td>LVDS data output for channel C of 1st Link</td></tr>
<tr><td>TD1+/–</td><td>LVDS data output for channel D of 1st Link</td></tr>
<tr><td>TE1+/–</td><td>LVDS data output for channel E of 1st Link</td></tr>
<tr><td>TCLK1+/–</td><td>LVDS clock output for 1st Link</td></tr>
<tr><td>TA2+/–</td><td>LVDS data output for channel A of 2nd Link</td></tr>
<tr><td>TB2+/–</td><td>LVDS data output for channel B of 2nd Link</td></tr>
<tr><td>TC2+/–</td><td>LVDS data output for channel C of 2nd Link</td></tr>
<tr><td>TD2+/–</td><td>LVDS data output for channel D of 2nd Link</td></tr>
<tr><td>TE2+/–</td><td>LVDS data output for channel E of 2nd Link</td></tr>
<tr><td>TCLK2+/-</td><td>LVDS clock output for 2nd Link</td></tr>
<tr><td>PD</td><td rowspan="3">Input</td><td rowspan="3">LV-TTL</td><td>Power Down
H: Normal operation
L: Power down state, all LVDS output signals turn to Hi-Z</td></tr>
<tr><td>RS</td><td>LVDS output swing level selection
H: Normal swing
L: Reduced swing</td></tr>
<tr><td>MODE1
MODE0</td><td>Mode selection
<table>
<tr><th>MODE1</th><th>MODE0</th><th>RCLK2+/-</th><th>Description</th></tr>
<tr><td>L</td><td>L</td><td>clkin</td><td>Dual-in / Dual-out mode</td></tr>
<tr><td>L</td><td>L</td><td>Hi-Z</td><td>Distribution mode</td></tr>
<tr><td>H</td><td>L</td><td>Hi-Z</td><td>Single-in / Dual-out mode</td></tr>
<tr><td>L</td><td>H</td><td>clkin</td><td>Dual-in / Single-out mode</td></tr>
<tr><td>H</td><td>H</td><td>-</td><td>Reserved</td></tr>
</table>
In Distribution and Single-in/Dual-out mode, RCLK2+/- must be Hi-Z.</td></tr>
<tr><td>VDD</td><td rowspan="3">Power</td><td rowspan="3">—</td><td>3.3v power supply pins</td></tr>
<tr><td>GND</td><td>Ground pins (Exposed PAD is also Ground)</td></tr>
<tr><td>CAP</td><td>Decoupling capacitor pins
These pins should be connected to external decoupling capacitors (C_{CAP}).
Recommended C_{CAP} is 0.1uF</td></tr>
</table>

Mode Setting

Input/Output	RCLK2+/-	MODE1 (Input mode) H: Single L: Dual	MODE0 (Output mode) H: Single L: Dual
Dual-In/Dual-Out (Fig.2-1, 3-1)	CLK in	L	L
Distribution (Fig.2-2, 3-2)	Hi-z	L	L
Single-In/Dual-Out (Fig.2-3, 3-3)	Hi-z	H	L
Dual-In/Single-Out (Fig.2-4, 3-4)	CLK in	L	H
Reserved	--	H	H

Signal Flow for Each Setting

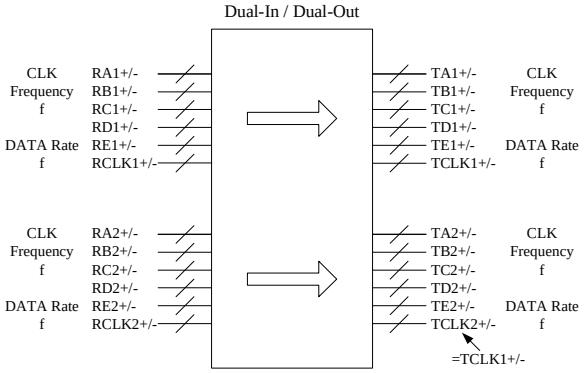


Fig2-1

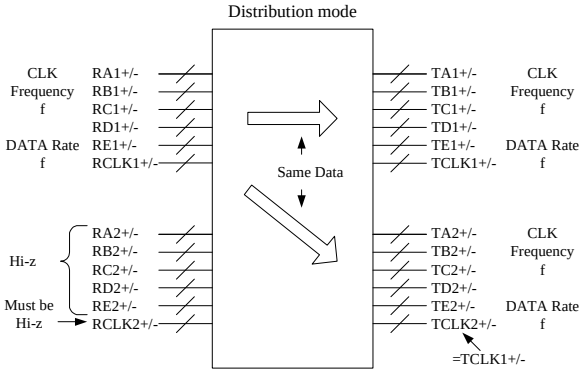


Fig2-2

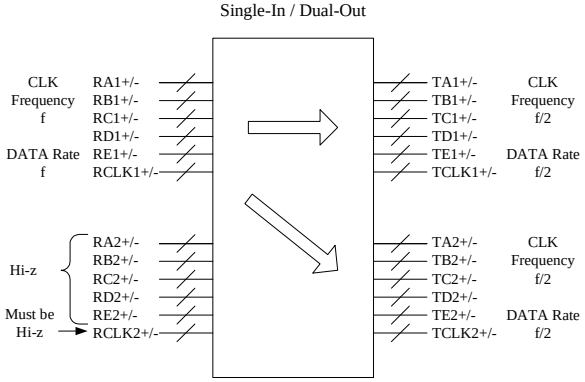


Fig2-3

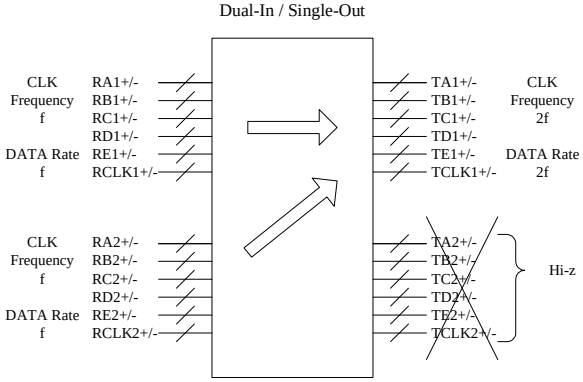


Fig2-4

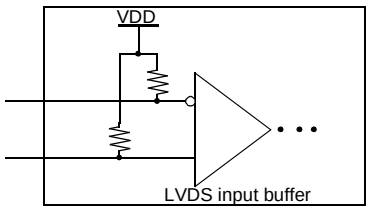
Output Control / Fail Safe

THC63LVD1027 has a function to control output depending on LVDS input condition.

PD	RCLK1+/-	RCLK2+/-	Output
L	*	*	All Hi-z
H	Hi-z	*	All Hi-z
H	CLK in	CLK in	Refer to p.4 Mode Setting #
H	CLK in	Hi-z	Refer to p.4 Mode Setting #

*: Don't care
#: If a particular input data pair is Hi-z, the corresponding output data become L according to LVDS DC spec.

For fail-safe purpose, all LVDS input pins are connected to VDD via resistance for detecting state of Hi-z.



Internal circuit of THC63LVD1027

Absolute Maximum Ratings

Parameter	Min	Max	Unit
Power Supply voltage	–0.3	4.0	V
LVDS Input Voltage	-0.3	V_{DD}+0.3	V
Junction Temperature	—	125	ºC
Storage Temperature	–55	125	ºC
Reflow Peak Temperature / Time	—	260 / 10sec.	ºC
Maximum Power Dissipation @+25°C	—	2.5	W

Operating Conditions

Symbol	Parameter		Min	Typ	Max	Unit
Ta	Ambient Temperature		–20	25	70	ºC
V_{DD}	Power Supply voltage		3.0	3.3	3.6	V
F_{clk}	Dual-in / Dual-out	Input	20	—	85	MHz
		Output	20	—	85	MHz
	Distribution	Input	20	—	85	MHz
		Output	20	—	85	MHz
	Single-in / Dual-out	Input	40	—	85	MHz
		Output	20	—	42.5	MHz
	Dual-in / Single-out	Input	20	—	42.5	MHz
		Output	40	—	85	MHz

Power Dissipation

Symbol	Parameter	Conditions			Min	Typ	Max	Unit
I_{CCW}	Operating Current (Worst Case Pattern) Fig1	Dual-in/Dual-out	C_{LKIN}=40MHz	R_{L_TX} = 100Ω CL=5pF RS=V_{DD} Fig2	—	—	265	mA
			C_{LKIN}=65MHz		—	—	305	mA
			C_{LKIN}=75MHz		—	—	325	mA
			C_{LKIN}=85MHz		—	—	340	mA
		Distribution	C_{LKIN}=40MHz		—	—	215	mA
			C_{LKIN}=65MHz		—	—	235	mA
			C_{LKIN}=75MHz		—	—	245	mA
			C_{LKIN}=85MHz		—	—	260	mA
		Single-in/Dual-out	C_{LKIN}=40MHz		—	—	175	mA
			C_{LKIN}=65MHz		—	—	190	mA
			C_{LKIN}=75MHz		—	—	200	mA
			C_{LKIN}=85MHz		—	—	210	mA
		Dual-in/Single-out	C_{LKIN}=20MHz		—	—	215	mA
			C_{LKIN}=32.5MHz		—	—	235	mA
			C_{LKIN}=37.5MHz		—	—	245	mA
			C_{LKIN}=42.5MHz		—	—	260	mA
I_{CCS}	Power Down Current	—	—		—	—	8	mA

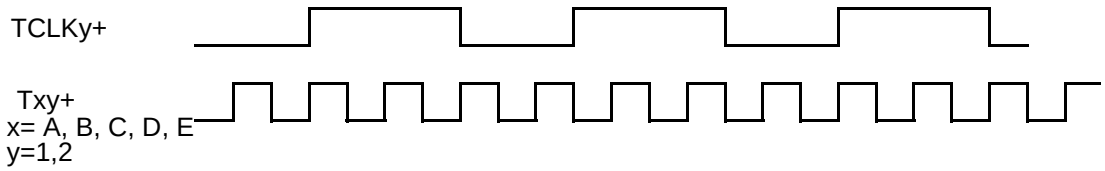
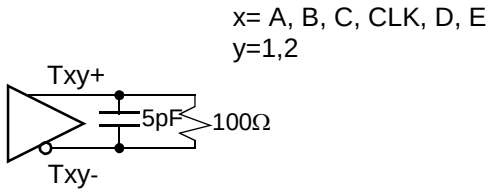


Fig1. Test Pattern (LVDS Output Full Toggle Pattern)



LVDS Output Load

Fig2. LVDS Output Load

Electrical Characteristics

THC63LVD1027 DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
Vcap	Capacitor pin appearance voltage	C_{CAP} = 0.1μF	—	1.8	—	V
V_{IL_TTL}	LV-TTL Input Low Voltage	—	GND	—	0.8	
V_{IH_TTL}	LV-TTL Input High Voltage	—	2.0	—	VDD	
I_{IN_TTL}	LV-TTL Input Leakage Current	—	-4	—	+4	μA

LVDS Receiver DC Specifications

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IN_RX}	LVDS-Rx Input voltage range	—	0.3	—	2.1	V
V_{IC_RX}	LVDS-Rx Common voltage	—	0.6	1.2	1.8	
V_{TH_RX}	LVDS-Rx differential High threshold	V_{IC_RX} = 1.2V	—	—	+100	mV
V_{TL_RX}	LVDS-Rx differential Low threshold		-100	—	—	
$\lvert V_{ID\_RX} \rvert$	LVDS-Rx differential Input Voltage	—	100	—	600	
I_{IN_RX}	LVDS-Rx Input Leakage current	—	-0.3	—	0.3	mA

LVDS Transmitter DC Specifications

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
V_{OC_TX}	LVDS-Tx Common voltage	R_{L_TX} = 100Ω	—	1.125	1.25	1.375	V
ΔV_{OC_TX}	Change in VOC between complementary output states		—	—	—	35	mV
$\lvert V_{OD\_TX} \rvert$	LVDS-Tx differential Output Voltage		Normal swing	250	350	450	mV
			Reduced swing	100	200	300	
ΔV_{OD_TX}	Change in VOD between complementary output states		—	—	—	35	mV
I_{OS_TX}	LVDS-Tx Output Short current		Vout= GND	-24	—	—	mA
I_{OZ_TX}	LVDS-Tx Output Tri-state current	PD=GND	Vout= GND to Vcc	-10	—	+10	uA

THC63LVD1027 AC Characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
t_{LT}	Phase Lock Loop Set Time (Fig.3)	—	—	—	—	10	ms
t_{DL}	Data Latency (Fig.4)	Dual-in/Dual-out	CLKIN=75MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	ns
		Distribution	CLKIN=75MHz	$9t_{RCP}+3$	$9t_{RCP}+5$	$9t_{RCP}+7$	
		Single-in/Dual-out	CLKIN=75MHz	$(11+2/7)t_{RCP}+3$	$(11+2/7)t_{RCP}+5$	$(11+2/7)t_{RCP}+7$	
		Dual-in/Single-out	CLKIN=37.5MHz	$(8+5/14)t_{RCP}+3$	$(8+5/14)t_{RCP}+5$	$(8+5/14)t_{RCP}+7$	
t_{DEH}	DE input High time (Fig.5)	Single-in/ Dual-out	—	$2t_{RCP}$	—	—	ns
t_{DEL}	DE input Low time (Fig.5)		—	$2t_{RCP}$	—	—	
t_{DEINT}	DE input Period (Fig.5)		—	$4t_{RCP}$	Must be $2nt_{RCP}$ (n=integer)	—	

AC Timing Diagrams

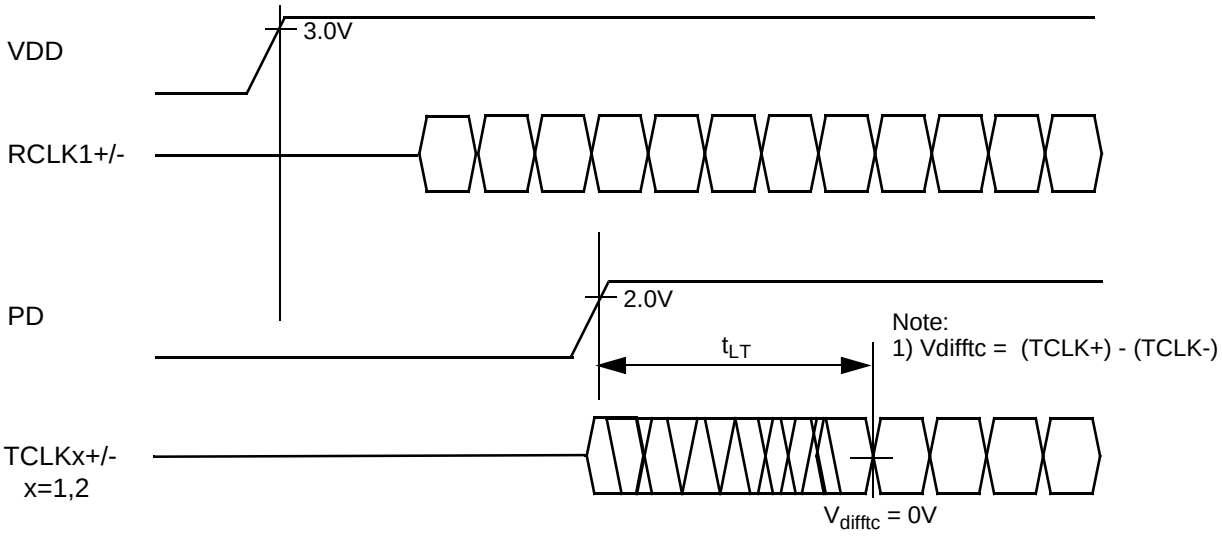


Fig.3. Phase Lock Loop Set Time

AC Timing Diagrams (Continued)

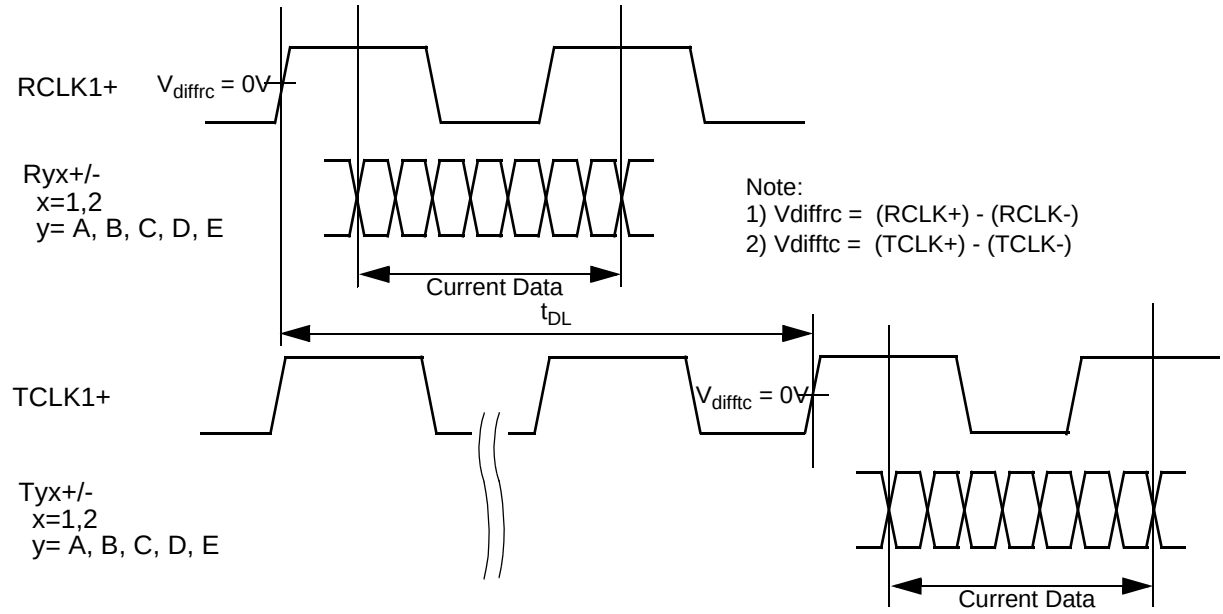


Fig.4. DATA Latency

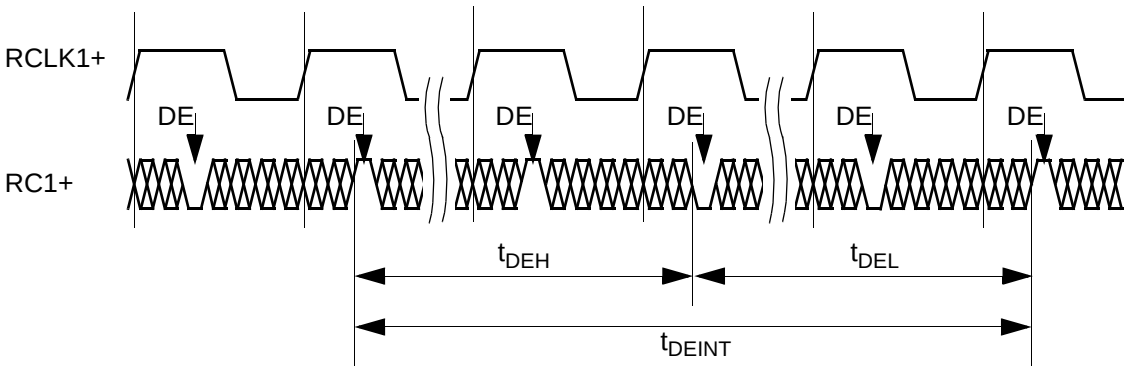
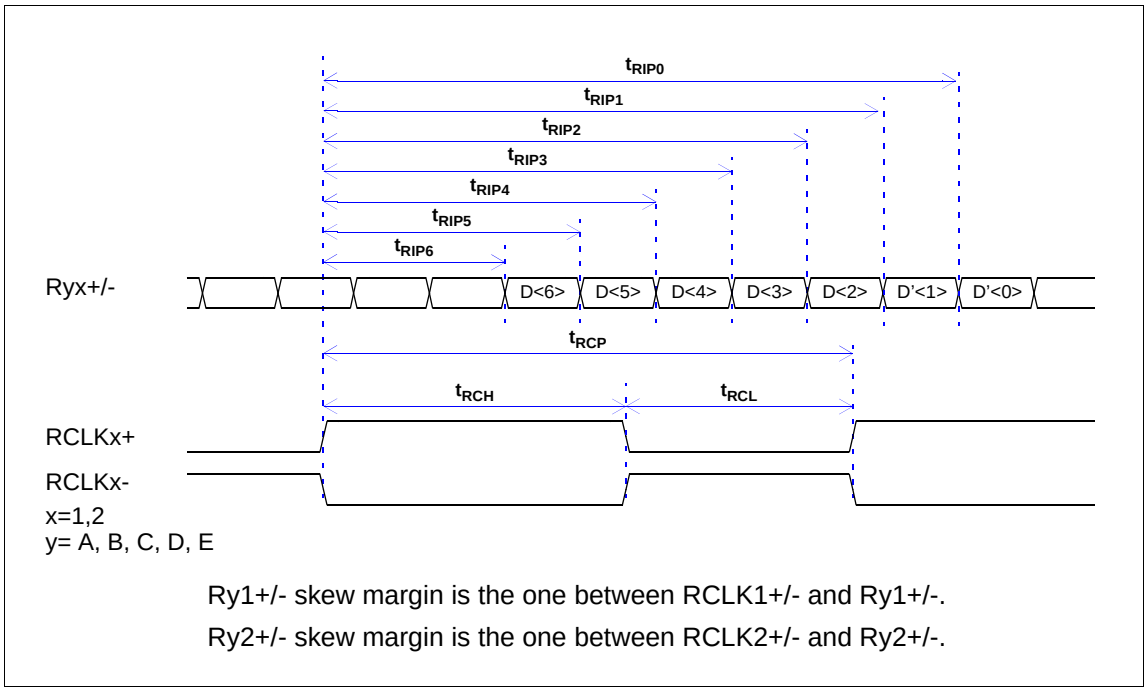


Fig.5. Single link input / Dual link output mode RC1(DE) input timing

LVDS Receiver AC Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{RCP}	LVDS Clock Period	—	11.76	—	50	ns
t_{RCH}	LVDS Clock High duration	—	2/7 t_{RCP}	4/7 t_{RCP}	5/7 t_{RCP}	
t_{RCL}	LVDS Clock Low duration	—	2/7 t_{RCP}	3/7 t_{RCP}	5/7 t_{RCP}	
t_{RSUP}	LVDS data input setup margin	CLKIN=75MHz	480	—	—	ps
t_{RHLD}	LVDS data input hold margin	CLKIN=75MHz	480	—	—	
t_{RIP6}	LVDS data input position 6	—	2/7t_{RCP} - t_{RHLD}	2/7 t_{RCP}	2/7t_{RCP} + t_{RSUP}	ps
t_{RIP5}	LVDS data input position 5	—	3/7t_{RCP} - t_{RHLD}	3/7 t_{RCP}	3/7t_{RCP} + t_{RSUP}	
t_{RIP4}	LVDS data input position 4	—	4/7t_{RCP} - t_{RHLD}	4/7 t_{RCP}	4/7t_{RCP} + t_{RSUP}	
t_{RIP3}	LVDS data input position 3	—	5/7t_{RCP} - t_{RHLD}	5/7 t_{RCP}	5/7t_{RCP} + t_{RSUP}	
t_{RIP2}	LVDS data input position 2	—	6/7t_{RCP} - t_{RHLD}	6/7 t_{RCP}	6/7t_{RCP} + t_{RSUP}	
t_{RIP1}	LVDS data input position 1	—	7/7t_{RCP} - t_{RHLD}	7/7 t_{RCP}	7/7t_{RCP} + t_{RSUP}	
t_{RIP0}	LVDS data input position 0	—	8/7t_{RCP} - t_{RHLD}	8/7 t_{RCP}	8/7t_{RCP} + t_{RSUP}	
t_{CK12}	Skew Time between RCLK1 and RCLK2 (Fig.6)	—	-0.3 t_{RCP}	—	0.3 t_{RCP}	ps

LVDS Receiver Input Timing



Ry1+/- skew margin is the one between RCLK1+/- and Ry1+/-.

Ry2+/- skew margin is the one between RCLK2+/- and Ry2+/-.

LVDS Receiver Input Timing (Continued)

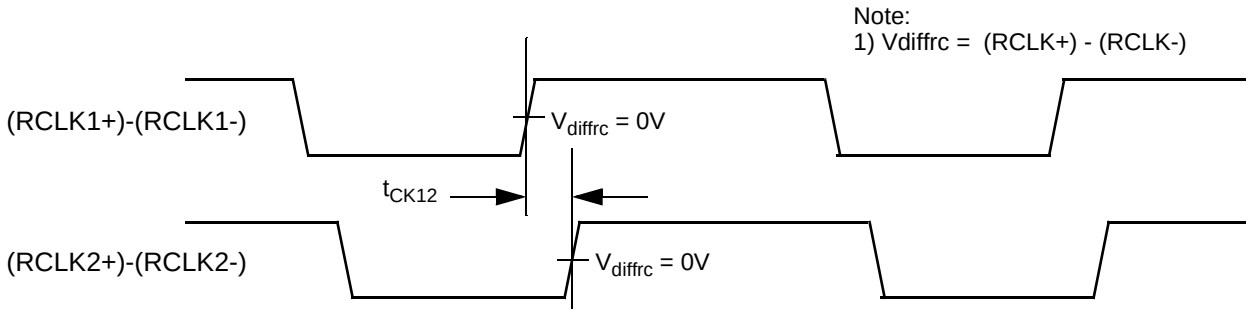
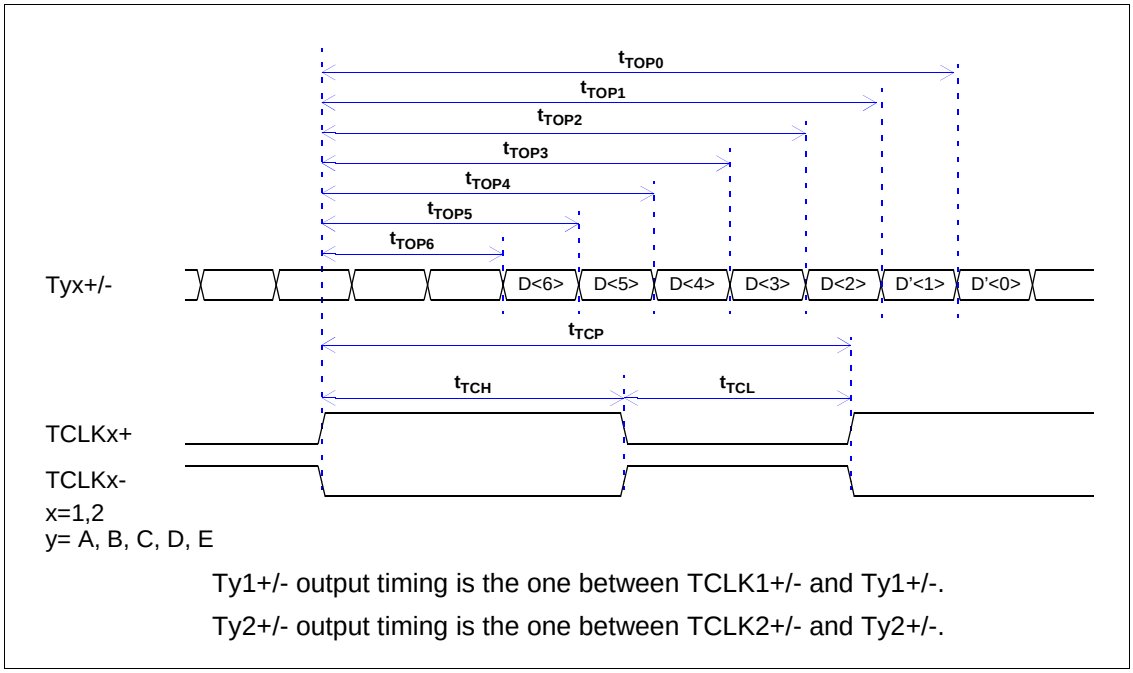


Fig.6. Skew Time between RCLK1 and RCLK2

LVDS Transmitter AC Characteristics

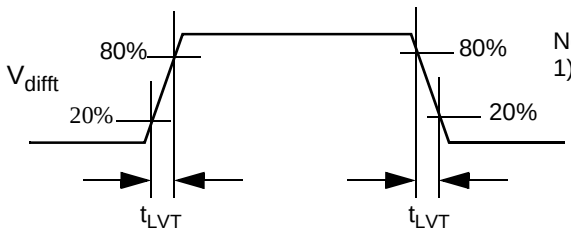
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
t_{TCP}	LVDS Clock Period	—	11.76	—	50	ns
t_{TCH}	LVDS Clock High duration	—	—	4/7 t_{TCP}	—	
t_{TCL}	LVDS Clock Low duration	—	—	3/7 t_{TCP}	—	
t_{TSUP}	LVDS data output setup	CLKOUT=75MHz	—	—	250	ps
t_{THLD}	LVDS data output hold	CLKOUT=75MHz	—	—	250	
t_{TOP6}	LVDS data output position 6	—	2/7t_{TCP} - t_{THLD}	2/7 t_{TCP}	2/7t_{TCP} + t_{TSUP}	ps
t_{TOP5}	LVDS data output position 5	—	3/7t_{TCP} - t_{THLD}	3/7 t_{TCP}	3/7t_{TCP} + t_{TSUP}	
t_{TOP4}	LVDS data output position 4	—	4/7t_{TCP} - t_{THLD}	4/7 t_{TCP}	4/7t_{TCP} + t_{TSUP}	
t_{TOP3}	LVDS data output position 3	—	5/7t_{TCP} - t_{THLD}	5/7 t_{TCP}	5/7t_{TCP} + t_{TSUP}	
t_{TOP2}	LVDS data output position 2	—	6/7t_{TCP} - t_{THLD}	6/7 t_{TCP}	6/7t_{TCP} + t_{TSUP}	
t_{TOP1}	LVDS data output position 1	—	7/7t_{TCP} - t_{THLD}	7/7 t_{TCP}	7/7t_{TCP} + t_{TSUP}	
t_{TOP0}	LVDS data output position 0	—	8/7t_{TCP} - t_{THLD}	8/7 t_{TCP}	8/7t_{TCP} + t_{TSUP}	
t_{LVT}	LVDS Transition Time (Fig7)	—	—	0.6	1.5	ns

LVDS Transmitter Output Timing



Ty1+/- output timing is the one between TCLK1+/- and Ty1+/-.

Ty2+/- output timing is the one between TCLK2+/- and Ty2+/-.

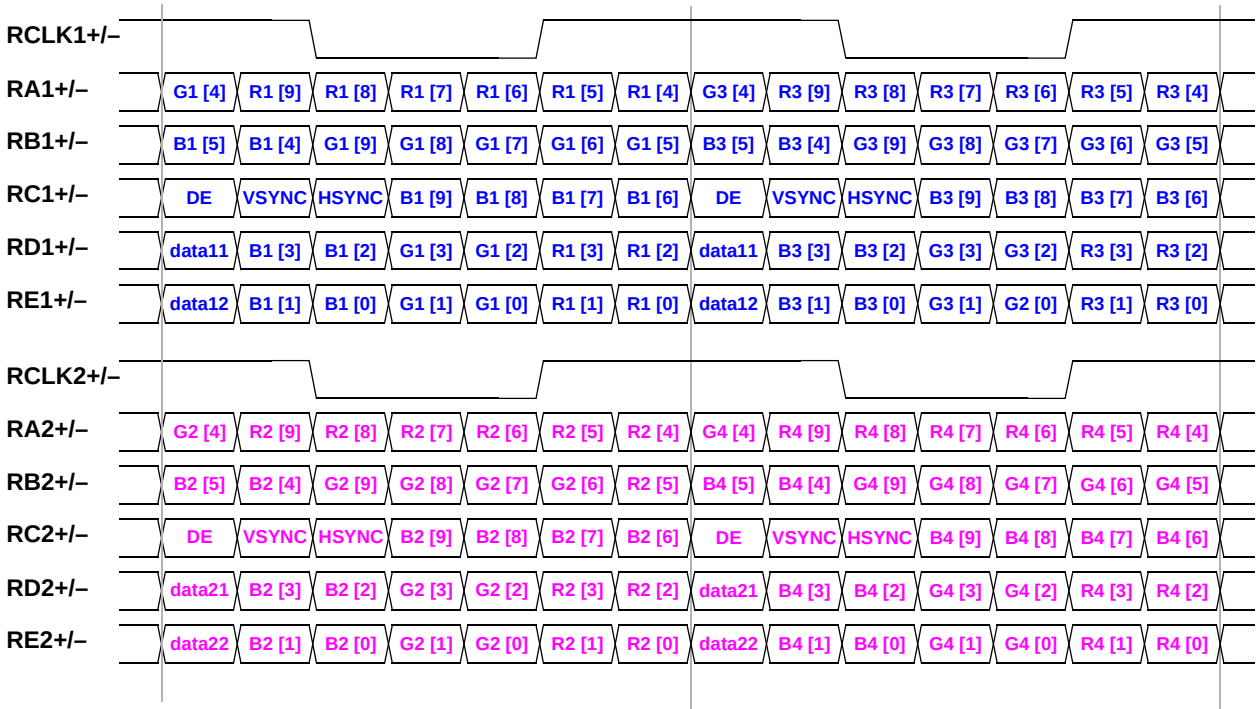


Note:
1) Vdifft = (Tyx+) - (Tyx-)
x= A, B, C, CLK, D, E
y=1,2

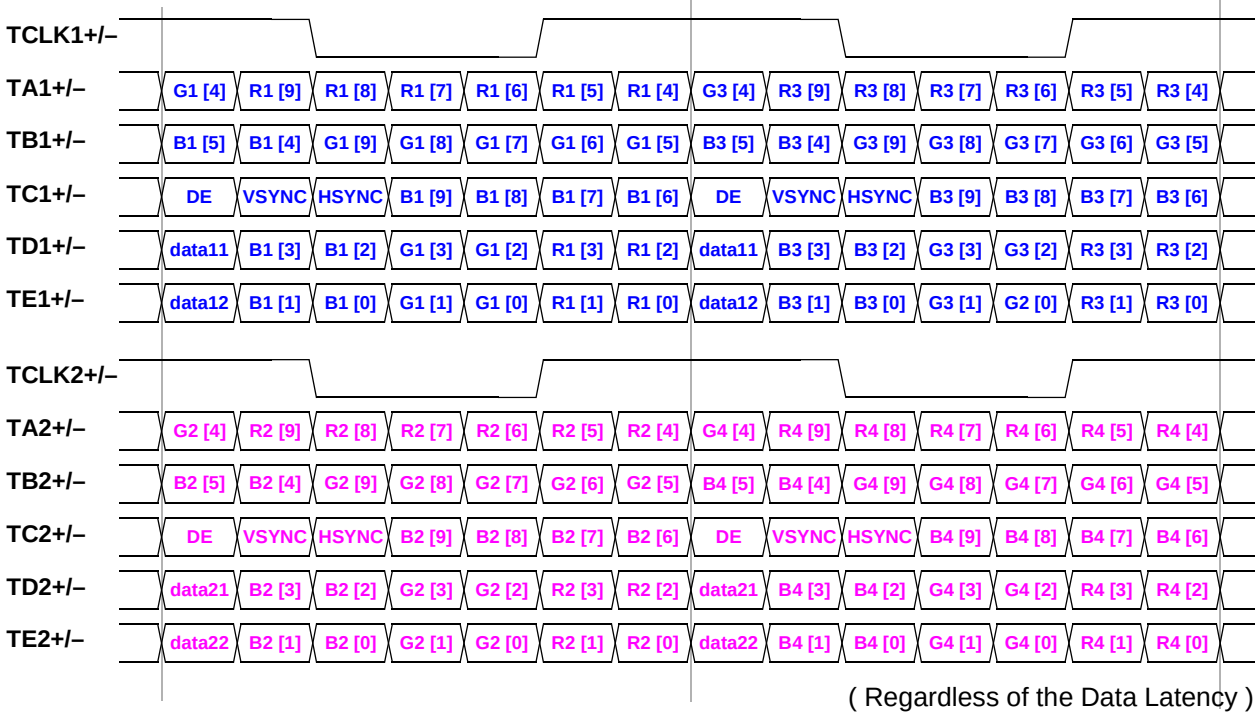
Fig7. LVDS Transition Time

LVDS Data Mapping
Dual-in / Dual-out mode

LVDS-Rx Input Mapping



LVDS-Tx Output Mapping



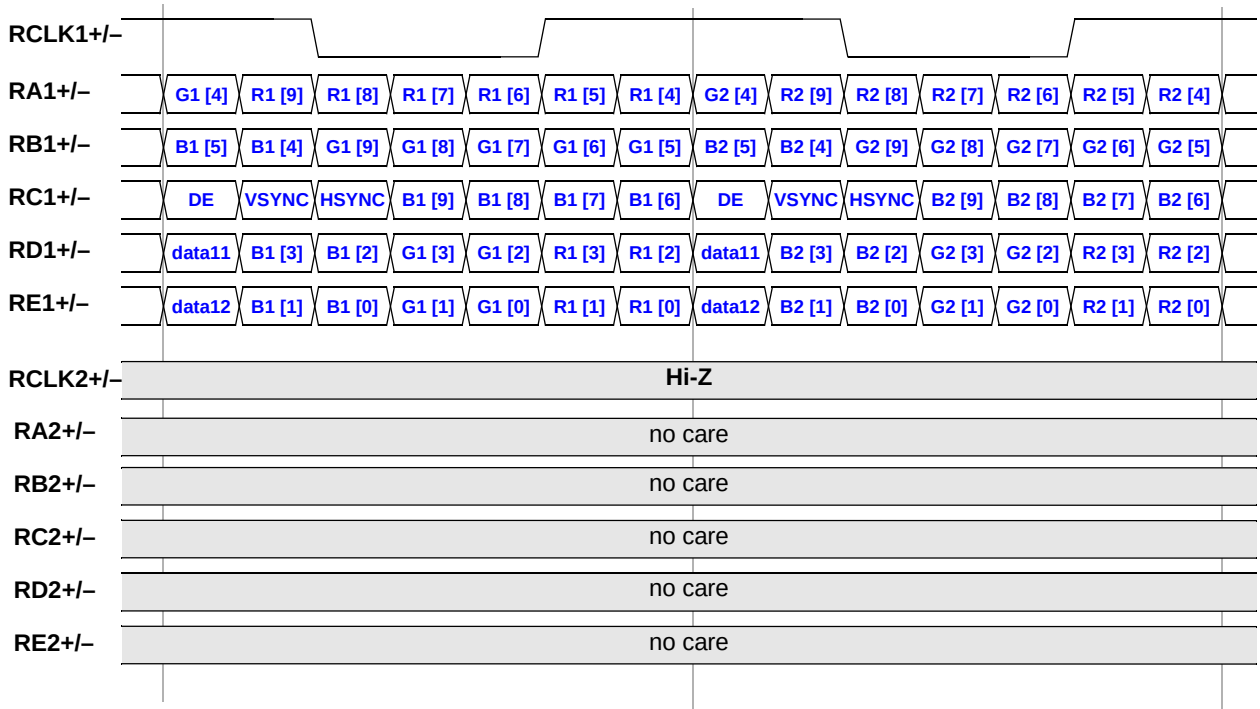
(Regardless of the Data Latency)

Data bits “data11, data12, data21, data22” are available for additional data transmission.

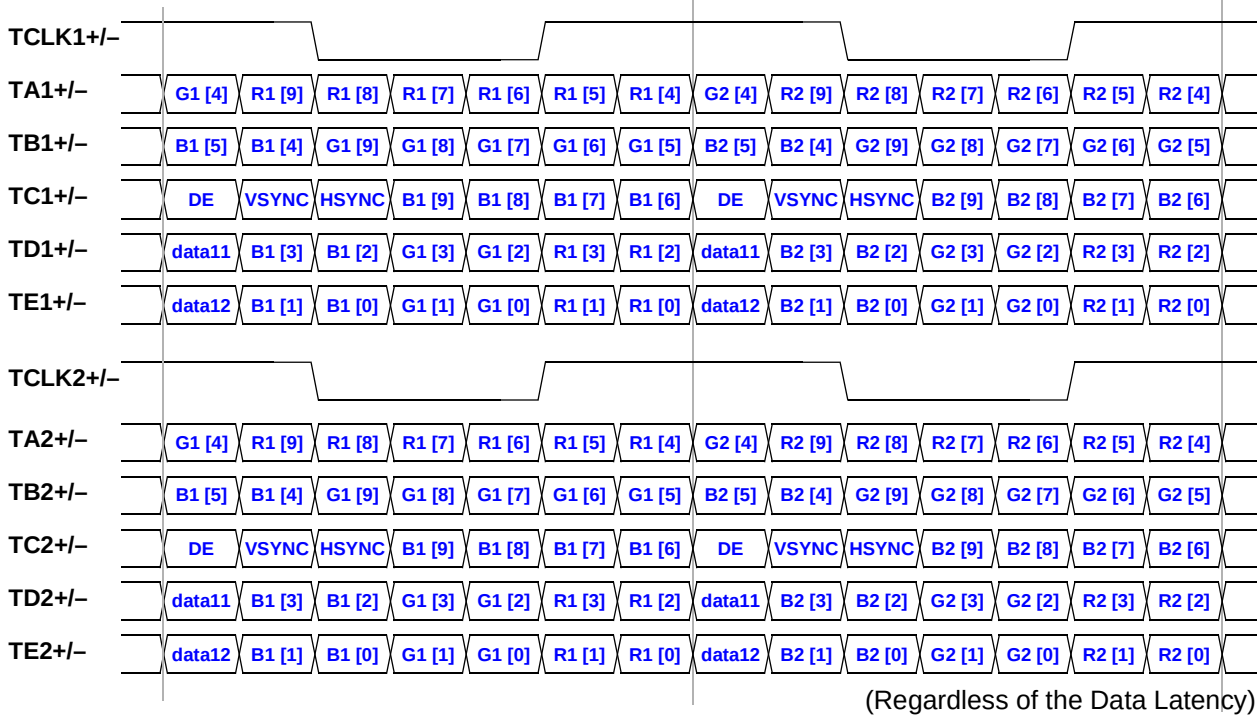
Distribution Mode

In Distribution mode, RCLK2+/- must be High-Z.

LVDS-Rx Input Mapping



LVDS-Tx Output Mapping



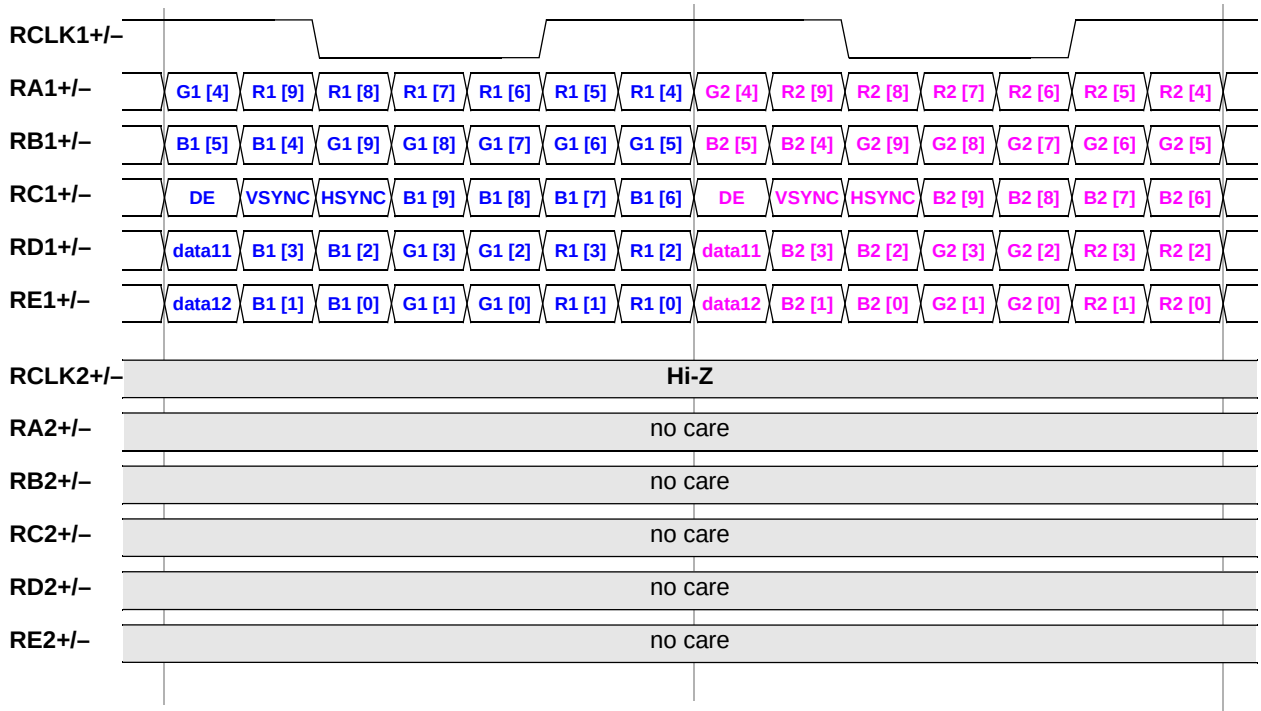
(Regardless of the Data Latency)

Data bits “data11, data12” are available for additional data transmission.

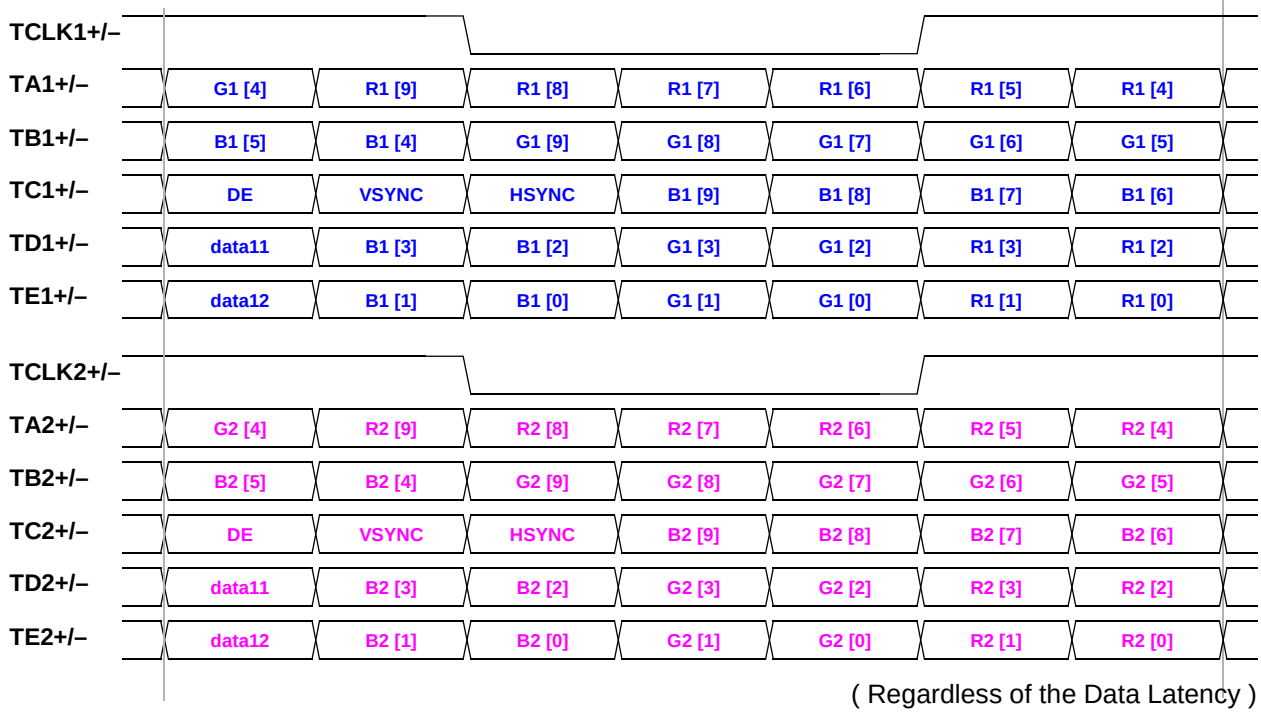
Single-in / Dual-out mode

In Single-in / Dual-out mode, RCLK2+/- must be High-Z.

LVDS-Rx Input Mapping



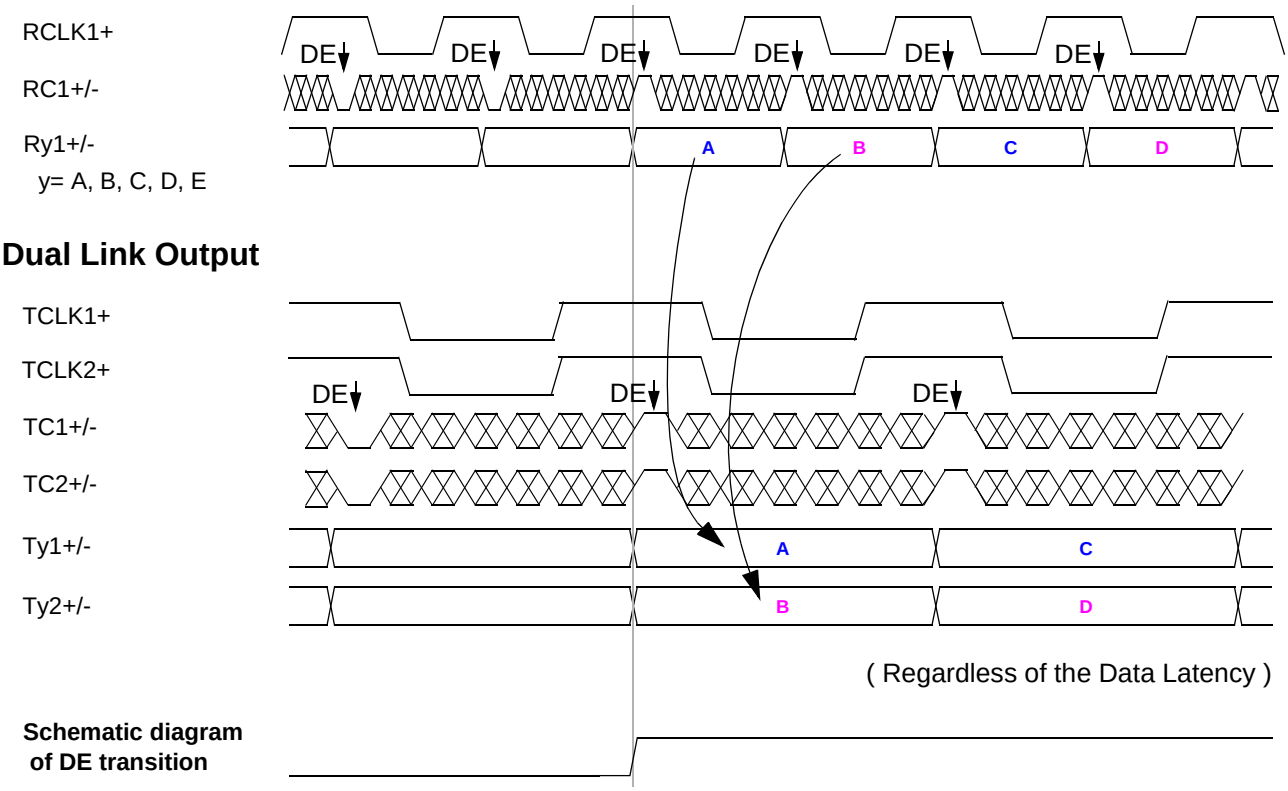
LVDS-Tx Output Mapping



(Regardless of the Data Latency)

Data bits “data11, data12” are available for additional data transmission.

Single Link Input



Dual Link Output

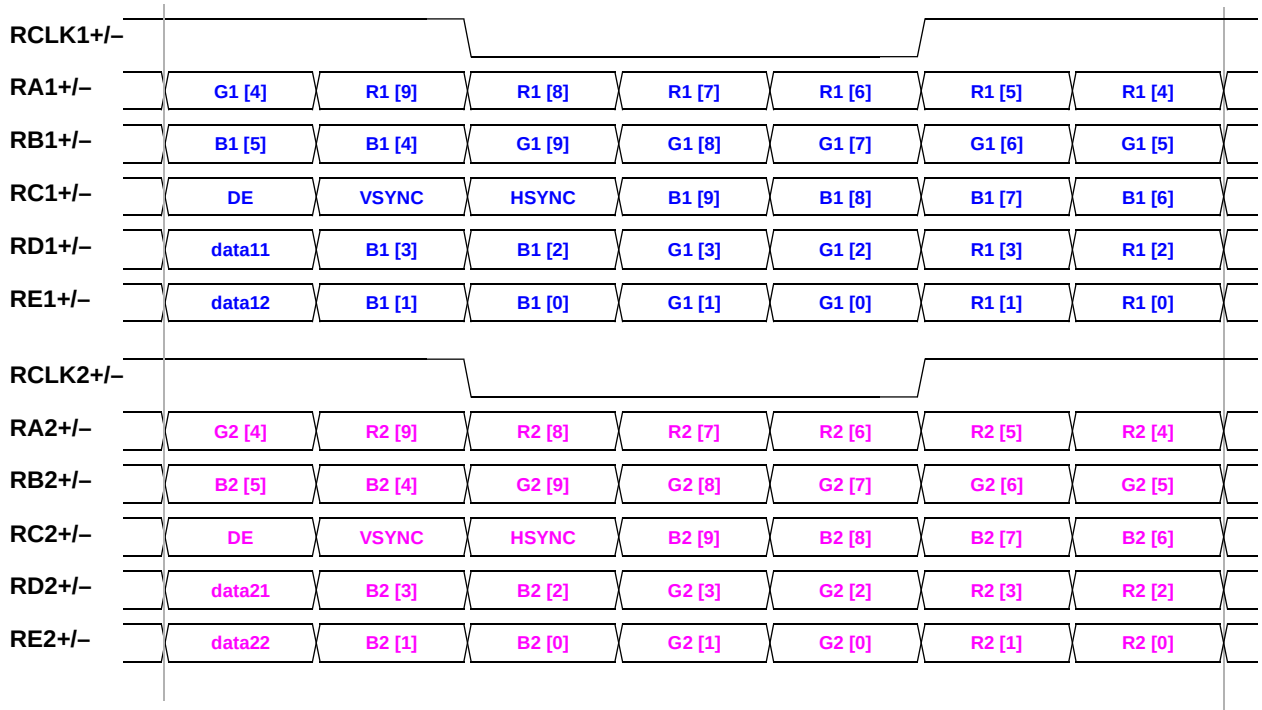
(Regardless of the Data Latency)

Schematic diagram of DE transition

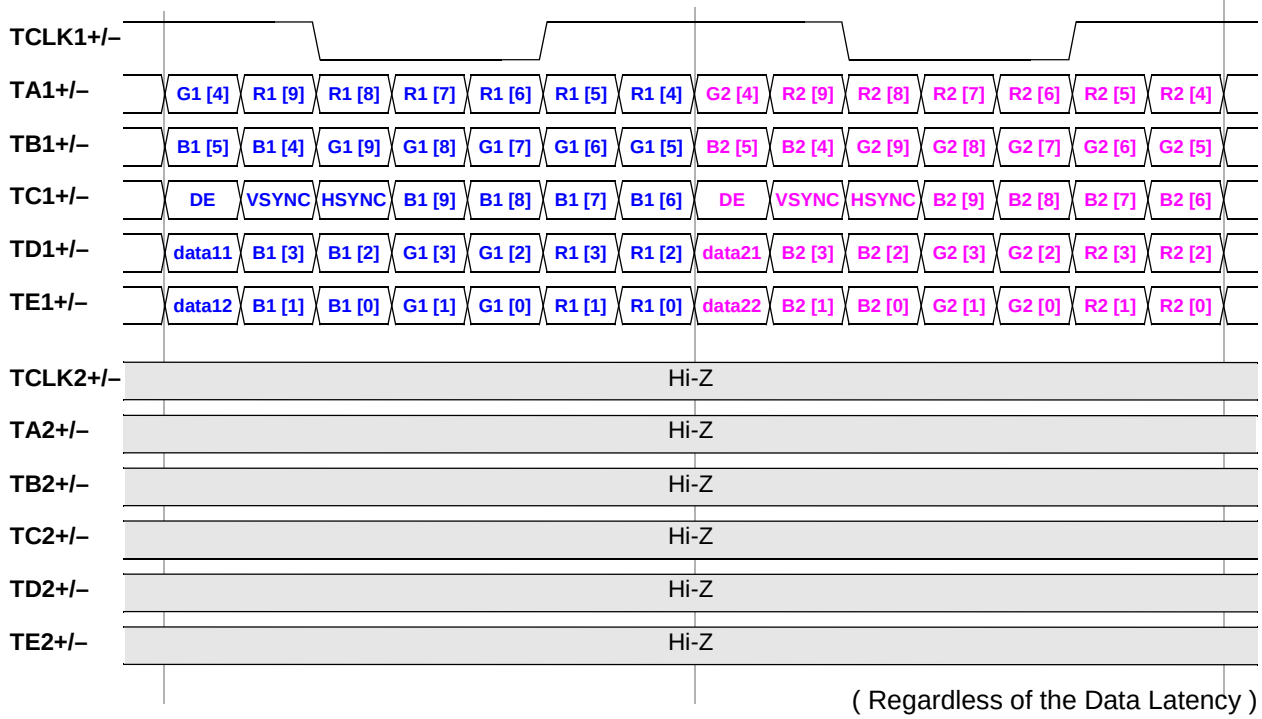
Single-in / Dual-out mode uses DE signal L-to-H-edge to start distribution of input data.

Dual-in / Single-out mode

LVDS-Rx Input Mapping



LVDS-Tx Output Mapping



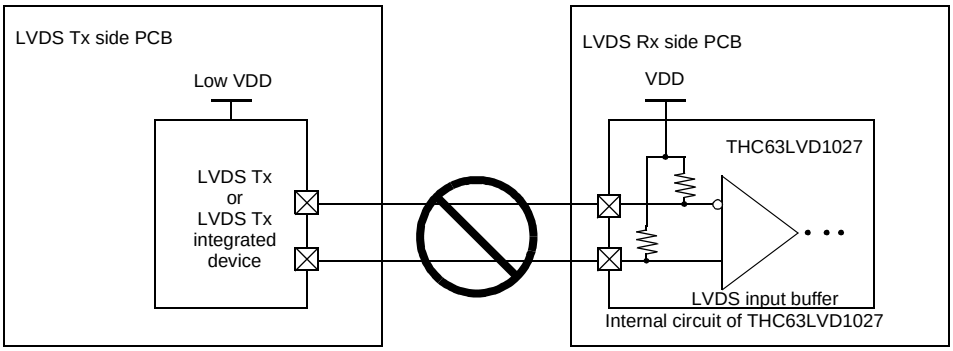
(Regardless of the Data Latency)

Data bits “data11, data12, data21, data22” are available for additional data transmission.

Note

1)LVDS input pin connection

When LVDS line is not drived from the previous device, the line is pulled up to 3.3V internally in THC63LVD1027. This can cause violation of absolute maximum ratings to the previous LVDS Tx device whose operating condition is lower voltage power supply than 3.3V. This phenomenon may happen at power on phase of the whole system including THC63LVD1027. One solution for this problem is PD=L control during no LVDS input period because pull-up resistors are cut off at power down state.



2)Power On Sequence

Don't input RCLK#+/- before THC63LVD1027 is on in order to keep absolute maximum ratings.

3)Cable Connection and Disconnection

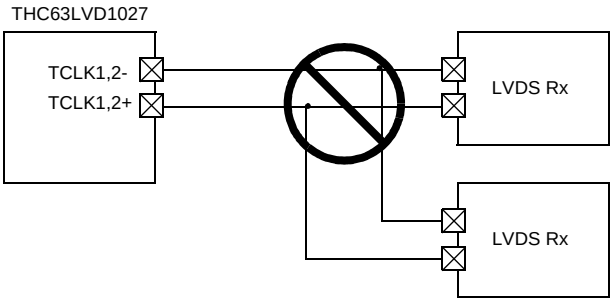
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

4)GND Connection

Connect the each GND of the PCB which Transmitter, Receiver and THC63LVD1027 on it.
It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

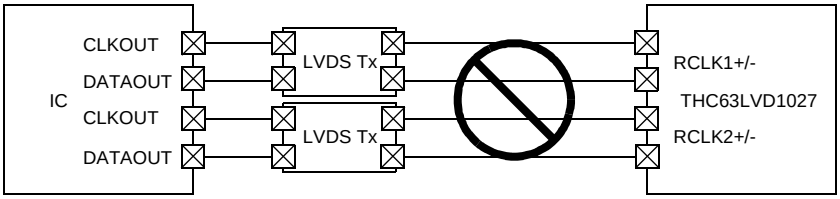
5)Multi Drop Connection

Multi drop connection is not recommended.



6)Asynchronous use

Asynchronous use such as following systems are not recommended.
Page.11 tCK12 spec should be kept.



Asynchronous use such as following systems are not recommended.