

# THC63LVDF84B

LVDS 24Bit COLOR HOST-LCD PANEL INTERFACE RECEIVER (Falling Edge Clock)

## General Description

The THC63LVDF84B receiver supports wide VCC range(2.5~3.6V). At single 2.5V supply, the THC63LVDF84B reduces EMI and power consumption.

The THC63LVDF84B receiver convert the four LVDS (Low Voltage Differential Signaling) data streams back into 24bits of CMOS/TTL data with falling edge clock. At a transmit clock frequency of 85MHz, 24bits of RGB data and 4bits of LCD timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at a rate of 2.3Gbps.

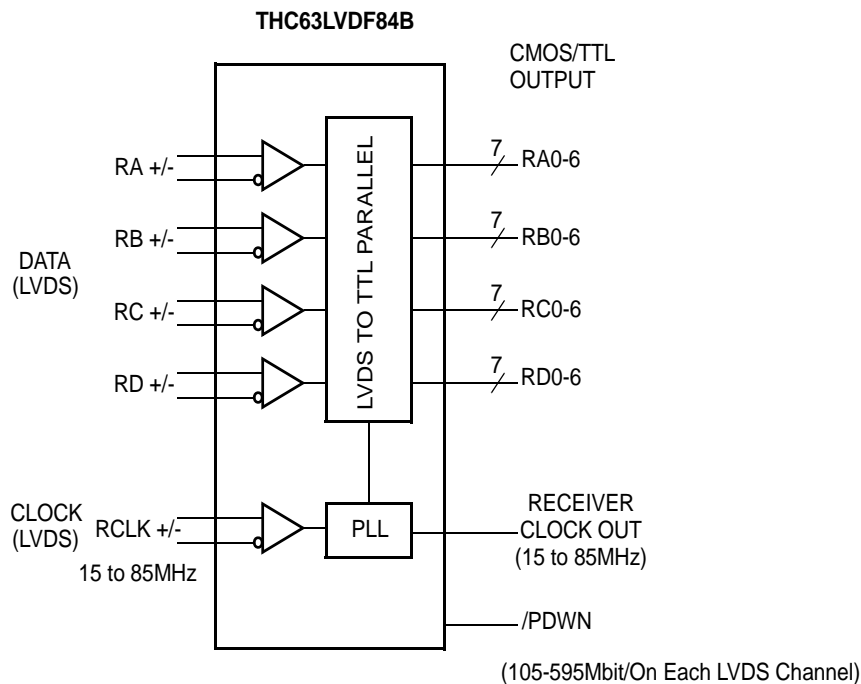
## Features

| VCC[V]     | Clock Frequency[MHz] |           |           |
|------------|----------------------|-----------|-----------|
|            | 15 to 20             | 20 to 70  | 70 to 85  |
| 2.5 to 2.7 | n/a                  | available | n/a       |
| 2.7 to 3.0 | available            | available | n/a       |
| 3.0 to 3.6 | available            | available | available |

n/a : not available

- Wide dot clock and Wide VCC range:
- Falling Edge Clock
- PLL requires No external components
- Rx power consumption < 80mW @VCC 2.5V, 65MHz Grayscale
- Power-Down Mode
- Low profile 56 Lead TSSOP Package
- Pin compatible with THC63LVDF84A

## Block Diagram



## Pin Out

**THC63LVDF84B**

|         |    |    |     |
|---------|----|----|-----|
| RC3     | 1  | 56 | VCC |
| RD6     | 2  | 55 | RC2 |
| RC4     | 3  | 54 | RC1 |
| GND     | 4  | 53 | RC0 |
| RC5     | 5  | 52 | GND |
| RC6     | 6  | 51 | RB6 |
| RD0     | 7  | 50 | RD5 |
| LVDSGND | 8  | 49 | RD4 |
| RA-     | 9  | 48 | VCC |
| RA+     | 10 | 47 | RB5 |
| RB-     | 11 | 46 | RB4 |
| RB+     | 12 | 45 | RB3 |
| LVDSVCC | 13 | 44 | GND |
| LVDSGND | 14 | 43 | RB2 |
| RC-     | 15 | 42 | RD3 |
| RC+     | 16 | 41 | RD2 |
| RCLK-   | 17 | 40 | VCC |
| RCLK+   | 18 | 39 | RB1 |
| RD-     | 19 | 38 | RB0 |
| RD+     | 20 | 37 | RA6 |
| LVDSGND | 21 | 36 | GND |
| PLLGND  | 22 | 35 | RA5 |
| PLLVCC  | 23 | 34 | RD1 |
| PLLGND  | 24 | 33 | RA4 |
| /PDWN   | 25 | 32 | RA3 |
| CLKOUT  | 26 | 31 | VCC |
| RA0     | 27 | 30 | RA2 |
| GND     | 28 | 29 | RA1 |

## Pin Description

| Pin Name     | Pin #                | Type    | Description   |
|--------------|----------------------|---------|---|
| RA+, RA-     | 10, 9                | LVDS IN | LVDS Data Inputs  |
| RB+, RB-     | 12, 11               | LVDS IN |   |
| RC+, RC-     | 16, 15               | LVDS IN |   |
| RD+, RD-     | 20, 19               | LVDS IN |   |
| RCLK+, RCLK- | 18, 17               | LVDS IN | LVDS Clock Inputs   |
| RA0~RA6      | 27,29,30,32,33,35,37 | OUT     | Pixel Data Outputs  |
| RB0~RB6      | 38,39,43,45,46,47,51 | OUT     |   |
| RC0~RC6      | 53,54,55,1,3,5,6     | OUT     |   |
| RD0~RD6      | 7,34,41,42,49,50,2   | OUT     |   |
| CLKOUT       | 26                   | OUT     | Pixel Clock Output  |
| /PDWN        | 25                   | IN      | H: Normal operation<br>L: Power down (all outputs are pulled to ground) |
| VCC          | 31,40,48,56          | Power   | Power Supply Pins for TTL outputs and digital circuitry                 |
| GND          | 4,28,36,44,52        | Ground  | Ground Pins for TTL outputs and digital circuitry                       |
| LVDSVCC      | 13                   | Power   | Power Supply Pin for LVDS inputs  |
| LVDSGND      | 8,14,21              | Ground  | Ground Pins for LVDS inputs   |
| PLLVCC       | 23                   | Power   | Power Supply Pin for PLL circuitry                                      |
| PLLGND       | 22,24                | Ground  | Ground Pins for PLL circuitry   |

## Absolute Maximum Ratings

|                                  |                             |
|----------------------------------|-----------------------------|
| Supply Voltage ( $V_{CC}$ )      | -0.3V ~ +4.0V               |
| CMOS/TTL Input Voltage           | -0.3V ~ ( $V_{CC} + 0.3V$ ) |
| CMOS/TTL Output Voltage          | -0.3V ~ ( $V_{CC} + 0.3V$ ) |
| LVDS Receiver Input Voltage      | -0.3V ~ ( $V_{CC} + 0.3V$ ) |
| Junction Temperature             | +125°C                      |
| Storage Temperature Range        | -55°C ~ +150°C              |
| Reflow Peak Temperature / Time   | +260°C / 10sec.             |
| Maximum Power Dissipation @+25°C | 1.9W                        |

## Recommended Operating Conditions

| Parameter                     |                  | Min. | Max. | Units |
|-------------------------------|------------------|------|------|-------|
| All Supply Voltage            |                  | 2.5  | 3.6  | V     |
| Operating Ambient Temperature |                  | -10  | 70   | °C    |
| Clock Frequency               | VCC=2.5V to 2.7V | 20   | 70   | MHz   |
|                               | VCC=2.7V to 3.0V | 15   | 70   | MHz   |
|                               | VCC=3.0V to 3.6V | 15   | 85   | MHz   |

## Electrical Characteristics

### CMOS/TTL DC SPECIFICATIONS

 $V_{CC} = V_{CC} = PV_{CC} = LV_{CC}$ 

| Symbol    | Parameter                 | Conditions                       | Min. | Typ. | Max. | Units |
|-----------|---------------------------|----------------------------------|------|------|------|-------|
| $V_{IH}$  | High Level Input Voltage  |                                  | 2.0  |      | VCC  | V     |
| $V_{IL}$  | Low Level Input Voltage   |                                  | GND  |      | 0.8  | V     |
| $V_{OH1}$ | High Level Output Voltage | VCC= 3.0V ~ 3.6V $I_{OH} = -4mA$ | 2.4  |      |      | V     |
| $V_{OL1}$ | Low Level Output Voltage  | VCC = 3.0V ~ 3.6V $I_{OL} = 4mA$ |      |      | 0.4  | V     |
| $V_{OH2}$ | High Level Output Voltage | VCC= 2.5V ~ 3.0V $I_{OH} = -2mA$ | 2.1  |      |      | V     |
| $V_{OL2}$ | Low Level Output Voltage  | VCC = 2.5V ~ 3.0V $I_{OL} = 2mA$ |      |      | 0.4  | V     |
| $I_{IN}$  | Input Current             | $0V \leq V_{IN} \leq V_{CC}$     |      |      | ±10  | μA    |

## LVDS RECEIVER DC SPECIFICATIONS

V<sub>CC</sub> = V<sub>CC</sub> = PV<sub>CC</sub> = LV<sub>CC</sub>

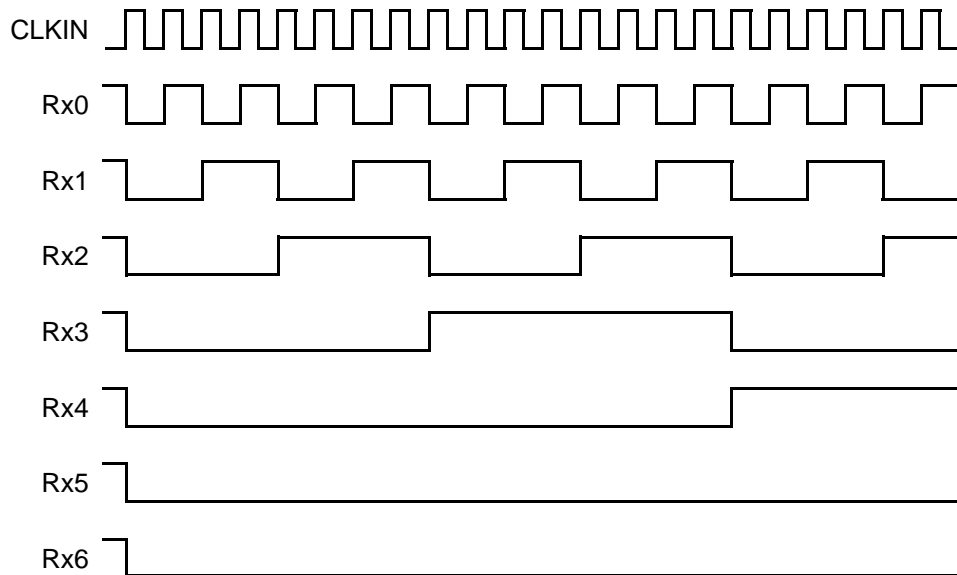
| Symbol          | Parameter                         | Conditions   | Min. | Typ. | Max. | Units |
|-----------------|-----------------------------------|--|------|------|------|-------|
| V <sub>TH</sub> | Differential Input High Threshold | VIC = +1.2V  |      |      | 100  | mV    |
| V <sub>TL</sub> | Differential Input Low Threshold  |  | -100 |      |      | mV    |
| I <sub>IN</sub> | Input Current                     | V <sub>IN</sub> = +2.4V/0V<br>V <sub>CC</sub> = 3.6V |      |      | ±10  | μA    |

## Supply Current

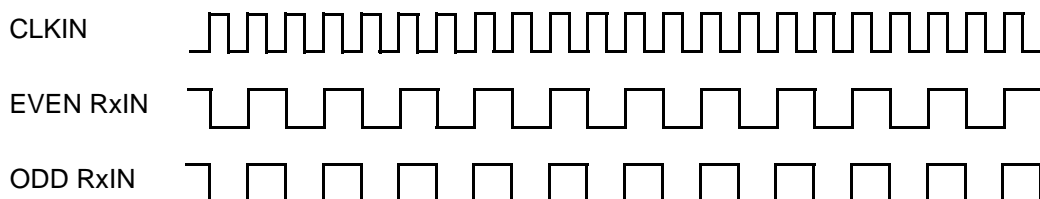
V<sub>CC</sub> = V<sub>CC</sub> = PV<sub>CC</sub> = LV<sub>CC</sub>

| Symbol            | Parameter                                      | Condition(*)     | Typ.      | Max. | Units |    |
|-------------------|--|------------------|-----------|------|-------|----|
| I <sub>RCCG</sub> | Receiver Supply Current<br>16Grayscale Pattern | CL=8pF, VCC=3.3V | f = 65MHz | 41   | 53    | mA |
|                   |  |                  | f = 85MHz | 52   | 64    | mA |
|                   |  | CL=8pF, VCC=2.5V | f = 65MHz | 30   | 42    | mA |
| I <sub>RCCW</sub> | Receiver Supply Current<br>Worst Case Pattern  | CL=8pF, VCC=3.3V | f = 65MHz | 72   | 94    | mA |
|                   |  |                  | f = 85MHz | 84   | 96    | mA |
|                   |  | CL=8pF, VCC=2.5V | f = 65MHz | 42   | 64    | mA |
| I <sub>RCCS</sub> | Receiver Power Down<br>Supply Current          | /PDWN = L        |           | 10   | μA    |    |

### 16 Gray Scale Pattern



### Worst Case Pattern



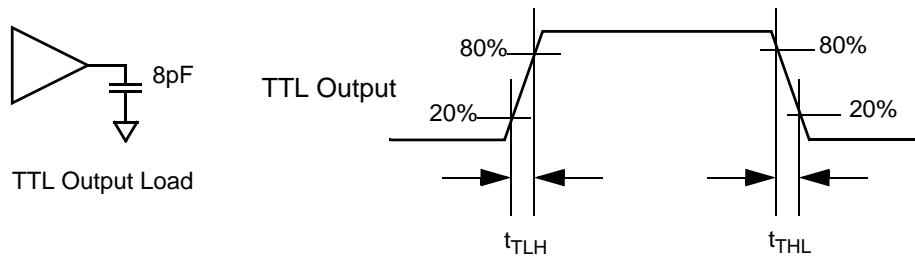
### Switching Characteristics

V<sub>CC</sub> = V<sub>CC</sub> = PV<sub>CC</sub> = LV<sub>CC</sub>

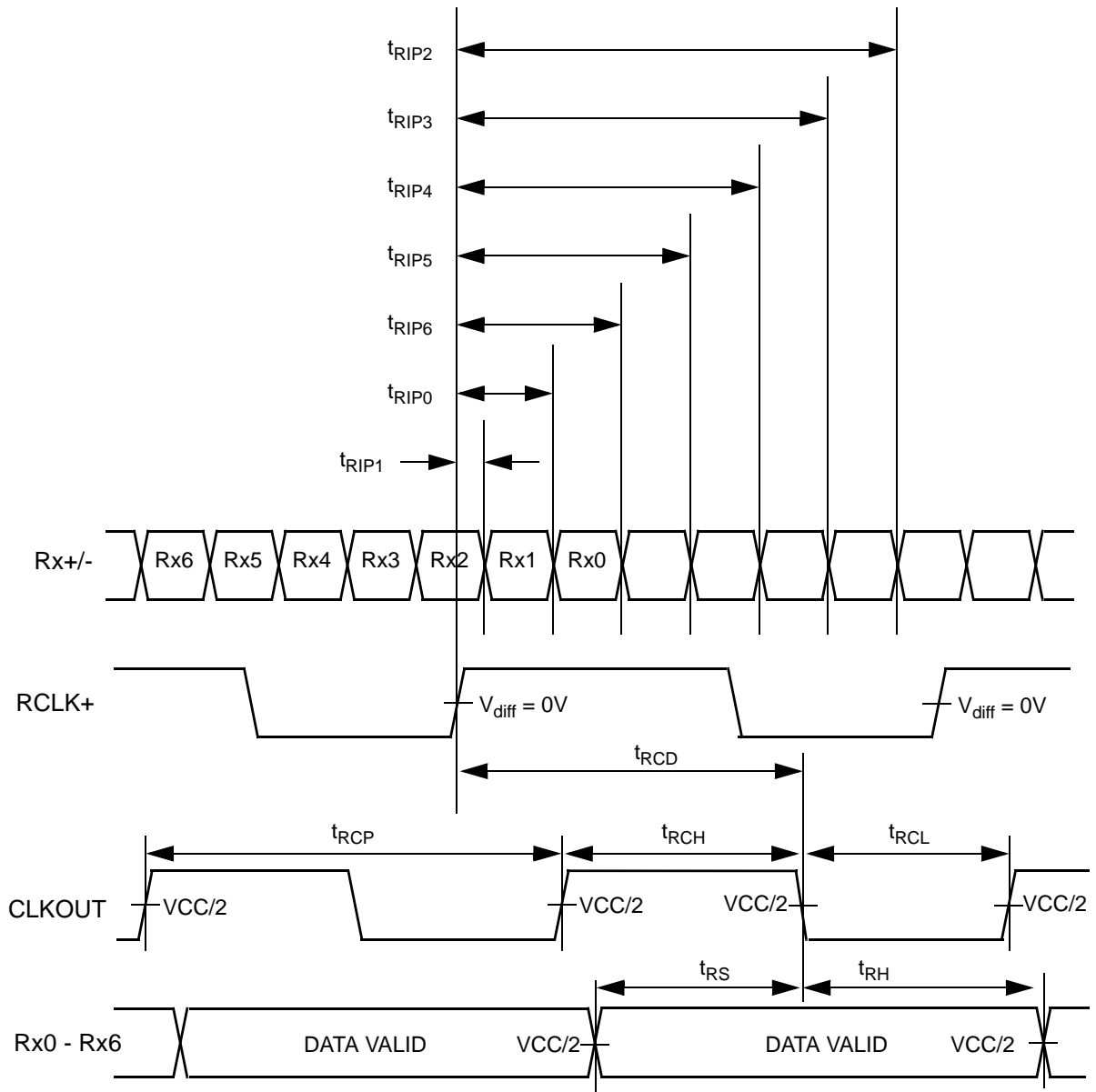
| Symbol            | Parameter                          | Min.                         | Typ. | Max.     | Units |    |
|-------------------|------------------------------------|------------------------------|------|----------|-------|----|
| t <sub>RCP</sub>  | CLK OUT Period                     | V <sub>CC</sub> = 2.5 - 2.7V | 14.3 | T        | 50.0  | ns |
|                   |                                    | V <sub>CC</sub> = 2.7 - 3.0V | 14.3 | T        | 66.6  | ns |
|                   |                                    | V <sub>CC</sub> = 3.0 - 3.6V | 11.8 | T        | 66.6  | ns |
| t <sub>RCH</sub>  | CLK OUT High Time                  |                              | 4T/7 |          | ns    |    |
| t <sub>RCL</sub>  | CLK OUT Low Time                   |                              | 3T/7 |          | ns    |    |
| t <sub>RCD</sub>  | RCLK +/- to CLK OUT Delay          |                              | 5T/7 |          | ns    |    |
| t <sub>RS</sub>   | TTL Data Setup to CLK OUT          | 0.35T-0.3                    |      |          | ns    |    |
| t <sub>RH</sub>   | TTL Data Hold from CKL OUT         | 0.45T-1.6                    |      |          | ns    |    |
| t <sub>TLH</sub>  | TTL Low to High Transition Time    |                              | 2.0  | 3.0      | ns    |    |
| t <sub>THL</sub>  | TTL High to Low Transition Time    |                              | 1.8  | 3.0      | ns    |    |
| t <sub>RIP1</sub> | Input Data Position0 (T = 11.76ns) | -0.4                         | 0.0  | 0.4      | ns    |    |
| t <sub>RIP0</sub> | Input Data Position1 (T = 11.76ns) | T/7-0.4                      | T/7  | T/7+0.4  | ns    |    |
| t <sub>RIP6</sub> | Input Data Position2 (T = 11.76ns) | 2T/7-0.4                     | 2T/7 | 2T/7+0.4 | ns    |    |
| t <sub>RIP5</sub> | Input Data Position3 (T = 11.76ns) | 3T/7-0.4                     | 3T/7 | 3T/7+0.4 | ns    |    |
| t <sub>RIP4</sub> | Input Data Position4 (T = 11.76ns) | 4T/7-0.4                     | 4T/7 | 4T/7+0.4 | ns    |    |
| t <sub>RIP3</sub> | Input Data Position5 (T = 11.76ns) | 5T/7-0.4                     | 5T/7 | 5T/7+0.4 | ns    |    |
| t <sub>RIP2</sub> | Input Data Position6 (T = 11.76ns) | 6T/7-0.4                     | 6T/7 | 6T/7+0.4 | ns    |    |
| t <sub>RPLL</sub> | Phase Lock Loop Set                |                              |      | 10.0     | ms    |    |

### AC Timing Diagrams

#### TTL Output



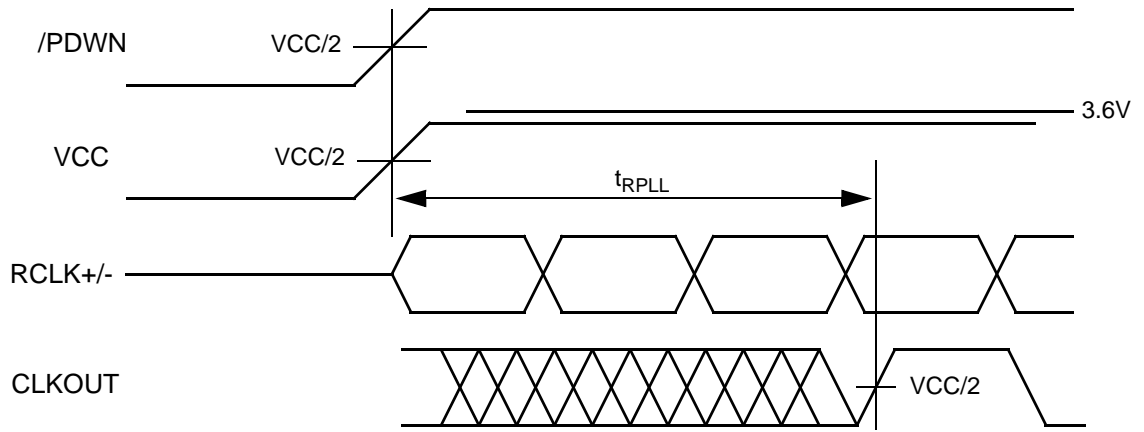
### AC Timing Diagrams



Note:  
 1)  $V_{diff} = (RA+) - (RA-), \dots, (RCLK+) - (RCLK-)$

### AC Timing Diagrams

#### Phase Lock Loop Set Time



Note

1)Power On Sequence

Power on LVDS-Tx after THC63LVDF84B.

2)Cable Connection and Disconnection

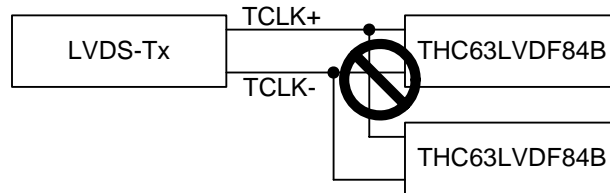
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

3)GND Connection

Connect the each GND of the PCB which LVDS-Tx and THC63LVDF84B on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

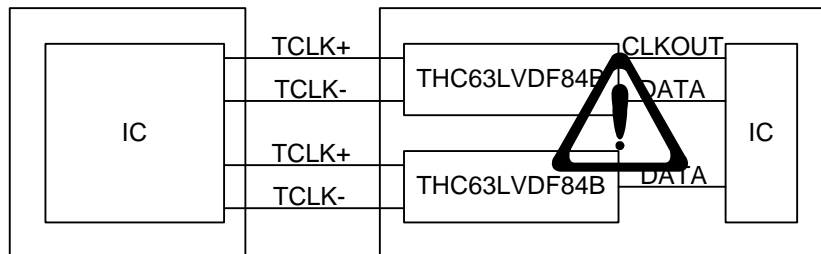
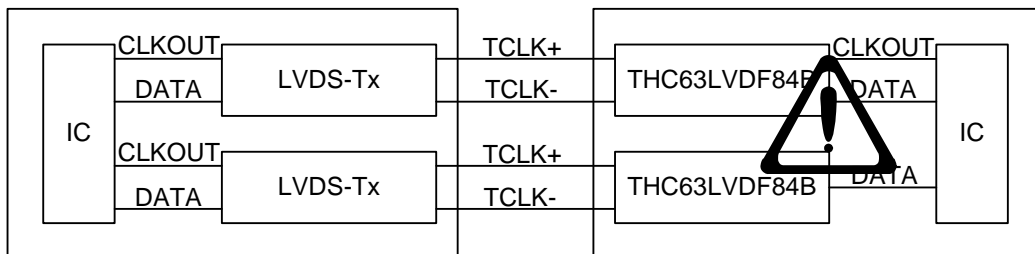
4)Multi Drop Connection

Multi drop connection is not recommended.

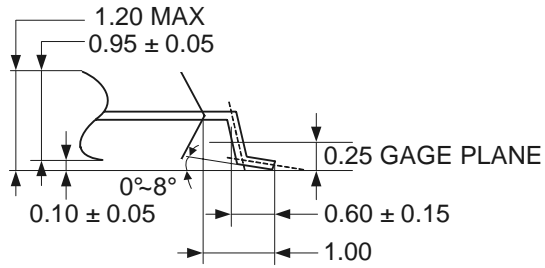
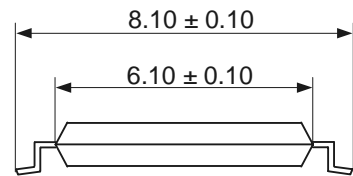
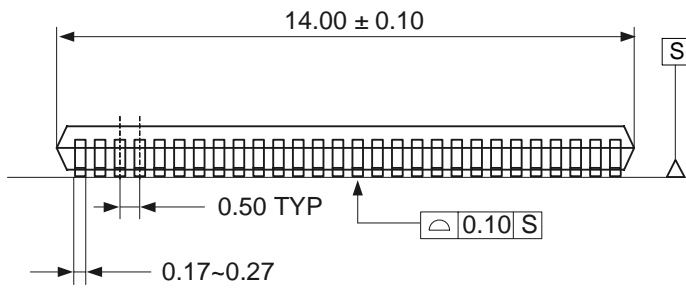


5)Asynchronous use

Asynchronous use such as following systems are not recommended.



# Package



Detail of Lead End

Unit:mm

## Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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