THC63LVD103D

160MHz 30Bits COLOR LVDS Transmitter

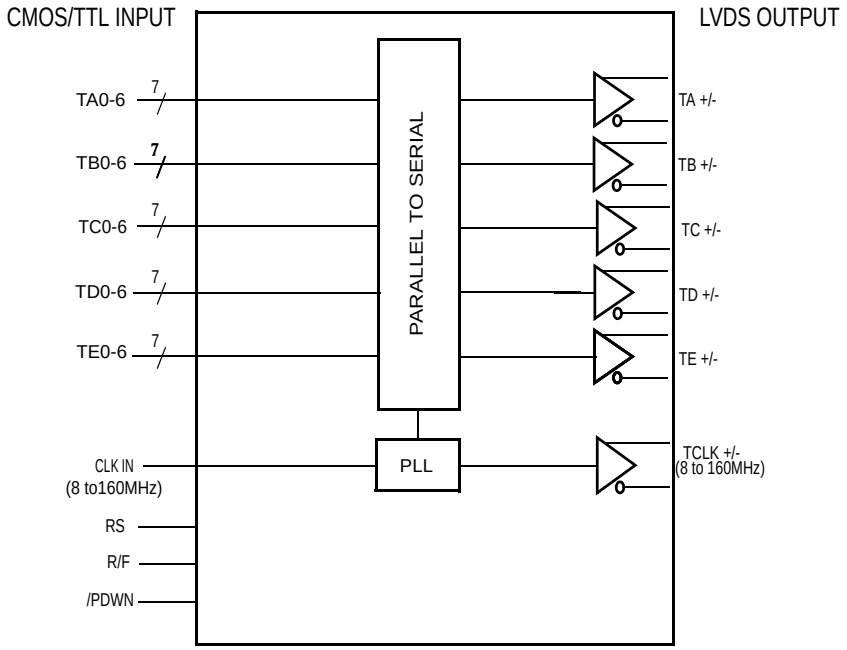
General Description

The THC63LVD103D transmitter is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to 1080p(60Hz).
The THC63LVD103D converts 35bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 160MHz, 30bits of RGB data and 5bits of timing and control data (HSYNC, VSYNC, DE, CNTL1, CNTL2) are transmitted at an effective rate of 1.12Gbps per LVDS channel.

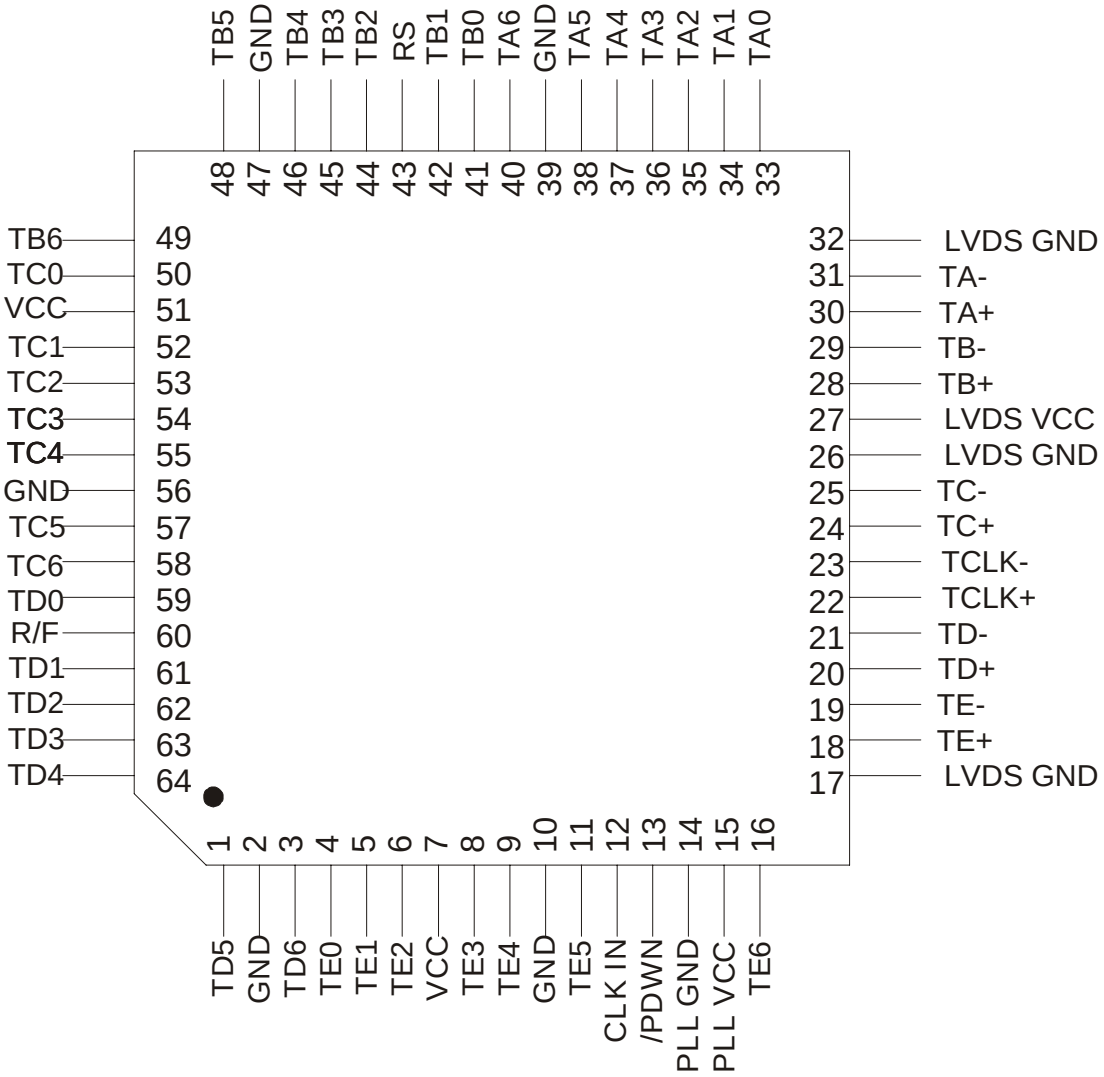
Features

- Wide dot clock range: 8-160MHz suited for NTSC, VGA, SVGA, XGA,SXGA and SXGA+ and 1080p
- PLL requires no external components
- Supports spread spectrum clock generator
- On chip jitter filtering
- Clock edge selectable
- Supports reduced swing LVDS for low EMI
- Power down mode
- Low power single 3.3V CMOS design
- 64pin TQFP
- Pin compatible with THC63LVD103(30bits)

Block Diagram



Pin Out


TB5 GND TB4 TB3 TB2 RS TB1 TB0 TA6 GND TA5 TA4 TA3 TA2 TA1 TA0
48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
TB6 49
TC0 50
VCC 51
TC1 52
TC2 53
TC3 54
TC4 55
GND 56
TC5 57
TC6 58
TD0 59
R/F 60
TD1 61
TD2 62
TD3 63
TD4 64
32 LVDS GND
31 TA-
30 TA+
29 TB-
28 TB+
27 LVDS VCC
26 LVDS GND
25 TC-
24 TC+
23 TCLK-
22 TCLK+
21 TD-
20 TD+
19 TE-
18 TE+
17 LVDS GND
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16
TD5 GND TD6 TE0 TE1 TE2 VCC TE3 TE4 GND TE5 CLK IN /PDWN PLL GND PLL VCC TE6

Pin Description

<table>
<tr><th>Pin Name</th><th>Pin #</th><th>Type</th><th>Description</th></tr>
<tr><td>TA+, TA-</td><td>30, 31</td><td>LVDS OUT</td><td rowspan="5">LVDS Data Out.</td></tr>
<tr><td>TB+, TB-</td><td>28, 29</td><td>LVDS OUT</td></tr>
<tr><td>TC+, TC-</td><td>24, 25</td><td>LVDS OUT</td></tr>
<tr><td>TD+, TD-</td><td>20, 21</td><td>LVDS OUT</td></tr>
<tr><td>TE+,TE-</td><td>18, 19</td><td>LVDS OUT</td></tr>
<tr><td>TCLK+,
TCLK-</td><td>22, 23</td><td>LVDS OUT</td><td>LVDS Clock Out.</td></tr>
<tr><td>TA0 ~ TA6</td><td>33,34,35,36,37,38,40</td><td>IN</td><td rowspan="5">Pixel Data Inputs.</td></tr>
<tr><td>TB0 ~ TB6</td><td>41,42,44,45,46,48,49</td><td>IN</td></tr>
<tr><td>TC0 ~ TC6</td><td>50,52,53,54,55,57,58</td><td>IN</td></tr>
<tr><td>TD0 ~ TD6</td><td>59,61,62,63,64,1,3</td><td>IN</td></tr>
<tr><td>TE0 ~ TE6</td><td>4,5,6,8,9,11,16</td><td>IN</td></tr>
<tr><td>/PDWN</td><td>13</td><td>IN</td><td>H: Normal operation,
L: Power down (all outputs are Hi-Z)</td></tr>
<tr><td>RS</td><td>43</td><td>IN</td><td>LVDS swing mode, VREF select.See Fig4, 5.
<table><tr><th>RS</th><th>LVDS Swing</th><th>Small Swing Input Support</th></tr><tr><td>VCC</td><td>350mV</td><td>N/A</td></tr><tr><td>0.6 ~ 1.4V</td><td>350mV</td><td>RS=VREF[a]</td></tr><tr><td>GND</td><td>200mV</td><td>N/A</td></tr></table>a. VREF is Input Reference Voltage.</td></tr>
<tr><td>R/F</td><td>60</td><td>IN</td><td>Input Clock Triggering Edge Select.
H: Rising edge, L: Falling edge</td></tr>
<tr><td>VCC</td><td>51, 7</td><td>Power</td><td>Power Supply Pins for TTL inputs and digital circuitry.</td></tr>
<tr><td>CLKIN</td><td>12</td><td>IN</td><td>Clock in.</td></tr>
<tr><td>GND</td><td>2, 10, 39, 47, 56</td><td>Ground</td><td>Ground Pins for TTL inputs and digital circuitry.</td></tr>
<tr><td>LVDS VCC</td><td>27</td><td>Power</td><td>Power Supply Pins for LVDS Outputs.</td></tr>
<tr><td>LVDS GND</td><td>17, 26, 32</td><td>Ground</td><td>Ground Pins for LVDS Outputs.</td></tr>
<tr><td>PLL VCC</td><td>15</td><td>Power</td><td>Power Supply Pin for PLL circuitry.</td></tr>
<tr><td>PLL GND</td><td>14</td><td>Ground</td><td>Ground Pins for PLL circuitry.</td></tr>
</table>

Absolute Maximum Ratings[1]

Supply Voltage (V_{CC})	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ (V_{CC} + 0.3V)
CMOS/TTL Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
LVDS Transmitter Output Voltage	-0.3V ~ (V_{CC} + 0.3V)
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	2.1W

1. "Absolute Maximum Ratings" are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of "Electrical Characteristics" specify conditions for device operation.

Electrical Characteristics

CMOS/TTL DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
V_{IH}	High Level Input Voltage	RS=VCC or GND	2.0		V_{CC}	V
V_{IL}	Low Level Input Voltage	RS=VCC or GND	GND		0.8	V
V_{DDQ}[1]	Small Swing Voltage		1.2		2.8	V
V_{REF}	Input Reference Voltage	Small Swing (RS=V_{DDQ}/2)		V_{DDQ}/2		
V_{SH}[2]	Small Swing High Level Input Voltage	V_{REF} = V_{DDQ}/2	V_{DDQ}/2 +100mV			V
V_{SL}[2]	Small Swing Low Level Input Voltage	V_{REF} = V_{DDQ}/2			V_{DDQ}/2 -100mV	V
I_{INC}	Input Current	$0V \le V_{IN} \le V_{CC}$			±10	μA

Notes: [1] V_{DDQ} voltage defines max voltage of small swing input. It is not an actual input voltage.
[2] Small swing signal is applied to TA[6:0], TB[6:0], TC[6:0], TD[6:0], TE[6:0] and CLKIN.

LVDS Transmitter DC Specifications

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Conditions		Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	RL=100Ω	Normal swing RS=VCC	250	350	450	mV
			Reduced swing RS=GND	100	200	300	mV
ΔVOD	Change in VOD between complementary output states	RL=100Ω				35	mV
VOC	Common Mode Voltage			1.125	1.25	1.375	V
ΔVOC	Change in VOC between complementary output states					35	mV
I_{OS}	Output Short Circuit Current	VOUT=0V, RL=100Ω				-24	mA
I_{OZ}	Output TRI-STATE Current	/PDWN=0V, V_{OUT}=0V to VCC				±10	μA

Supply Current

V_{CC} = 3.0V ~ 3.6V, Ta =0°C ~ +70°C

Symbol	Parameter	Conditions		Typ.	Max.	Units
I_{TCCW}	Transmitter Supply Current	RL=100Ω,CL=5pF V_{CC}=3.3V, RS=V_{CC} Worst Case Pattern	f=85MHz	69	75	mA
			f=135MHz	87	93	mA
			f=160MHz	97	104	mA
		RL=100Ω,CL=5pF V_{CC}=3.3V, RS=GND Worst Case Pattern	f=85MHz	55	61	mA
			f=135MHz	73	79	mA
			f=160MHz	83	89	mA
I_{TCCS}	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = L or H			10	μA

.

Worst Case Pattern

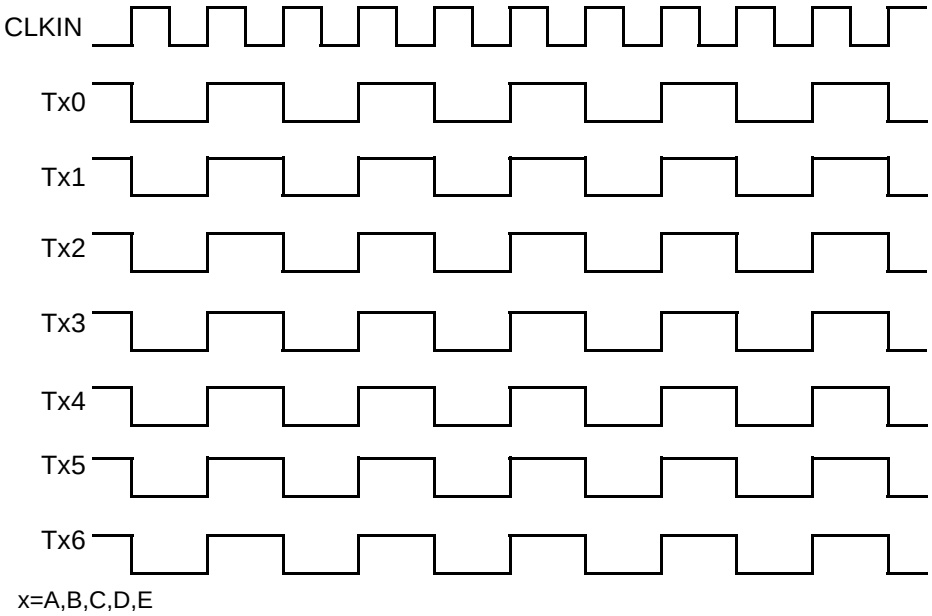


Fig1. Worst Case Pattern

Switching Characteristics

V_{CC} = 3.0V ~ 3.6V, Ta = 0°C ~ +70°C

Symbol	Parameter	Min.	Typ.	Max.	Units
t_{TCIT}	CLK IN Transition time			5.0	ns
t_{TCP}	CLK IN Period	6.25		125.0	ns
t_{TCH}	CLK IN High Time	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCL}	CLK IN Low Time	$0.35t_{TCP}$	$0.5t_{TCP}$	$0.65t_{TCP}$	ns
t_{TCD}	CLK IN to TCLK+/- Delay		$3t_{TCP}$		ns
t_{TS}	TTL Data Setup to CLK IN	2.0			ns
t_{TH}	TTL Data Hold from CKL IN	0.0			ns
t_{LVT}	LVDS Transition Time		0.6	1.5	ns
t_{TOP1}	Output Data Position0 (t_{TCP}=6.25ns~20ns)	-0.15	0.0	+0.15	ns
t_{TOP0}	Output Data Position1 (t_{TCP}=6.25ns~20ns)	$\frac{t_{TCP}}{7} - 0.15$	$\frac{t_{TCP}}{7}$	$\frac{t_{TCP}}{7} + 0.15$	ns
t_{TOP6}	Output Data Position2 (t_{TCP}=6.25ns~20ns)	$2\frac{t_{TCP}}{7} - 0.15$	$2\frac{t_{TCP}}{7}$	$2\frac{t_{TCP}}{7} + 0.15$	ns
t_{TOP5}	Output Data Position3 (t_{TCP}=6.25ns~20ns)	$3\frac{t_{TCP}}{7} - 0.15$	$3\frac{t_{TCP}}{7}$	$3\frac{t_{TCP}}{7} + 0.15$	ns
t_{TOP4}	Output Data Position4 (t_{TCP}=6.25ns~20ns)	$4\frac{t_{TCP}}{7} - 0.15$	$4\frac{t_{TCP}}{7}$	$4\frac{t_{TCP}}{7} + 0.15$	ns
t_{TOP3}	Output Data Position5 (t_{TCP}=6.25ns~20ns)	$5\frac{t_{TCP}}{7} - 0.15$	$5\frac{t_{TCP}}{7}$	$5\frac{t_{TCP}}{7} + 0.15$	ns
t_{TOP2}	Output Data Position6 (t_{TCP}=6.25ns~20ns)	$6\frac{t_{TCP}}{7} - 0.15$	$6\frac{t_{TCP}}{7}$	$6\frac{t_{TCP}}{7} + 0.15$	ns
t_{TPLL}	Phase Lock Loop Set			10.0	ms

AC Timing Diagrams

TTL Input

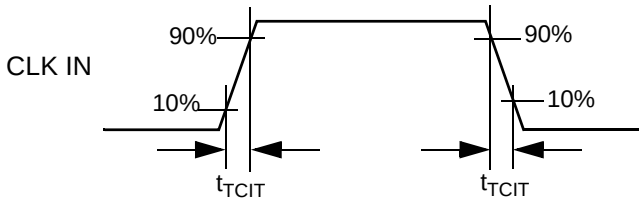
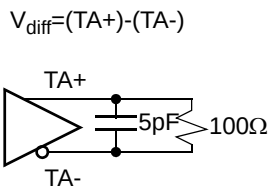


Fig2. CLKIN Transition Time

LVDS Output



LVDS Output Load

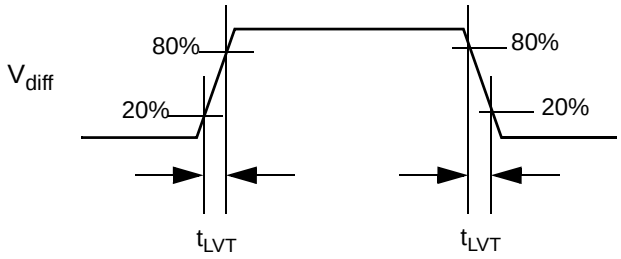
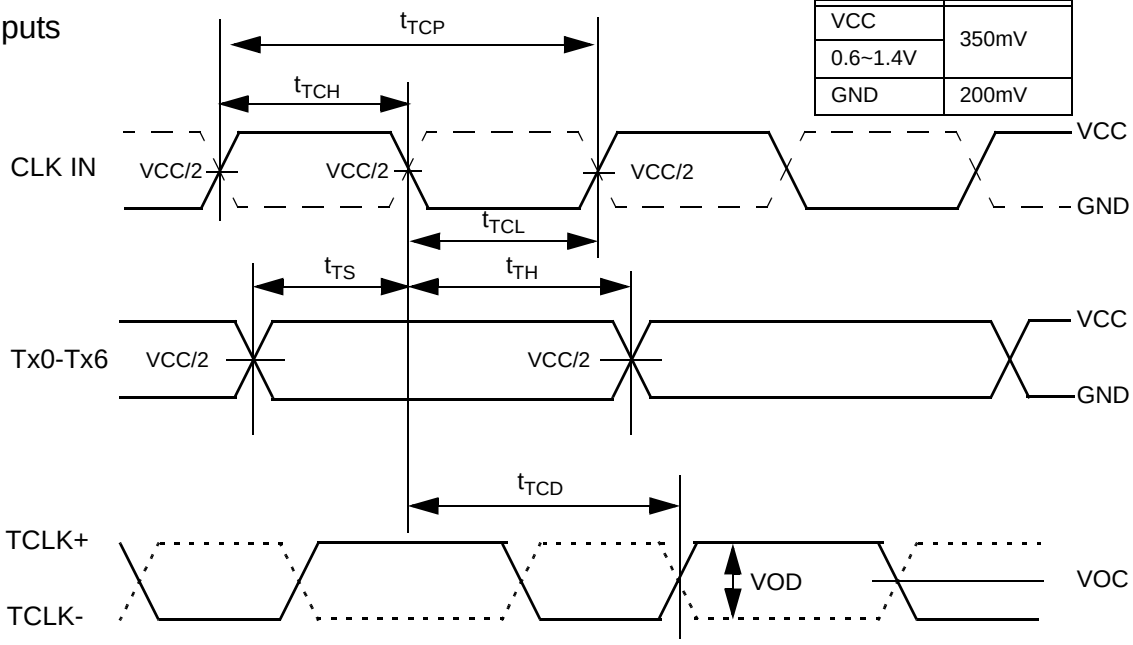


Fig3. LVDS Output Load and Transition Time

AC Timing Diagrams

TTL Inputs

RS pin	VOD
VCC	350mV
0.6~1.4V	
GND	200mV



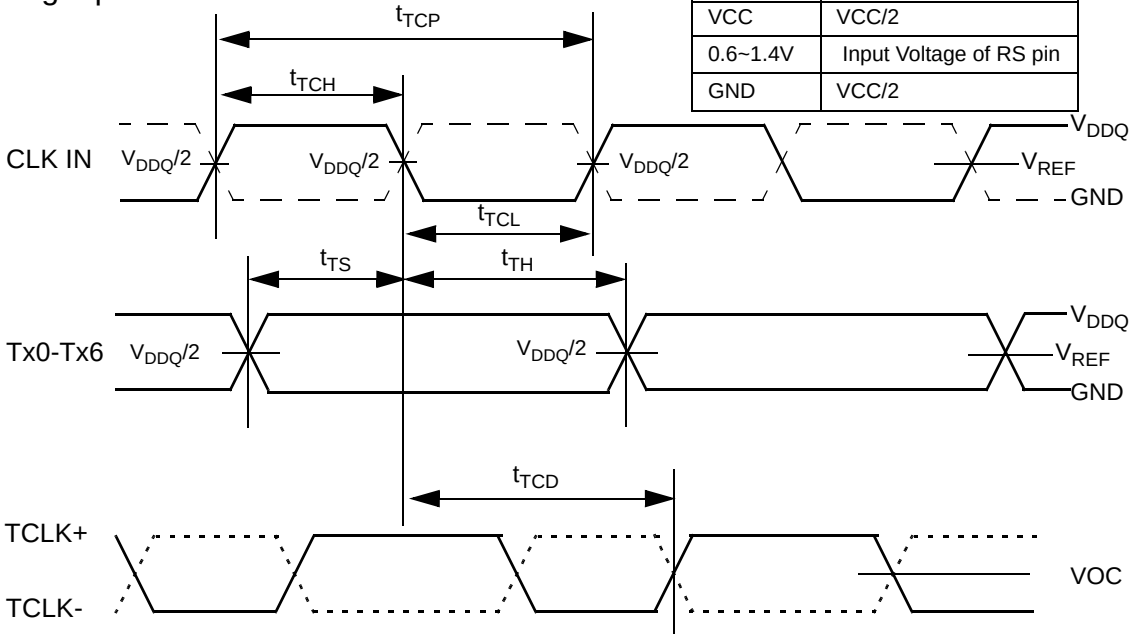
Note:

CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

Small Swing Inputs

RS pin	VREF
VCC	VCC/2
0.6~1.4V	Input Voltage of RS pin
GND	VCC/2



Note:

CLK IN: for R/F=GND, denote as solid line,
for R/F=VCC, denote as dashed line.

Fig5. Small Swing Inputs

AC Timing Diagrams

LVDS Output

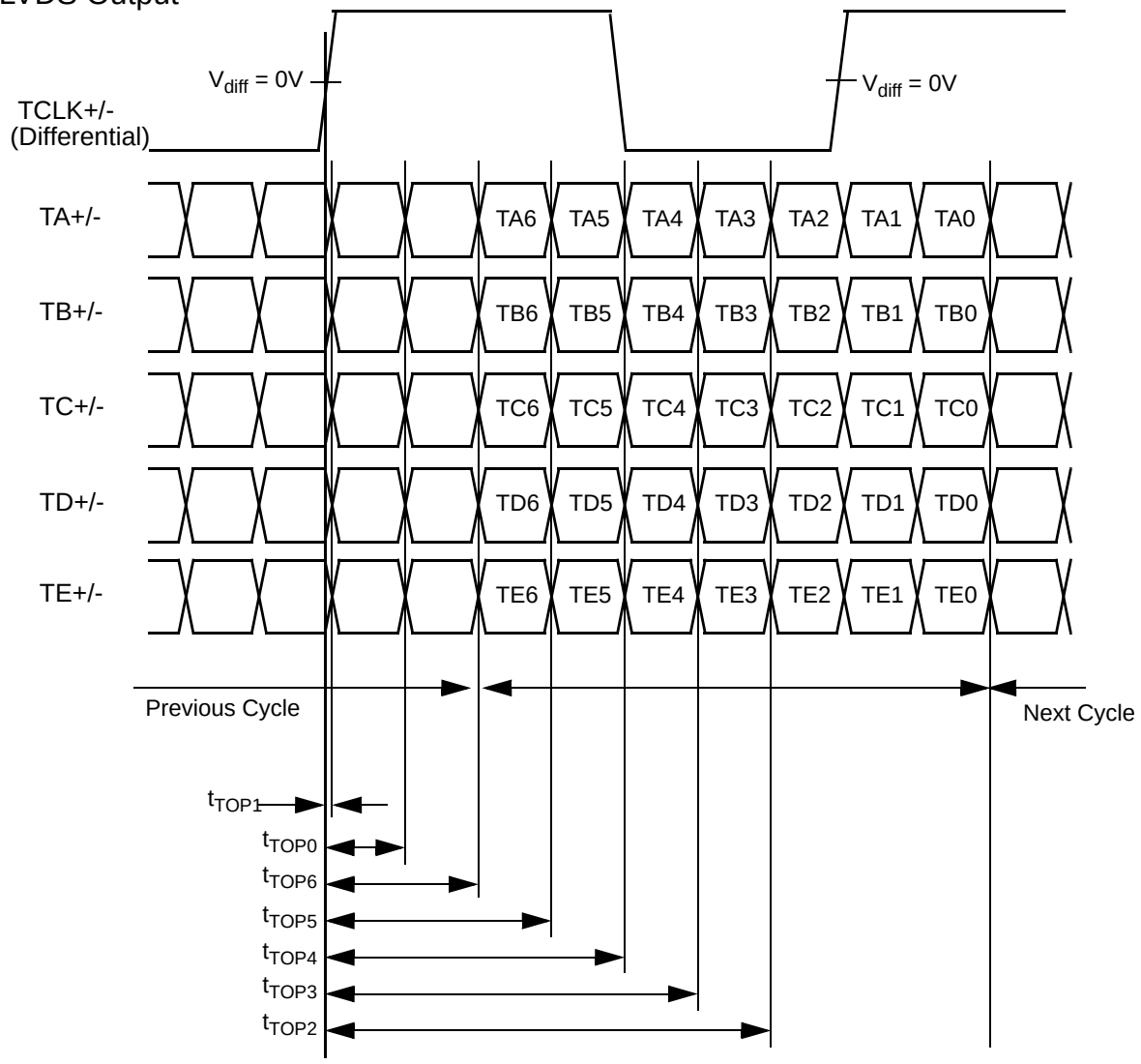


Fig6. LVDS Output Data Position

Phase Lock Loop Set Time

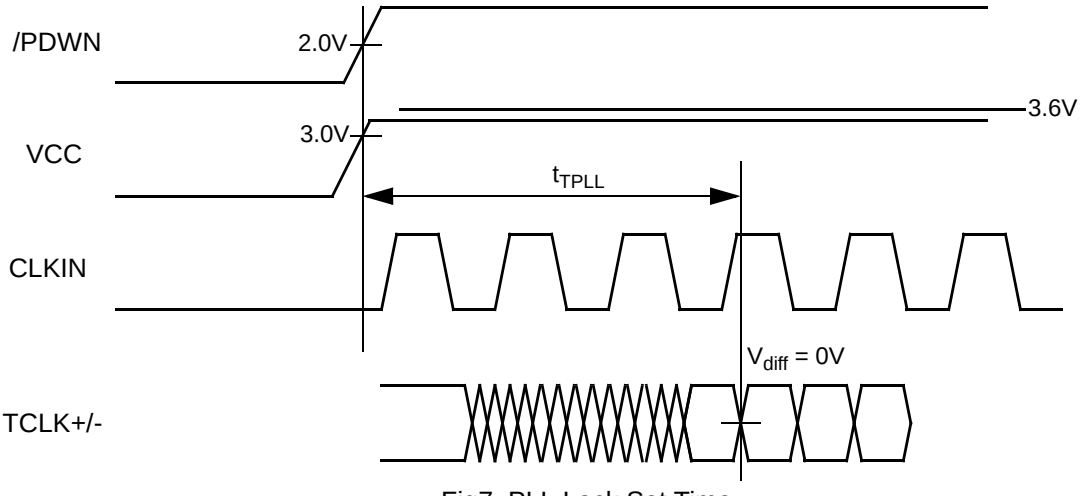


Fig7. PLL Lock Set Time

Note

1)Cable Connection and Disconnection

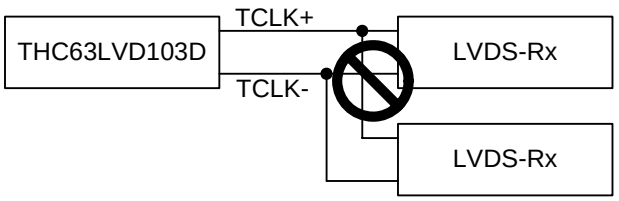
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVD103D and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

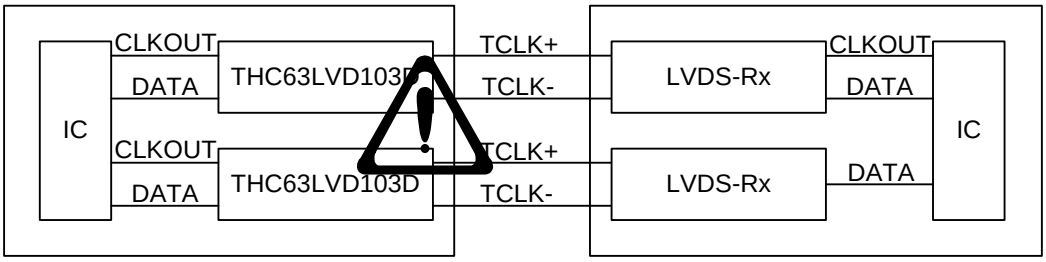
3)Multi Drop Connection

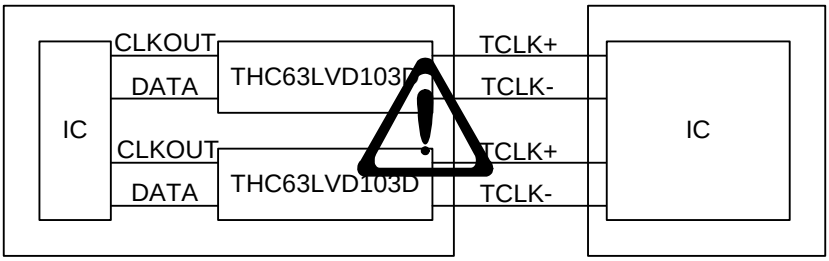
Multi drop connection is not recommended.



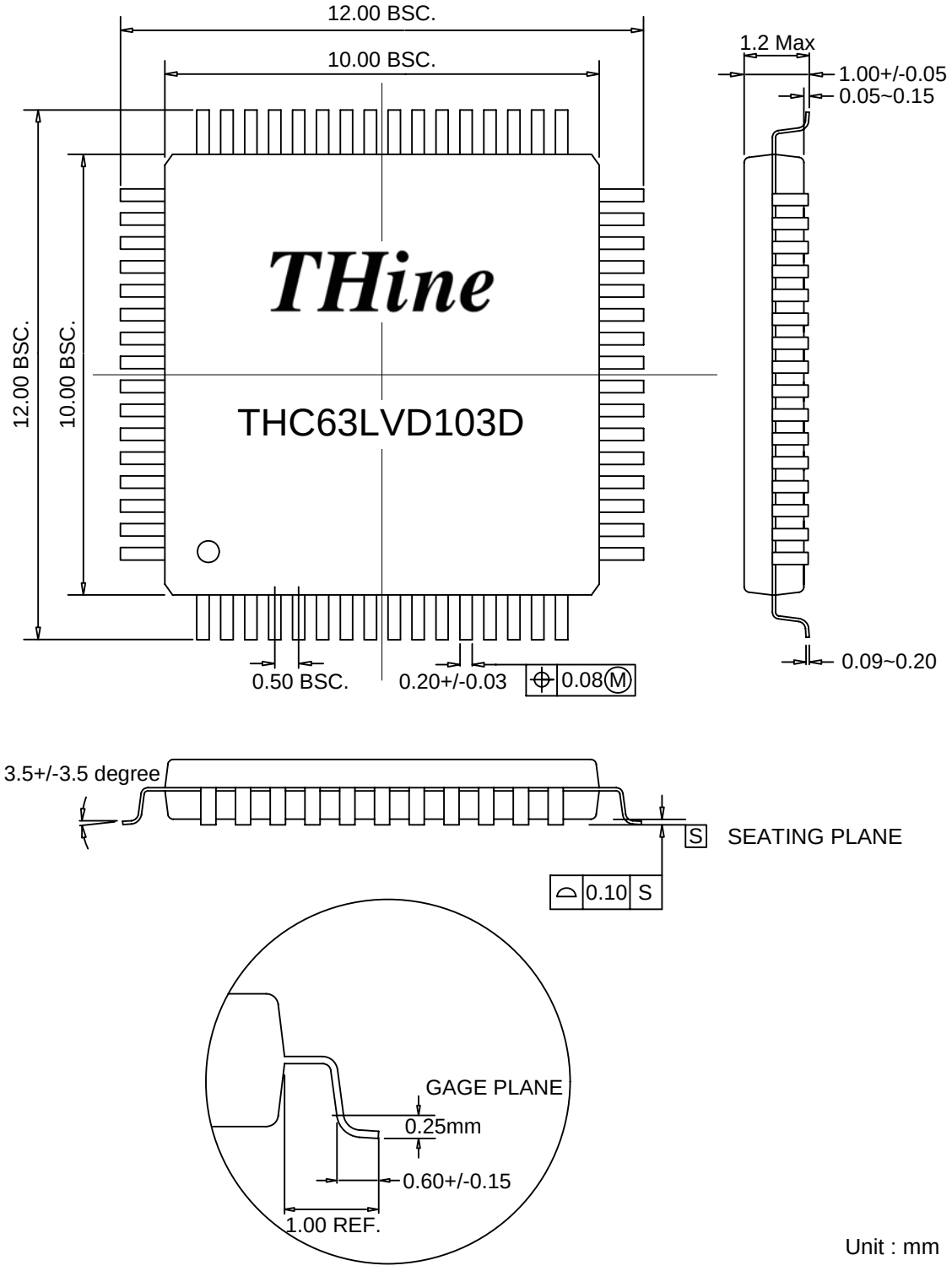
4)Asynchronous use

Asynchronous use such as following systems are not recommended.





Package



Unit : mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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6. Despite our utmost efforts to improve the quality and reliability of the product, faults will occur with a certain small probability, which is inevitable to a semi-conductor product. Therefore, you are encouraged to have sufficiently redundant or error preventive design applied to the use of the product so as not to have our product cause any social or public damage.
7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.

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