

# THC63LVDM83D

## REDUCED SWING LVDS 24Bit COLOR HOST-LCD PANEL INTERFACE

### General Description

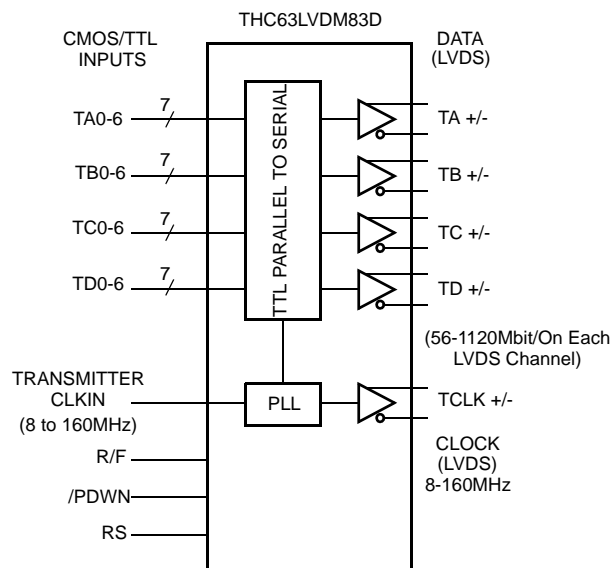
The THC63LVDM83D transmitter is designed to support pixel data transmission between Host and Flat Panel Display from NTSC up to 1080p(60Hz).

The THC63LVDM83D converts 28bits of CMOS/TTL data into LVDS(Low Voltage Differential Signaling) data stream. The transmitter can be programmed for rising edge or falling edge clocks through a dedicated pin. At a transmit clock frequency of 160MHz, 24bits of RGB data and 4bits of timing and control data (HSYNC, VSYNC, CNTL1, CNTL2) are transmitted at an effective rate of 1120Mbps per LVDS channel.

### Features

- Wide dot clock range: 8-160MHz suited for NTSC, VGA, SVGA, XGA, SXGA and SXGA+
- PLL requires no external components
- Supports spread spectrum clock generator
- On chip jitter filtering
- Clock edge selectable
- Supports reduced swing LVDS for low EMI
- Power down mode
- Low power single 3.3V CMOS design
- Low profile 56 Lead TSSOP Package
- 1.2 up to 3.3V tolerant data inputs to connect directly to low power, low voltage application and graphic processor.
- Pin compatible with THC63LVDM83C/83R(24bits)

### Block Diagram



## Pin Out

THC63LVDM83D

RS	1	56	TA4
TD1	2	55	TA3
TA5	3	54	TA2
TA6	4	53	GND
GND	5	52	TA1
TB0	6	51	TA0
TB1	7	50	TD0
TD2	8	49	LVDS GND
VCC	9	48	TA-
TD3	10	47	TA+
TB2	11	46	TB-
TB3	12	45	TB+
GND	13	44	LVDS VCC
TB4	14	43	LVDS GND
TB5	15	42	TC-
TD4	16	41	TC+
R/F	17	40	TCLK-
TD5	18	39	TCLK+
TB6	19	38	TD-
TC0	20	37	TD+
GND	21	36	LVDS GND
TC1	22	35	PLL GND
TC2	23	34	PLL VCC
TC3	24	33	PLL GND
TD6	25	32	/PDWN
VCC	26	31	CLK IN
TC4	27	30	TC6
TC5	28	29	GND

## Pin Description

Pin Name	Pin #	Type	Description												
TA+, TA-	47, 48	LVDS OUT	LVDS Data Out.												
TB+, TB-	45, 46	LVDS OUT													
TC+, TC-	41, 42	LVDS OUT													
TD+, TD-	37, 38	LVDS OUT													
TCLK+, TCLK-	39, 40	LVDS OUT	LVDS Clock Out.												
TA0 ~ TA6	51, 52, 54, 55, 56, 3, 4	IN	Pixel Data Inputs.												
TB0 ~ TB6	6, 7, 11, 12, 14, 15, 19	IN													
TC0 ~ TC6	20, 22, 23, 24, 27, 28, 30	IN													
TD0 ~ TD6	50, 2, 8, 10, 16, 18, 25	IN													
/PDWN	32	IN	H: Normal operation, L: Power down (all outputs are Hi-Z)												
RS	1	IN	LVDS swing mode, VREF select. See Fig4, 5. <table border="1" data-bbox="948 913 1374 1093" style="margin-left: auto; margin-right: auto;"> <thead> <tr> <th>RS</th> <th>LVDS Swing</th> <th>Small Swing Input Support</th> </tr> </thead> <tbody> <tr> <td>VCC</td> <td>350mV</td> <td>N/A</td> </tr> <tr> <td>0.6 ~ 1.4V</td> <td>350mV</td> <td>RS=VREF<sup>a</sup></td> </tr> <tr> <td>GND</td> <td>200mV</td> <td>N/A</td> </tr> </tbody> </table> <p>a. VREF is Input Reference Voltage.</p>	RS	LVDS Swing	Small Swing Input Support	VCC	350mV	N/A	0.6 ~ 1.4V	350mV	RS=VREF <sup>a</sup>	GND	200mV	N/A
RS	LVDS Swing	Small Swing Input Support													
VCC	350mV	N/A													
0.6 ~ 1.4V	350mV	RS=VREF <sup>a</sup>													
GND	200mV	N/A													
R/F	17	IN	Input Clock Triggering Edge Select. H: Rising edge, L: Falling edge												
VCC	9, 26	Power	Power Supply Pins for TTL inputs and digital circuitry.												
CLKIN	31	IN	Clock in.												
GND	5, 13, 21, 29, 53	Ground	Ground Pins for TTL inputs and digital circuitry.												
LVDS VCC	44	Power	Power Supply Pins for LVDS Outputs.												
LVDS GND	36, 43, 49	Ground	Ground Pins for LVDS Outputs.												
PLL VCC	34	Power	Power Supply Pin for PLL circuitry.												
PLL GND	33, 35	Ground	Ground Pins for PLL circuitry.												

## Absolute Maximum Ratings<sup>1</sup>

Supply Voltage ( $V_{CC}$ )	-0.3V ~ +4.0V
CMOS/TTL Input Voltage	-0.3V ~ ( $V_{CC} + 0.3V$ )
CMOS/TTL Output Voltage	-0.3V ~ ( $V_{CC} + 0.3V$ )
LVDS Transmitter Output Voltage	-0.3V ~ ( $V_{CC} + 0.3V$ )
Output Current	continuous
Junction Temperature	+125°C
Storage Temperature Range	-55°C ~ +150°C
Reflow Peak Temperature / Time	+260°C / 10sec.
Maximum Power Dissipation @+25°C	1.8W

1. “Absolute Maximum Ratings” are those valued beyond which the safety of the device can not be guaranteed. They are not meant to imply that the device should be operated at these limits. The tables of “Electrical Characteristics” specify conditions for device operation.

## Electrical Characteristics CMOS/TTL DC Specifications

 $V_{CC} = 3.0V \sim 3.6V$ ,  $T_a = 0^{\circ}C \sim +70^{\circ}C$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
$V_{IH}$	High Level Input Voltage	$RS=V_{CC}$ or GND	2.0		$V_{CC}$	V
$V_{IL}$	Low Level Input Voltage	$RS=V_{CC}$ or GND	GND		0.8	V
$V_{DDQ}^1$	Small Swing Voltage		1.2		2.8	V
$V_{REF}$	Input Reference Voltage	Small Swing ( $RS=V_{DDQ}/2$ )		$V_{DDQ}/2$		
$V_{SH}^2$	Small Swing High Level Input Voltage	$V_{REF} = V_{DDQ}/2$	$V_{DDQ}/2$ +100mV			V
$V_{SL}^2$	Small Swing Low Level Input Voltage	$V_{REF} = V_{DDQ}/2$			$V_{DDQ}/2$ -100mV	V
$I_{INC}$	Input Current	$0V \leq V_{IN} \leq V_{CC}$			$\pm 10$	$\mu A$

Notes: <sup>1</sup> $V_{DDQ}$  voltage defines max voltage of small swing input. It is not an actual input voltage.<sup>2</sup> Small swing signal is applied to TA0-6, TB0-6, TC0-6, TD0-6 and CLKIN.

## LVDS Transmitter DC Specifications

 $V_{CC} = 3.0V \sim 3.6V$ ,  $T_a = 0^{\circ}C \sim +70^{\circ}C$ 

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Units
VOD	Differential Output Voltage	Normal swing $RS=V_{CC}$	250	350	450	mV
		Reduced swing $RS=GND$	100	200	300	mV
$\Delta VOD$	Change in VOD between complementary output states	$RL=100\Omega$			35	mV
VOC	Common Mode Voltage		1.125	1.25	1.375	V
$\Delta VOC$	Change in VOC between complementary output states				35	mV
$I_{OS}$	Output Short Circuit Current	$V_{OUT}=0V$ , $RL=100\Omega$			-24	mA
$I_{OZ}$	Output TRI-STATE Current	$/PDWN=0V$ , $V_{OUT}=0V$ to $V_{CC}$			$\pm 10$	$\mu A$

## Supply Current

$V_{CC} = 3.0V \sim 3.6V, T_a = 0^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Condition(*)	Typ.	Max.	Units	
$I_{TCCW}$	Transmitter Supply Current	RL=100Ω, CL=5pF V <sub>CC</sub> =3.3V, RS=V <sub>CC</sub> Worst Case Pattern	f=85MHz	61	67	mA
			f=135MHz	77	83	mA
			f=160MHz	84	92	mA
		RL=100Ω, CL=5pF V <sub>CC</sub> =3.3V, RS=GND Worst Case Pattern	f=85MHz	50	56	mA
			f=135MHz	65	71	mA
			f=160MHz	73	80	mA
$I_{TCCS}$	Transmitter Power Down Supply Current	/PDWN = L, All Inputs = L or H		10	μA	

### Worst Case Pattern

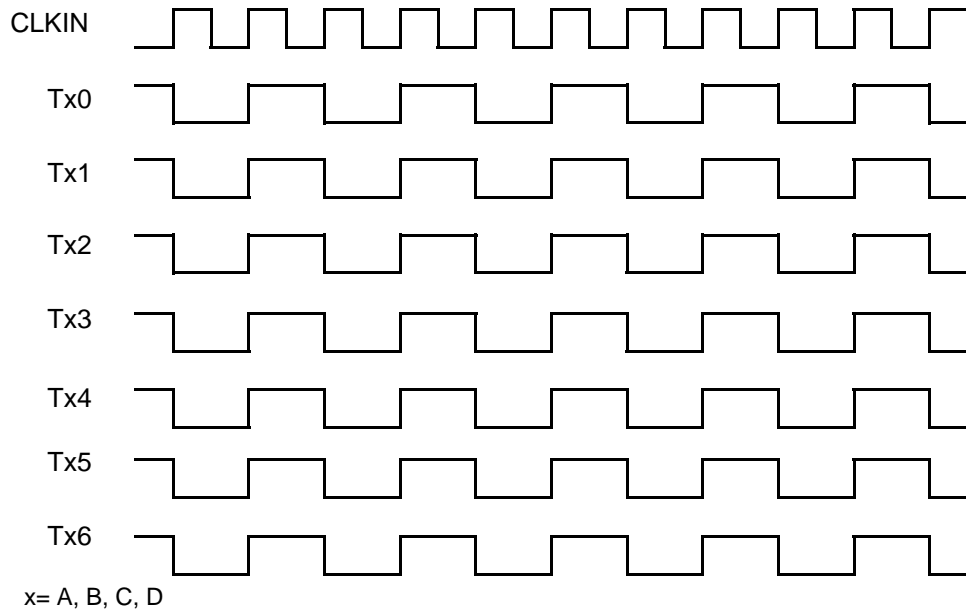


Fig1. Worst Case Pattern

## Switching Characteristics

$V_{CC} = 3.0V \sim 3.6V, T_a = 0^{\circ}C \sim +70^{\circ}C$

Symbol	Parameter	Min.	Typ.	Max.	Units
$t_{TCIT}$	CLK IN Transition time			5.0	ns
$t_{TCP}$	CLK IN Period	6.25	T	125	ns
$t_{TCH}$	CLK IN High Time	0.35T	0.5T	0.65T	ns
$t_{TCL}$	CLK IN Low Time	0.35T	0.5T	0.65T	ns
$t_{TCD}$	CLK IN to TCLK+/- Delay		3T		ns
$t_{TS}$	TTL Data Setup to CLK IN	2.0			ns
$t_{TH}$	TTL Data Hold from CLK IN	0.0			ns
$t_{LVT}$	LVDS Transition Time		0.6	1.5	ns
$t_{TOP1}$	Output Data Position0 (T=6.25ns~20ns)	-0.15	0.0	+0.15	ns
$t_{TOP0}$	Output Data Position1 (T=6.25ns~20ns)	$\frac{T}{7} - 0.15$	$\frac{T}{7}$	$\frac{T}{7} + 0.15$	ns
$t_{TOP6}$	Output Data Position2 (T=6.25ns~20ns)	$2\frac{T}{7} - 0.15$	$2\frac{T}{7}$	$2\frac{T}{7} + 0.15$	ns
$t_{TOP5}$	Output Data Position3(T=6.25ns~20ns)	$3\frac{T}{7} - 0.15$	$3\frac{T}{7}$	$3\frac{T}{7} + 0.15$	ns
$t_{TOP4}$	Output Data Position4 (T=6.25ns~20ns)	$4\frac{T}{7} - 0.15$	$4\frac{T}{7}$	$4\frac{T}{7} + 0.15$	ns
$t_{TOP3}$	Output Data Position5 (T=6.25ns~20ns)	$5\frac{T}{7} - 0.15$	$5\frac{T}{7}$	$5\frac{T}{7} + 0.15$	ns
$t_{TOP2}$	Output Data Position6 (T=6.25ns~20ns)	$6\frac{T}{7} - 0.15$	$6\frac{T}{7}$	$6\frac{T}{7} + 0.15$	ns
$t_{TPLL}$	Phase Lock Loop Set			10.0	ms

### AC Timing Diagrams

#### TTL Input

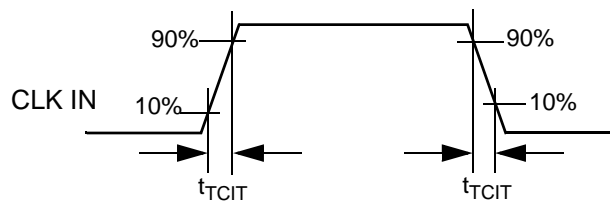
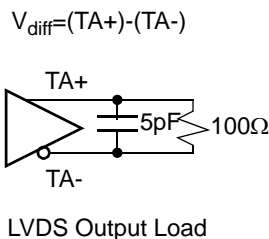


Fig2. CLKIN Transition Time

#### LVDS Output



LVDS Output Load

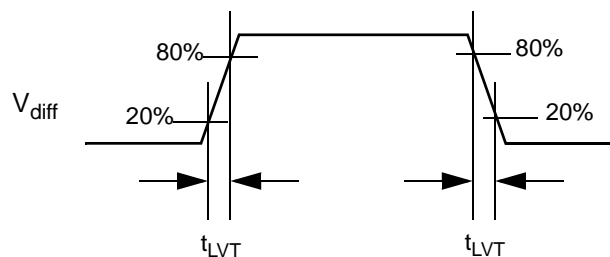
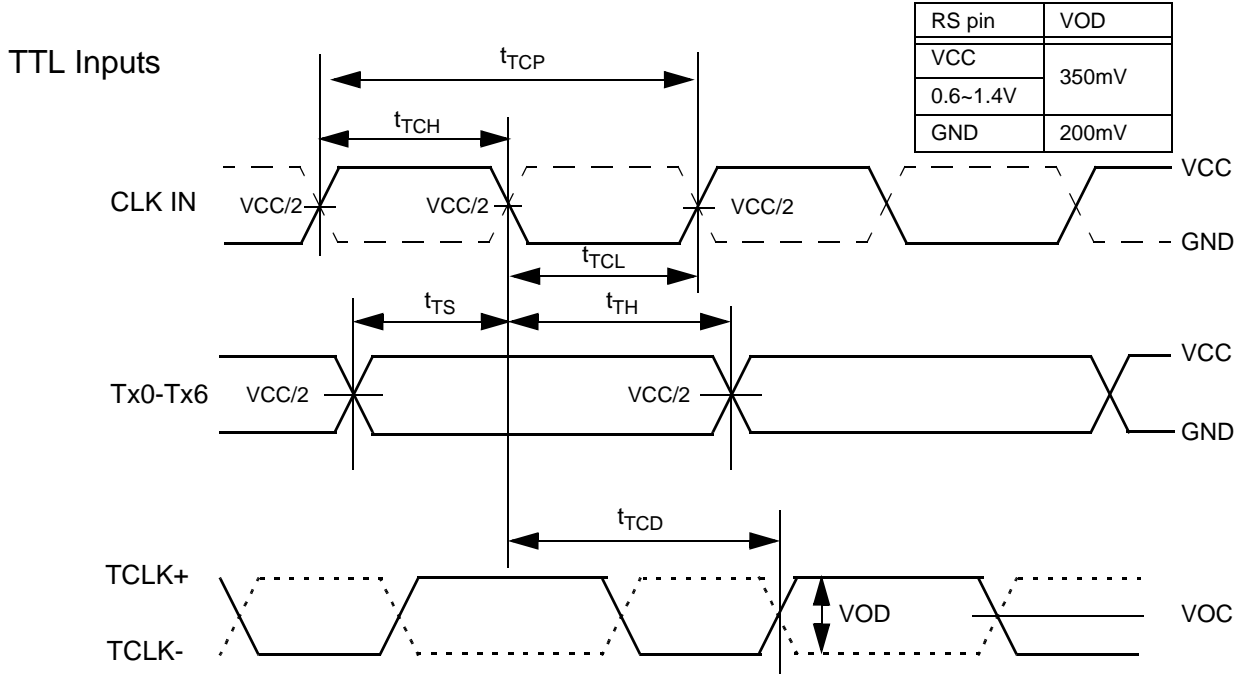


Fig3. LVDS Output Load and Transition Time

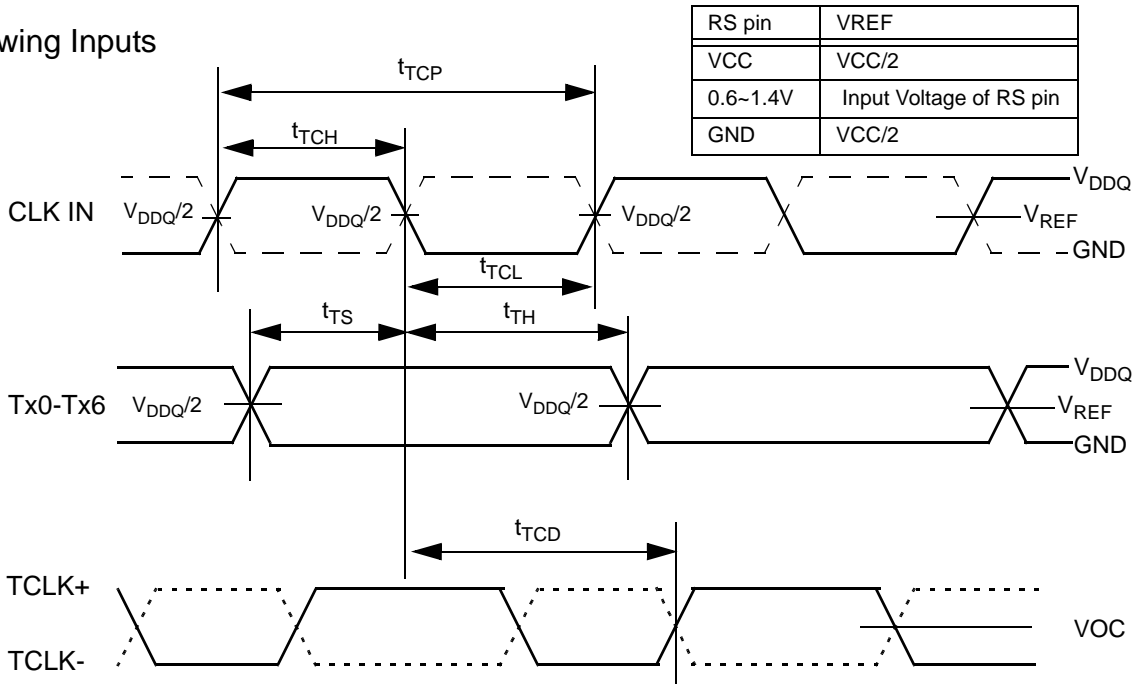
### AC Timing Diagrams



Note:  
 CLK IN: for R/F=GND, denote as solid line,  
 for R/F=VCC, denote as dashed line.

Fig4. CLKIN Period, High/Low Time, Setup/Hold Timing

### Small Swing Inputs



Note:  
 CLK IN: for R/F=GND, denote as solid line,  
 for R/F=VCC, denote as dashed line.

Fig5. Small Swing Inputs



### AC Timing Diagrams

#### LVDS Output

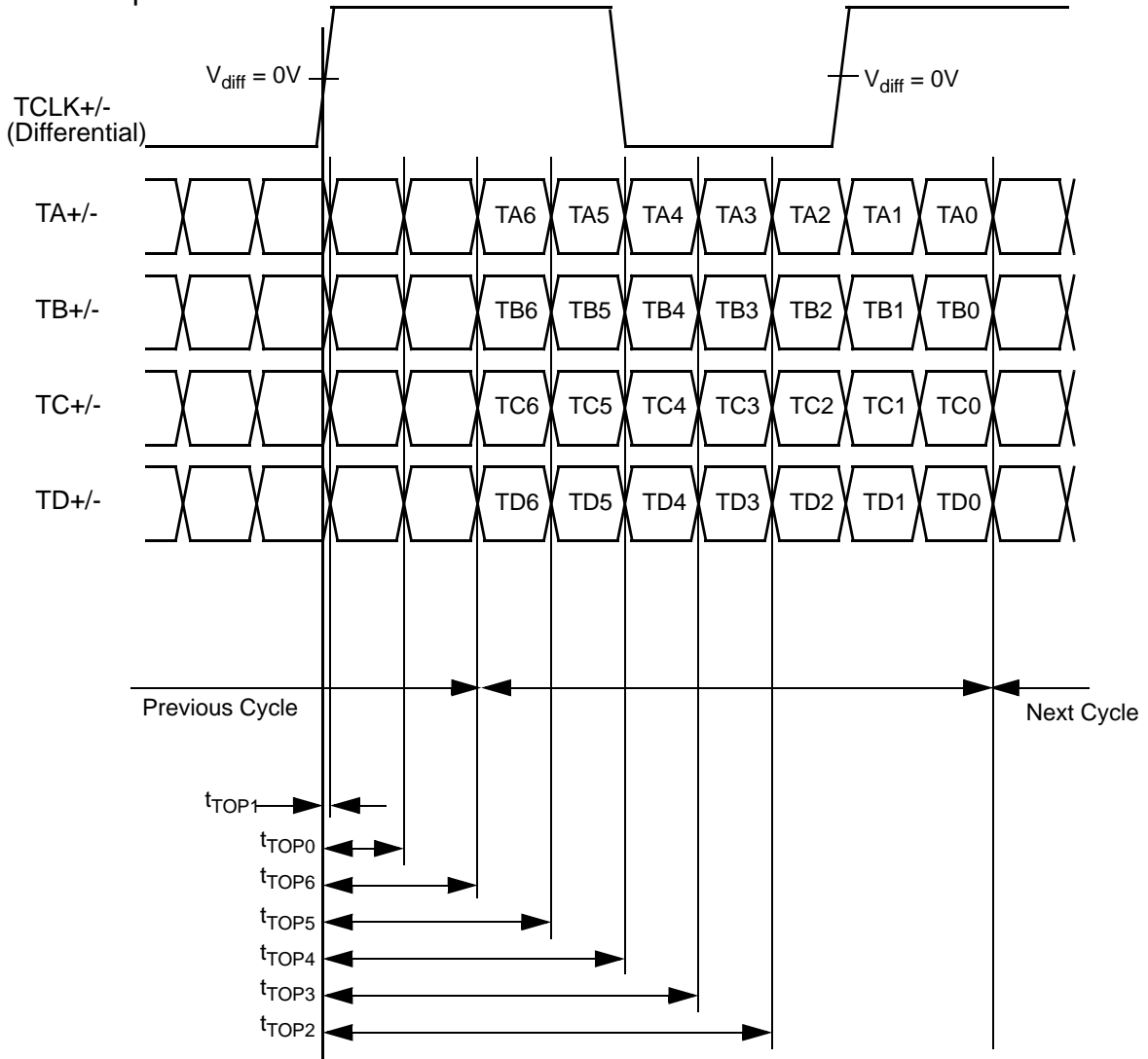


Fig6. LVDS Output Data Position

#### Phase Lock Loop Set Time

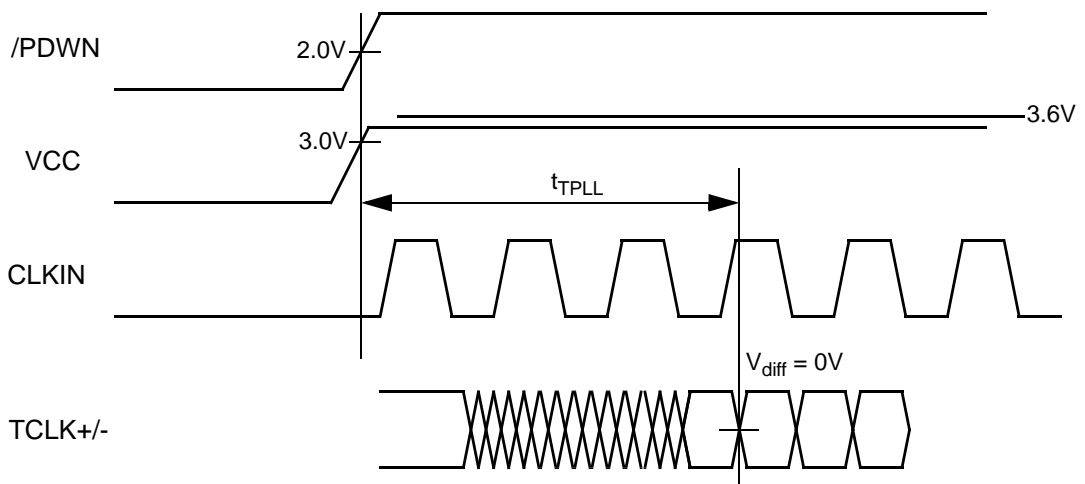


Fig7. PLL Lock Set Time

Note

1)Cable Connection and Disconnection

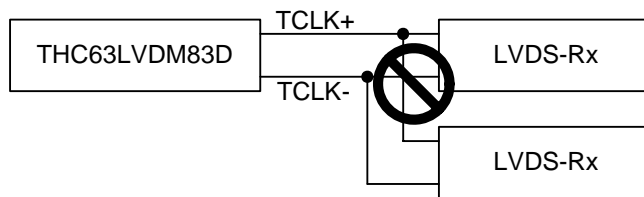
Don't connect and disconnect the LVDS cable, when the power is supplied to the system.

2)GND Connection

Connect the each GND of the PCB which THC63LVDM83D and LVDS-Rx on it. It is better for EMI reduction to place GND cable as close to LVDS cable as possible.

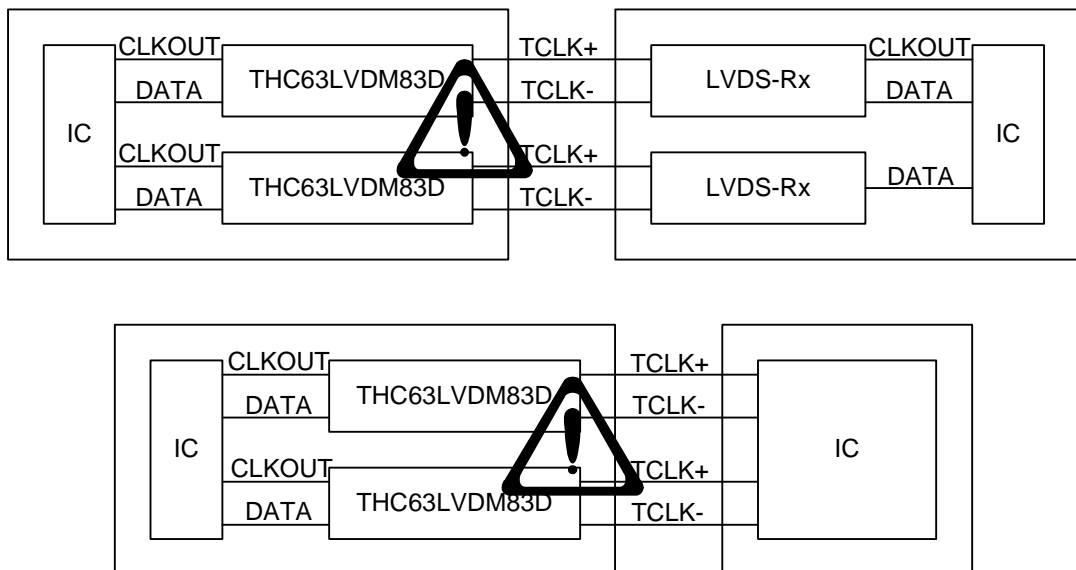
3)Multi Drop Connection

Multi drop connection is not recommended.

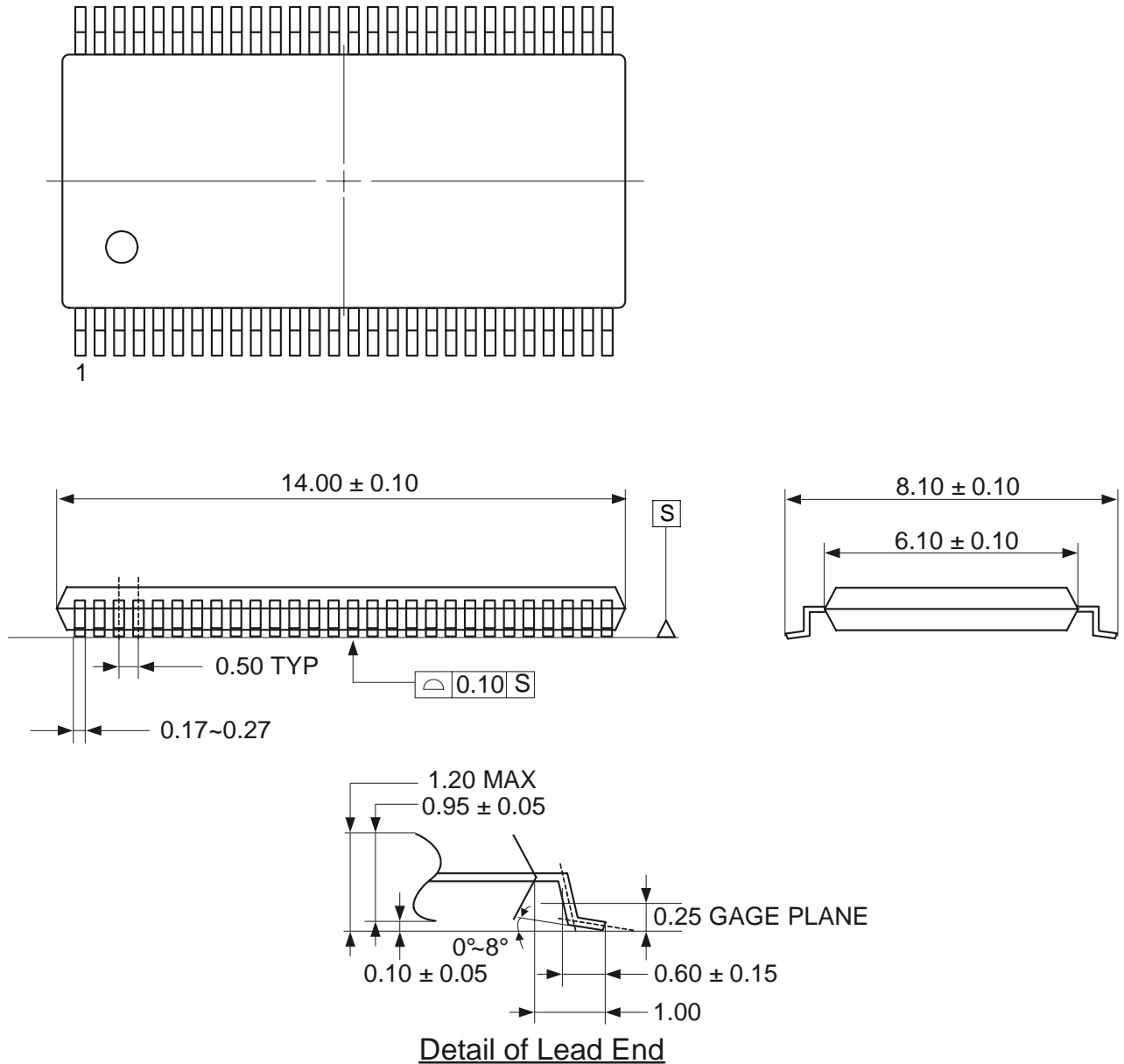


4)Asynchronous use

Asynchronous use such as following systems are not recommended.



Package



Unit:mm

## Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
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