THV3058

3CH (Buck/Boost) 2CH CP 1CH HVLDO Controller

Description

THV3058 is a controller IC for multi-channel power supply system with 3 channel PWM DC/DC converters(CH-1 Boost/CH-2, CH-3 Buck) and 2 channel charge pump circuits.

THV3058 contains internal soft start, under voltage protection, over voltage protection and over current protection, which helps reducing the number of external component count and increasing reliability.

Built-in positive and negative charge pump circuits(VGL/VGH) achieve enhanced performance.

Ceramic capacitors are available for output, that provides space-saving and low cost system.

THV3058 is ideal for TFT-LCD bias power supply system.

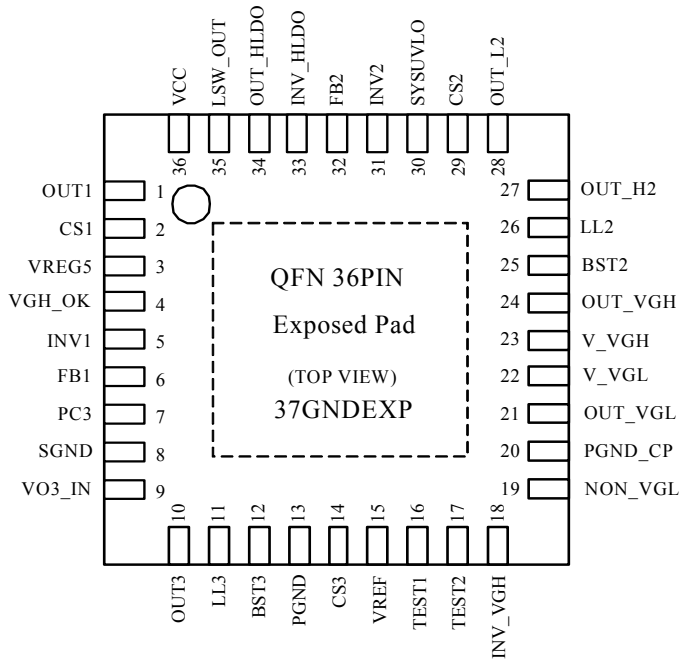
Features

- QFN 36 pin package
- Input Voltage range : 9 ~ 15V
- Push Pull output for direct Power MOS driving
- Optimized for ceramic output capacitor
- Complete PWM mode controller
- Positive/Negative charge pumps
  (PFM mode controller)
- Switching Frequency : 500kHz
- Under Voltage Protection (Timer Latch)
- DC/DC Over Voltage Protection
  (CH-2, CH-3 : Timer Latch)
- DC/DC Over Current Protection
- UVLO function
- CH-1 Boost Converter
- CH-2 Buck Converter (Reference Voltage:0.85V)
- CH-3 Buck Converter (Output Voltage : 3.3V)
- High Voltage LDO

Application

・TFT-LCD Bias power supply

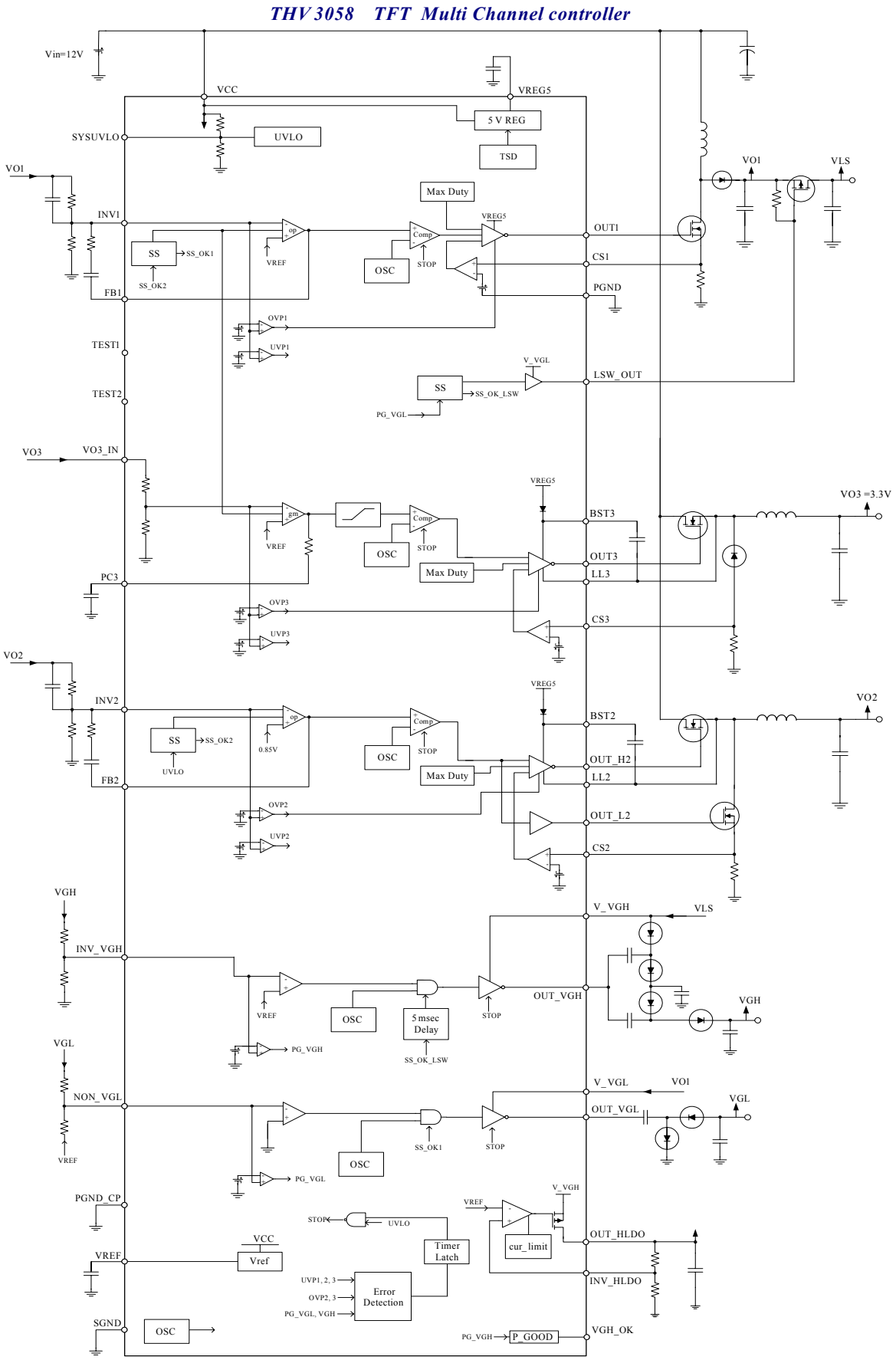
Pin Assignment



Output Channel Description

Output Channel	Description
CH-1	PWM Boost converter
CH-2	PWM Buck converter (NMOS transistor drive for synchronous rectifier / available for diode rectification)
CH-3	PWM Buck converter fixed 3.3V
VGH	Positive charge pump
VGL	Negative charge pump
HVLDO	High voltage LDO
LSW_OUT	Output for the external load switch.
VGH_OK	Output for VGH Power Good Signal.

Block Diagram



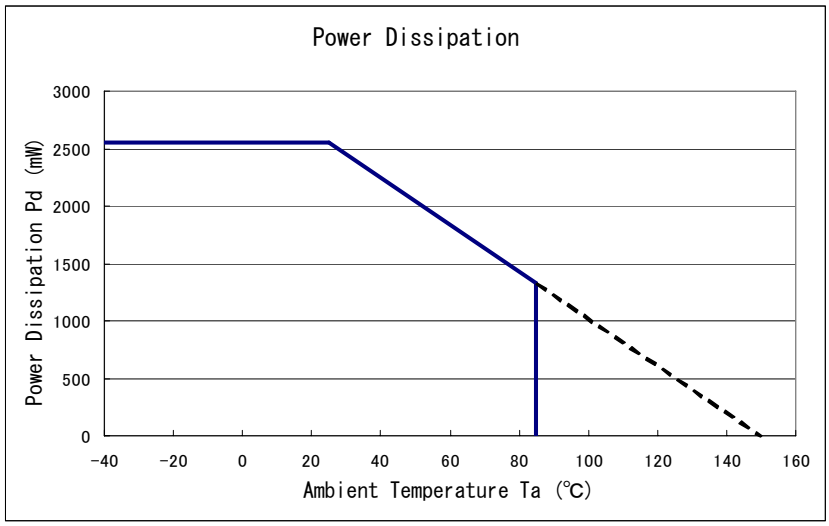
Pin Description

Pin#	Symbol	Function	Description
1	OUT1	CH-1 output	Boost driver pin for CH-1 external device. Output range is 0~5V.
2 29 14	CS1 CS2 CS3	CH-1, CH-2, CH-3 over current sense	Connect CS1 to sence registance connected Low side NMOS source. Connect CS2 to sence registance connected Low side NMOS source or diode anode. Connect CS3 to sence registance connected diode anode.
3	VREG5	5V regulator output	5V regulator output pin. Power supply for low voltage output. Connect an external capacitor(Typ:4.7μF) between this pin.
4	VGH_OK	VGH power good signal	Open drain output. Connect an approximately 100k ohm pull-up resistor. When VGH has generated normally, the output is fixed to High level.
5 31	INV1 INV2	CH-1,CH-2 error amplifier inverting input	CH-1, CH-2 error amp inverting inputs. The voltage on INV1 is 1.2V, and INV2 is 0.85V, in the normal operation.
6 32	FB1 FB2	CH-1,CH-2 error amplifier output	CH-1, CH-2 error amplifier outputs for phase compensation by connecting resistors and capacitors between FB1,2 and INV1,2.
7	PC3	CH-3 phase compensation	Connect a capacitor between this pin for phase compensation.
8	SGND	Signal Ground	Ground for control circuit.
9	VO_3IN	CH-3 output voltage feedback	CH-3 output voltage feedback pin.
26 11	LL2 LL3	CH-2, CH-3 node connection to inductor	CH-2, CH-3 node connection to inductor.
10	OUT3	CH-3 output	Driver pin for CH-3 High side transistor.
25 12	BST2 BST3	CH-2, CH-3 High side capacitor connection	CH-2, CH-3 power supply for High side driver output. Bootstrap diodes are built-in.
13 20	PGND PGND_CP	Power Ground	Ground for power supply
15	VREF	Reference voltage	Reference voltage(1.2V). Connect an external capacitor(0.01μF) between this pin for stability. Maximum load current is 1mA.
16 17	TEST1 TEST2	Test pin	Connect to Ground or open in normal use..
18	INV_VGH	VGH comparator inverting input	VGH comparator inverting input
19	NON_VGL	VGL comparator non-inverting input	VGL comparator non-inverting input
21	OUT_VGL	VGL (charge pump -)output	VGL drive output for negative voltage charge pump. V_VGL is used as input power supply. In PFM mode, this pin can be used as PMOS gate drive.
22	V_VGL	VGL output voltage supply	VGL output voltage supply.
23	V_VGH	VGH output voltage supply	VGH output voltage supply.
24	OUT_VGH	VGH (charge pump +)output	VGH drive output for positive voltage charge pump. V_VGH is used as power supply. In PFM mode, this pin can be used as NMOS gate drive.

Pin#	Symbol	Function	Description
27	OUT_H2	CH-2 High side drive output	CH-2 High side NMOS transistor drive for synchronous rectifier.
28	OUT_L2	CH-2 Low side driver output	CH-2 Low side NMOS transistor drive for synchronous rectifier. Available even without Low side NMOS transistor.
30	SYSUVLO	System UVLO input	SYSUVLO pin shuts down the IC, when the power supply voltage (Vin) is lower than the predetermined voltage. The threshold voltage is 3.5V, the release voltage is 5.46V. by internal setting. The threshold voltage also can be set optionally by changing the external resistance value.
33	INV_HLDO	HVLDO amplifier inverting input	HVLDO inverting input. The voltage on this pin is 1.2V in the normal operation.
34	OUT_HLDO	HVLDO output	HVLDO output. Connect to an external capacitor(Typ:2.2μF).
35	LSW_OUT	Output for CH-1 switch control	Gate control pin for CH-1 external switch. Soft start function is built-in.
36	VCC	Power supply	Power supply for control.

Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Power Supply Voltage VCC	Vcc	18	V
CS1, CS2, CS3, INV1, INV2, FB1, FB2, VO3_IN, TEST1, TEST2, INV_VGH, NON_VGL, SYSUVLO, INV_HLDO,	VL_in	6.5	V
OUT1, VREG5, VGH_OK, PC3, VREF, OUT_L2, BST2-LL2, OUT_H2-LL2, BST3-LL3, OUT3-LL3	VL_out	6.5	V
OUT_VGL, OUT_VGH, OUT_HLDO, LSW_OUT	VH_out1	20	V
LL2, LL3	VH_out2	18	V
OUT_H2, BST2, OUT3, BST3	VH_out3	24.5	V
V_VGL, V_VGH	VH_cc	20	V
Power Dissipation	Pd	2556 (Ta<25°C)	mW
Junction Temperature	Tj	150	°C
Operating Ambient Temperature Range	Ta	-40 ~ +85	°C
Storage Temperature Range	Tstg	-55 ~ +150	°C



Recommended Operating Conditions

Parameter	Min	Typ	Max	Unit
VCC voltage (Input Power Supply Voltage)	9	–	15	V
V_VGH, V_VGL voltage	9	–	17	V
OUT_HLDO, LSW_OUT voltage	-0.1	–	17	V
VGH_OK, SYSUVLO voltage	-0.1	–	5.5	V
External capacitance for VREF pin	–	0.01	–	µF
External capacitance for VREG5 pin	2.2	4.7	–	µF
External capacitance for OUT_HLDO pin	1	2.2	–	µF

Electrical Characteristics (Unless otherwise specified, VCC=12V, Ta=25°C)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Reference Voltage Block						
Reference Voltage	Vref	Cvref = 0.01μF	1.188	1.200	1.212	V
Reference Voltage (ch-2)	Vref(ch-2)	Vref x 0.85/1.2	0.84	0.85	0.86	V
Line Regulation	Vref (line)	Iref = -100μA, VCC = 9 ~ 15V	-	2	5	mV
Load Regulation	Vref (load)	Iref = -100μA ~ -1mA	-	2	5	mV
5V Regulator Block						
Output Voltage	Vreg5 (range)	Io = -1mA	–	5.0	–	V
Load Regulation	Vreg5(load)	Io = -0.1mA ~ -5mA	–	–	100	mV
Line Regulation	Vreg5(line)	Io = -1mA, VCC = 9 ~ 15V	–	–	20	mV
Oscilator Circuit Block						
Oscillation Frequency	Fosc		430	500	570	kHz
DTC Circuit Block						
Maximum Duty Cycle(ch-1)	Dmax (ch-1)		–	86	–	%
Maximum Duty Cycle(ch-2, 3)	Dmax (ch-2, 3)		–	84	–	%
Duty Cycle(VGH)	D(VGH)		–	50	–	%
Duty Cycle(VGL)	D(VGL)		–	18	–	%
Error Amplifier Block						
Offset voltage	Vio1	Based on VREF pin voltage	-10	–	10	mV
	Vio2	Buffer connection Based on the value : VREF x 0.85/1.2				
gm (ch-3)	gm(ch-3)	PC3 = 2.5V	-340	-520	-760	μS
Charge Pump Block						
Threshold Voltage(VGH)	Vthc(VGH)	INV_VGH pin	–	1.2	–	V
Threshold Voltage(VGL)	Vthc(VGL)	NON_VGL pin	–	0	–	V
Offset Voltage(VGH, VGL)	Vioc (VGH,VGL)		-20	–	20	mV
VGH Power Good						
INV_VGH Threshold Voltage	Vpgvgh	INV_VGH pin	–	1.02	–	V
Output Resistance	Ropgvgh	VGH_OK = Low, Io = 1mA	–	0.9	1.6	kΩ
Off Leak Current	Ioffpgvgh	VGH_OK = 5V	–	–	1	μA

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
High Voltage LDO Block						
Reference Voltage	Vref(hvldo)	INV_HLDO pin	–	1.2	–	V
Offset voltage	Vhvldo(off)	Ildo = -1mA	-20	–	20	mV
Load regulation	Vhvldo (load)	VO_1IN = 16V, OUT_HLDO = 15V Ildo = -0.1m ~ -20mA	–	16.5	45	mV
High side output voltage range	Vhldo (hrange)	Ildo = -10mA	V_VGH -0.5	V_VGH -0.2	–	V
Low side output voltage range	Vhldo (lrange)	Ildo = -10mA	5.5	–	–	V
Dropout voltage	Vdrop (hldo)	Ildo = -10mA,VO_1IN = 16V, INV_HLDO = 0V	–	60	120	mV
Switch Control Block						
LSW_OUT Output Resistance	Ro(1sw_out)	Io = 1mA	–	1.2	–	kΩ
Output Block						
OUT1 H level Output Resistance	Roh(ch-1)	Ioh = -50mA	–	17	–	Ω
OUT1 L level Output Resistance	Rol(ch-1)	Iol = 50mA	–	11	–	Ω
OUT_H2 H level Output Resistance	Roh(ch-2h)	Ioh = -50mA	–	17	–	Ω
OUT_H2 L level Output Resistance	Rol(ch-2h)	Iol = 50mA	–	13	–	Ω
OUT_L2 H level Output Resistance	Roh(ch-2l)	Ioh = -50mA	–	22	–	Ω
OUT_L2 L level Output Resistance	Rol(ch-2l)	Iol = 50mA	–	6	–	Ω
OUT3 H level Output Resistance	Roh(ch-3)	Ioh = -50mA	–	17	–	Ω
OUT3 L level Output Resistance	Rol(ch-3)	Iol = 50mA	–	13	–	Ω
OUT_VGH H level Output Resistance	Roh(vgh)	V_VGH = 15V, Ioh = -50mA	–	3.5	–	Ω
OUT_VGH L level Output Resistance	Rol(vgh)	V_VGH = 15V, Iol = 50mA	–	3.5	–	Ω
OUT_VGL H level Output Resistance	Roh(vgl)	V_VGL = 15V, Ioh = -50mA	–	11	–	Ω
OUT_VGL L level Output Resistance	Rol(vgl)	V_VGL = 15V, Iol = 50mA	–	5	–	Ω
Output Voltage						
VO3 Output Voltage	Vo3	VO3_IN pin	3.23	3.30	3.37	V
Under Voltage Protection Block						
Threshold Voltage (ch-1)	Vuvp(ch-1)	INV1 pin	–	1.02	–	V
Threshold Voltage (ch-2)	Vuvp(ch-2)	INV2 pin	–	0.64	–	V
Threshold Voltage (ch-3)	Vuvp(ch-3)	VO3_IN pin	–	2.64	–	V
Threshold Voltage (VGH)	Vuvp(vgh)	INV_VGH pin	–	1.02	–	V
Threshold Voltage (VGL)	Vuvp(vgl)	NON_VGL pin	–	0.18	–	V

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Timer Latch Block						
Timer (UVP)	Timer(uvp)		–	12.2	–	ms
Timer (OVP)	Timer(ovp)		–	2.44	–	ms
Soft Start Block						
Soft Start Time(ch-1,3)	ss1,3		–	10	–	ms
Soft Start Time(ch-2)	ss2		–	7	–	ms
Soft Start Time(LSW)	ss_lsw		–	10	–	ms
VGH Delay Time	vgh_delay		–	5	–	ms
Over Voltage Protection Block						
Threshold Voltage (ch-1)	Vovp(ch-1)	INV1 pin	–	1.5	–	V
Threshold Voltage (ch-2)	Vovp(ch-2)	INV2 pin	–	1.06	–	V
Threshold Voltage (ch-3)	Vovp(ch-3)	VO3_IN pin	–	4.13	–	V
Over Current Protection						
Threshold Voltage(ch-1)	CS1(Vth)	CS1 pin	–	100	–	mV
Threshold Voltage(ch-2)	CS2(Vth)	CS2 pin	–	-100	–	mV
Threshold Voltage(ch-3)	CS3(Vth)	CS3 pin	–	-175	–	mV
System UVLO Block						
Release Voltage	Vuvlo	VCC pin	5.0	5.46	6.0	V
Hysteresis Voltage	Vuvlo(hys)	VCC pin	1.4	1.96	2.5	V
System UVLO External Setting						
Release Voltage	Vsysuvlo	SYSUVLO pin	1.44	1.56	1.68	V
Hysteresis Voltage	Vsysuvlo (hys)	SYSUVLO pin	0.41	0.56	0.71	V
Overall						
Average Current Consumption	Icc(op)	Output Swing On(VCC pin)	–	3.1	–	mA
	Icc	Output Swing Off	–	2.1	–	mA

Functional Description

● **System UVLO**

UVLO stops the device operation if the input power supply voltage drops below a preset voltage. The threshold voltage is 3.5V, the release voltage is 5.46V by internal setting. When input power supply voltage(Vin) rises above 5.46V, the device goes into soft start mode and output voltage(Vo) increases gradually up to the regular voltage. If the input power supply voltage(Vin) drops below 3.5V, UVLO stops switching operation immediately and accompanies output voltage drop (see Figure 1).

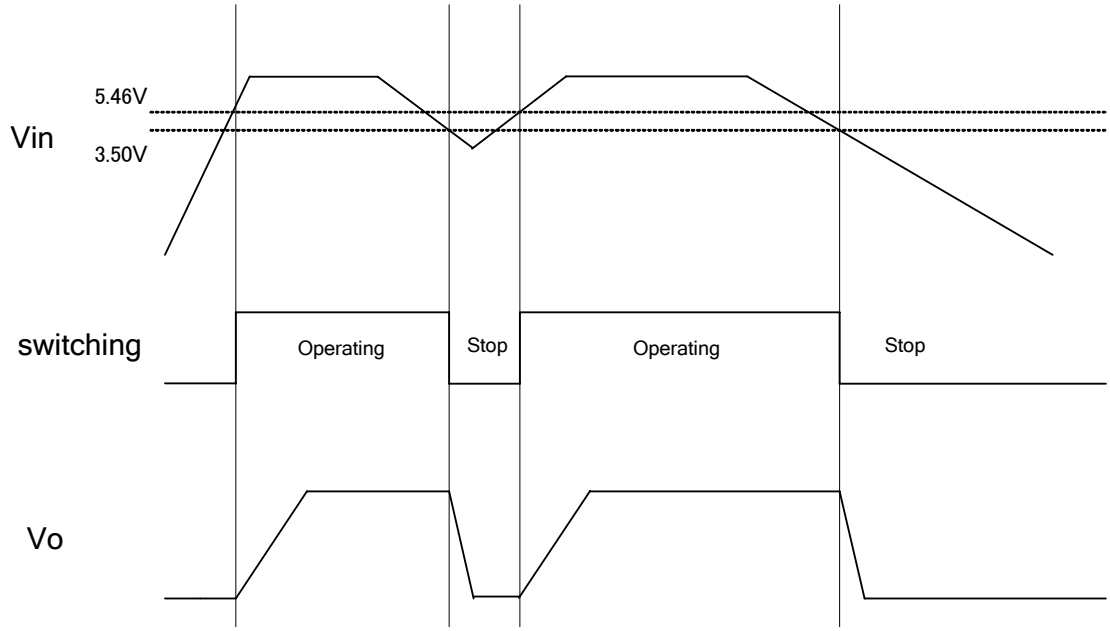


Figure 1.UVLO Operation

The UVLO threshold voltage also can be set optionally by changing the external resistance value (see Figure 2). The UVLO threshold voltage are given by the following formulas. Please use lower the external resistance value than the internal resistance value.

$$\text{Release Voltage of System UVLO} = 1.56 \times \frac{R1 + R2}{R2}$$

$$\text{Detection Voltage of System UVLO} = 1.0 \times \frac{R1 + R2}{R2}$$

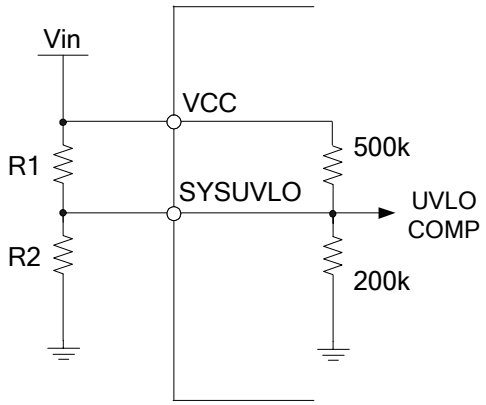


Figure 2. System UVLO Setting Circuit

● **DC/DC Converter CH-1, CH-2, CH-3**

CH-1, CH-2 and CH-3 are PWM controllers. CH-1 is for Boost, CH2 is synchronous rectifier Buck and CH-3 is fixed 3.3V for Buck. Implementing over current protection circuit. The maximum duty cycle of CH-1 is internally limited to 86%, CH-2, CH-3 to 84%.

● **Charge Pump Circuit VGH, VGL**

VGH is positive charge pump circuit, and VGL is negative one. These also operate in PFM mode. The pulse duty of VGH is fixed 50%, VGL is fixed 18%.

● **High Voltage LDO**

Figure 3 shows the circuit of High Voltage LDO. Connect to an external output capacitor (Typ:2.2μF). High voltage LDO has built-in auto-recovery current limit function. The threshold current is 250mA. The output voltage is given by the following formula.

$$Vhldo = VREF \times \left(1 + \frac{R1}{R2}\right) = 1.2 \times \left(1 + \frac{R1}{R2}\right)$$

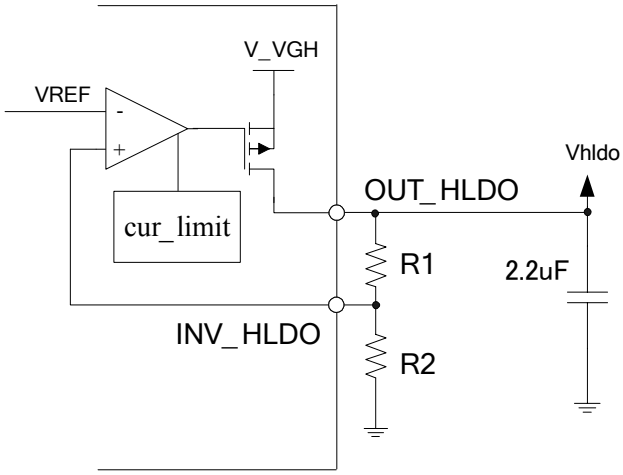


Figure 3. High Voltage LDO Circuit

● **VGH_OK**

VGH_OK pin is open drain output of NMOS pull-down transistor. When the power supply is turned On, VGH_OK pin is Gnd level. When the voltage on VGH reaches 85% of normal output voltage, NMOS transistor is turned Off.

● **Soft Start**

To prevent excessive rise of output voltage during start-up. THV3058 have soft start circuits within CH-1, CH-2, CH-3 and load switch circuit. The output voltages of these internal soft start circuits rise according to each internal start-up sequences, and then make the output of DC/DC converter and the output after load switch rise up. Soft start operation is completed when these outputs have reached each regular voltages.

Soft start time of CH-2 is 7msec and CH-1, CH-3 and load switch are set to 10msec (See Figure 4).

● **Start-up Sequence**

Figure 4 shows the waveform of start-up sequence. CH-1 and CH-3 are operate after CH-2 is generated completely. VGL starts after the start-up of CH-1 is completed. VGH starts with 5msec delay, after VLS signal is generated.

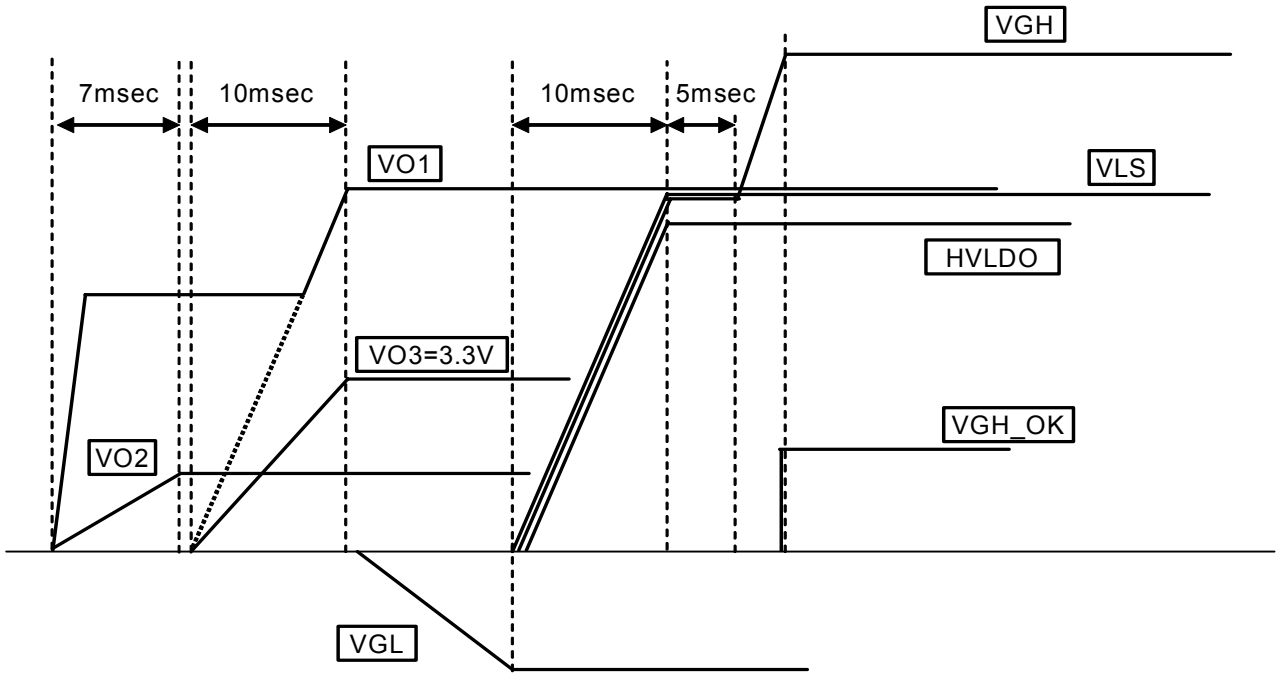


Figure 4. Start-up Sequence Waveforms

● **Thermal Shut Down(TSD)**

THV3058 has the built-in Thermal Shut Down circuit to prevent damages caused by excessive heat. When the junction temperature reaches 175°C, TSD circuit stops switching operation and the regulator VREG5 operation. The release temperature is 160°C.

● **Voltage Reference Circuit**

Voltage reference circuit generates temperature-compensated voltage(= 1.2V) for use as the internal reference volteage. Also, an external load current can be obtained from the power supply at VREF pin, up to 1mA, maximum. Please connect a capacitor of 0.01μF between VREF pin and SGND for stability.

● **Under Voltage Protection(UVP)**

UVP circuit shuts down the power supply, when the under voltage condition continues for longer time than a predetermined time. The internal comparator monitors the output voltage feedback pin. When the output voltage drops under a predetermined voltage, the timer latch circuit is activated (See Figure 5). When under voltage condition continues for more than 12.2msec, the device stops switching operation and goes into latch state. The timer will be reset, if UVLO operates before the device goes into the latch state.

In case of VGH and VGL, UVP is operated in 3msec after the startup. Please set the startup time of charge pumps within 15msec to prevent abnormal operation.

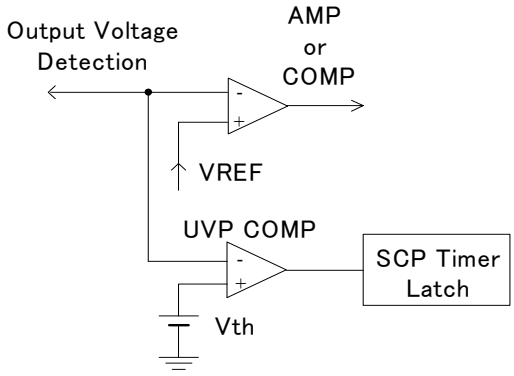


Figure 5. Under Voltage Detection Circuit

● **Over Voltage Protection(OVP)**

OVP shuts down the power supply, when the output voltage of CH-1, CH-2 and CH-3 exceeds a predetermined voltage. When the voltage of INV1 pin exceeds 1.5V on CH-1, INV2 pin exceeds 1.06V on CH-2 and ,VO3_IN pin exceeds 4.13V on CH-3, controller turns off an external MOS transistor and stops switching operation, respectively (See Figure 6).

As to CH-2 and CH-3, when abnormal output is detected, timer latch circuit is activated. When abnormal output continues 2.44msec, the device stops switching operation and goes into the latch state.

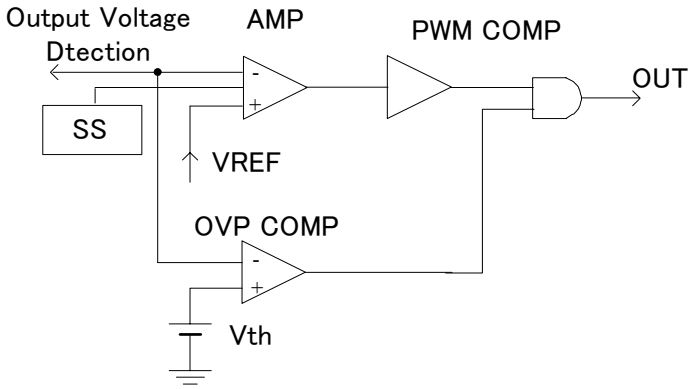


Figure 6. Over Voltage Detection Circuit

● **Over Current Protection(OCP)**

CH-1, CH-2 and CH-3 have built-in over current protection circuit. Over current detection circuit monitors the load current. When load current exceeds a predetermined current, the external MOS transistor is turned off and the device stops switching operation for 128usec(See Figure 7, 8, 9). The maximam current are given by the following formulas.

$$I_{max1} = \frac{Vin}{Vo1} \times \frac{Vcs1}{Rcs1} = \frac{Vin}{Vo1} \times \frac{0.1}{Rcs1} \ [A]$$

$$I_{max2} = \frac{Vcs2}{Rcs2} = \frac{0.1}{Rcs2} \ [A]$$

$$I_{max3} = \frac{Vcs3}{Rcs3} = \frac{0.175}{Rcs3} \ [A]$$

If the over current is detected continuously, the switching pulse is generated at 128usec interval and that causes output voltage drop. When the output voltage drops below the predetermined voltage for more than 12.2msec, SCP stops switching operation and the device goes into latch state.

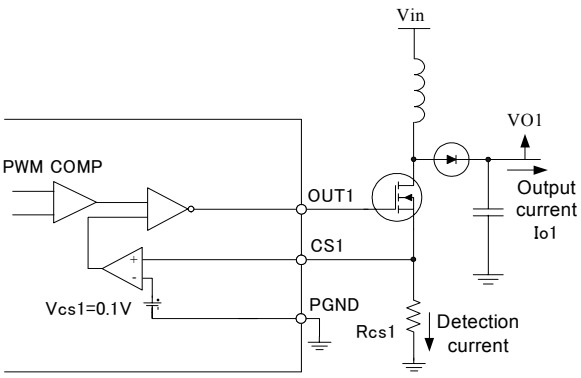


Figure.7 CH-1 Over Current Detection Circuit

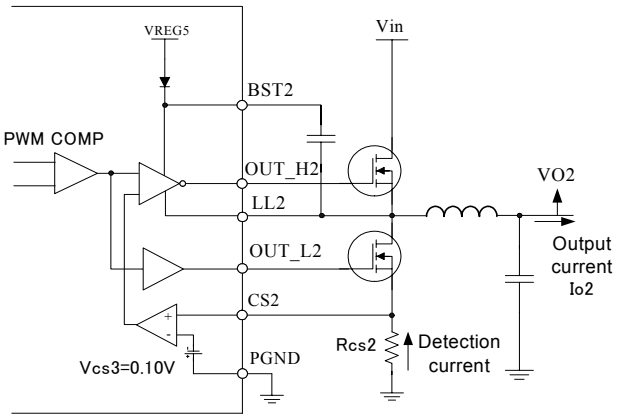


Figure.8 CH-2 Over Current Detection Circuit

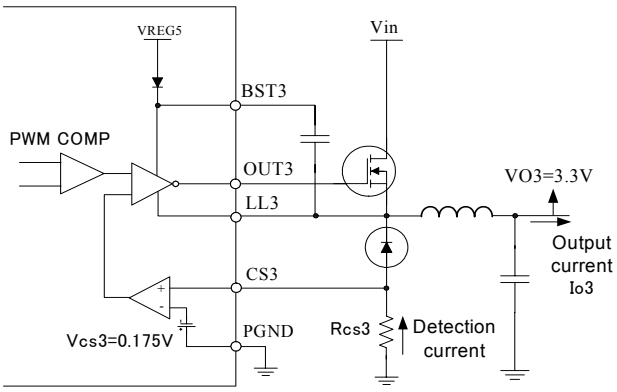


Figure.9 CH-3 Over Current Detection Circuit

● **Output Voltage Setting**

Figure 10 shows CH-1 and CH-2 output voltage setting model. The voltage on INV1 pin is equal to the voltage on VREF pin due to the effect of feed-back. The voltage on INV_1 pin is the divided voltage of Vout by R1 and R2.

So,

$$Vout1 \times \frac{R2}{R1+R2} = VREF$$

Therefore,

$$Vout1 = VREF \times \left(1 + \frac{R1}{R2}\right)$$

Since VREF =1.2V, then

$$Vout1 = 1.2 \times \left(1 + \frac{R1}{R2}\right)$$

Similarly the output voltage of CH-2 is described as follows.

$$Vout2 = 0.85 \times \left(1 + \frac{R4}{R5}\right)$$

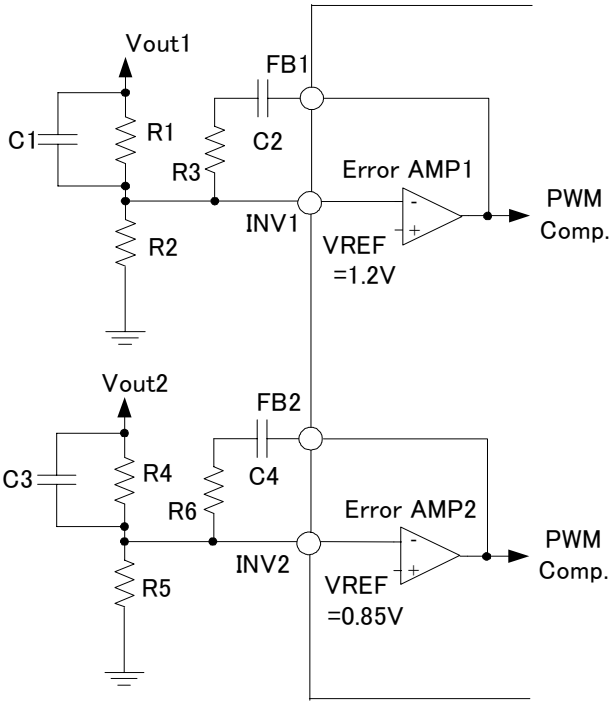


Figure 10. Output Voltage Setting

Description of charge pumps. As to VGH, the voltage on INV_VGH pin is controlled to be equal to the voltage of VREF (See Figure 11). The voltage on INV_VGH pin is the divided voltage of VGH by R9 and R10.
So

$$VGH = VREF \times \left(1 + \frac{R7}{R8}\right) = 1.2 \times \left(1 + \frac{R7}{R8}\right)$$

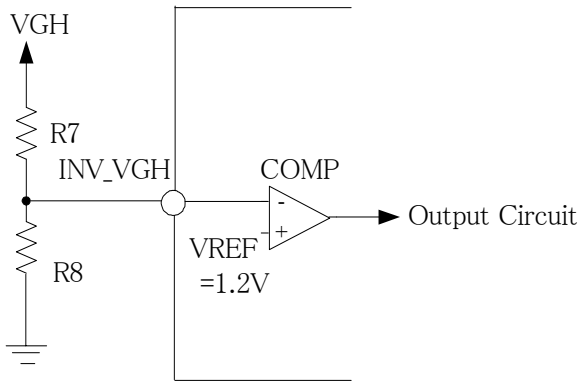


Figure 11. Output Setting for VGH

As to VGL, the voltage on NON_VGL pin is controlled to be zero (See Figure 12, Figure 13). The current through NON_VGL is negligible.
Therefore

$$VGL = -(VREF) \times \frac{R9}{R10} = -1.2 \times \frac{R9}{R10}$$

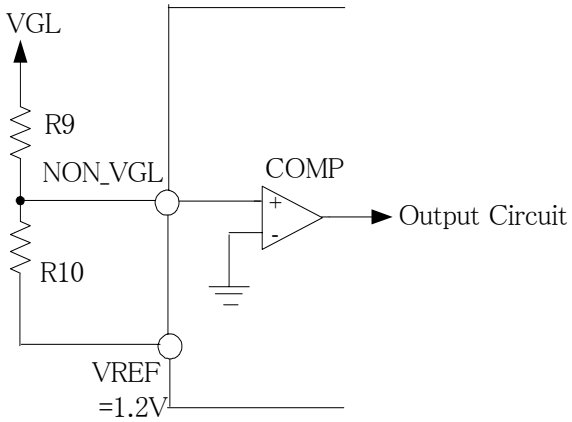


Figure 12. Output Setting for VGL

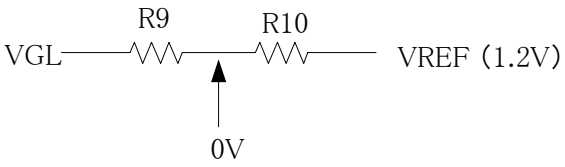
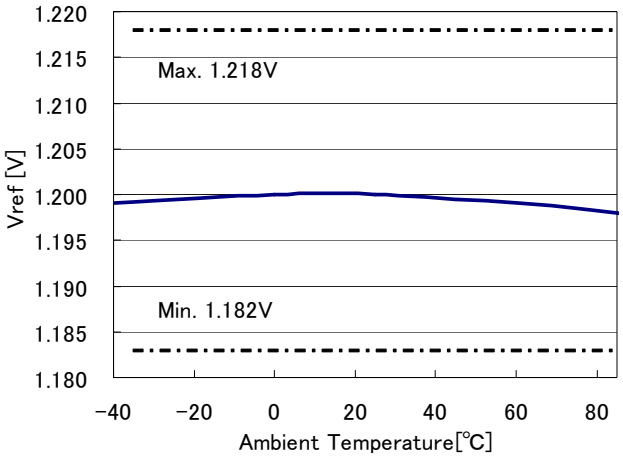


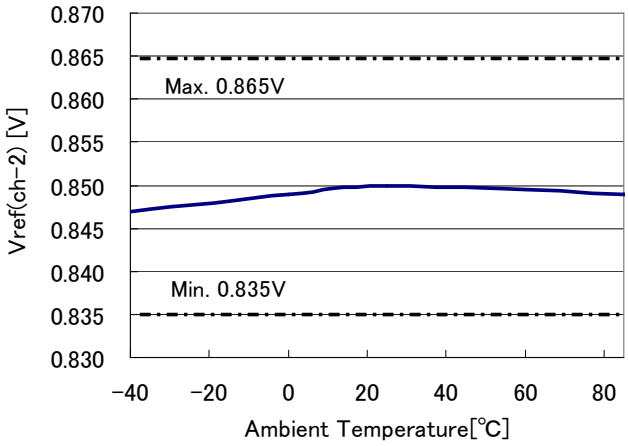
Figure 13. Output Setting for Inverting Mode

Temperature Characteristics

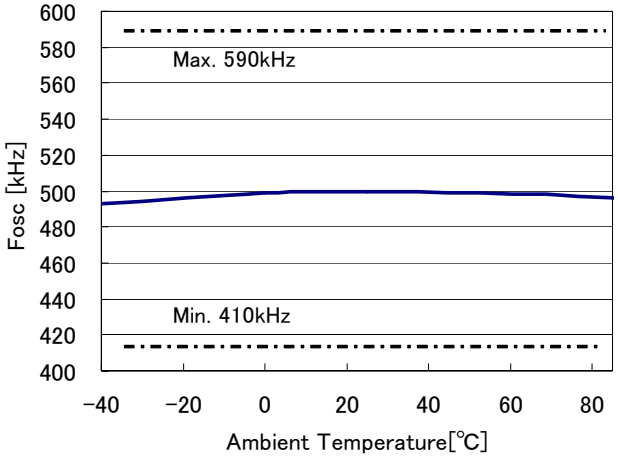
VREF vs Ambient Temperature



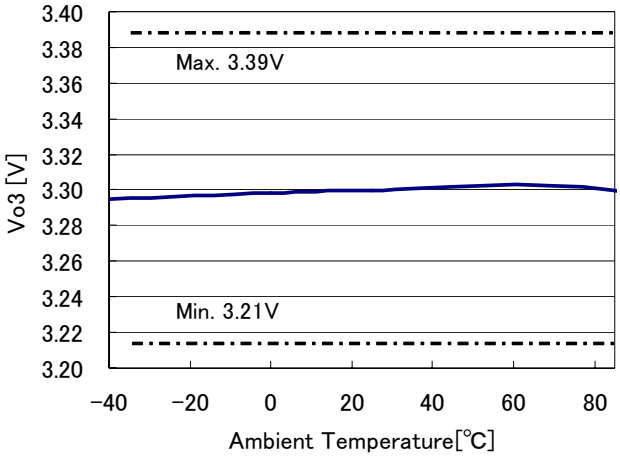
VREF (ch-2) vs Ambient Temperature



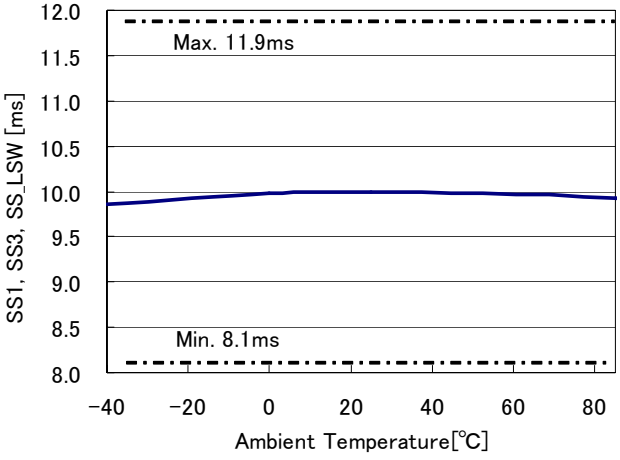
Oscillation Frequency vs Ambient Temperature



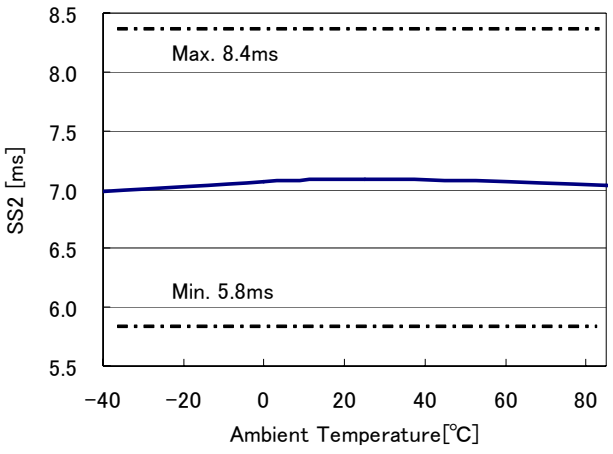
Vo3 vs Ambient Temperature



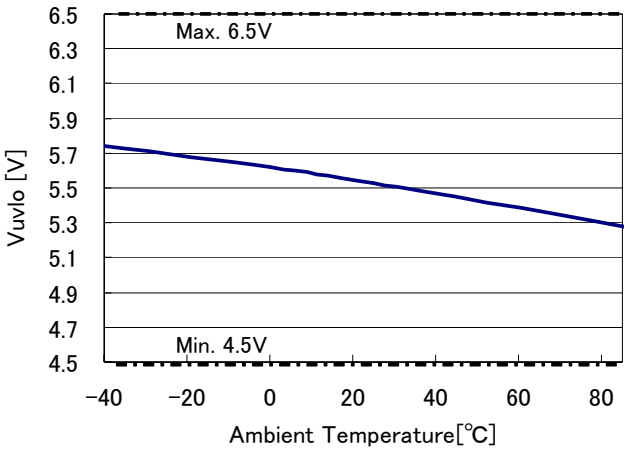
SS1, SS3, SS_LSW vs Ambient Temperature



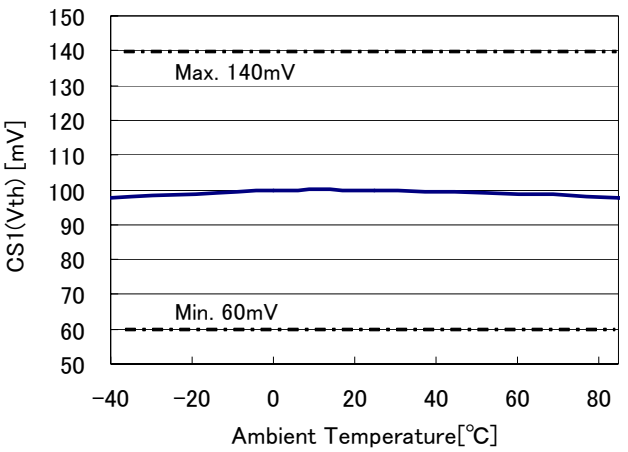
SS2 vs Ambient Temperature



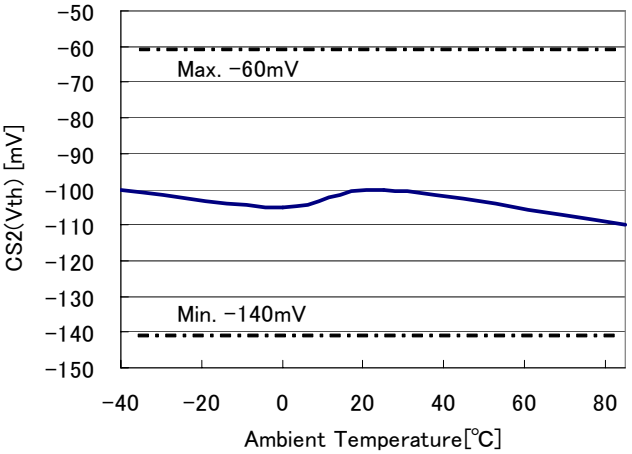
UVLO vs Ambient Temperature



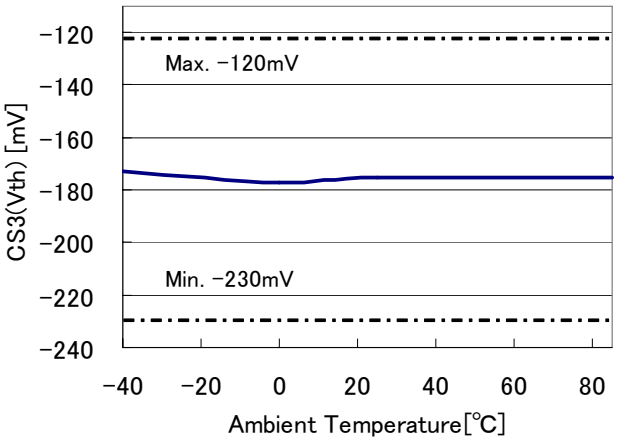
CS1(Vth) vs Ambient Temperature



CS2(Vth) vs Ambient Temperature

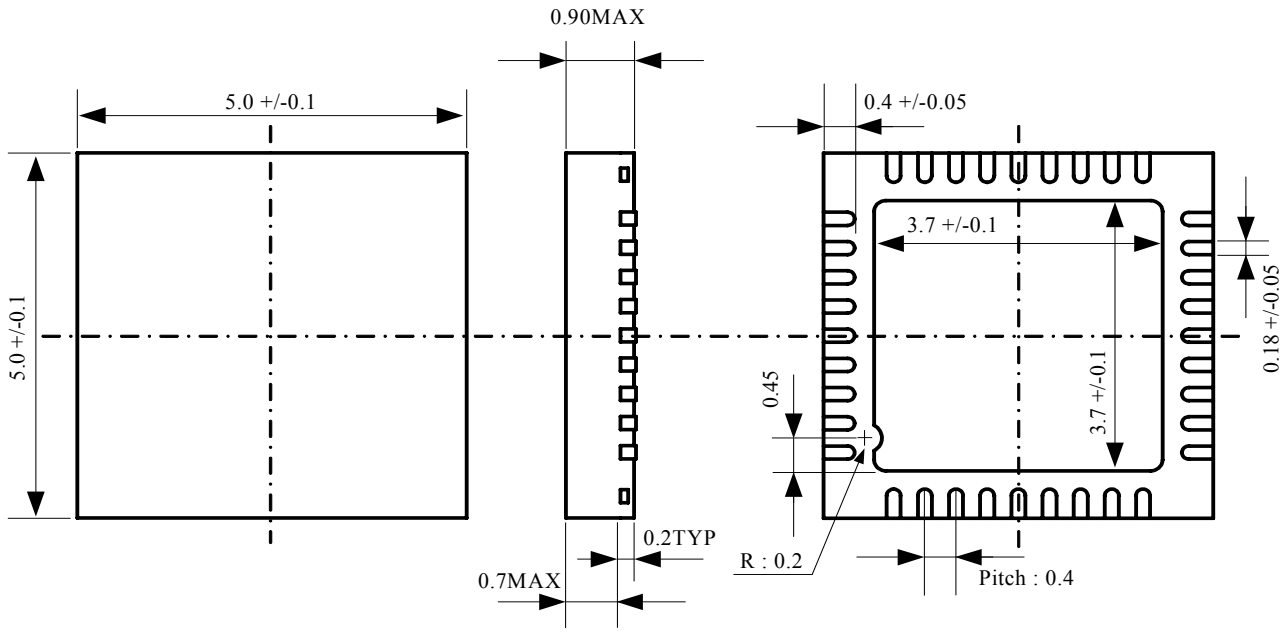


CS3(Vth) vs Ambient Temperature



Package Outline

QFN36 pin



Note) The Back Side of Exposed Pad must be connected to GND, in order to improve thermal properties.

Unit : mm

Notices and Requests

1. The product specifications described in this material are subject to change without prior notice.
2. The circuit diagrams described in this material are examples of the application which may not always apply to the customer's design. We are not responsible for possible errors and omissions in this material. Please note if errors or omissions should be found in this material, we may not be able to correct them immediately.
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5. This product is presumed to be used for general electric equipment, not for the applications which require very high reliability (including medical equipment directly concerning people's life, aerospace equipment, or nuclear control equipment). Also, when using this product for the equipment concerned with the control and safety of the transportation means, the traffic signal equipment, or various Types of safety equipment, please do it after applying appropriate measures to the product.
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7. Please note that this product is not designed to be radiation-proof.
8. Customers are asked, if required, to judge by themselves if this product falls under the category of strategic goods under the Foreign Exchange and Foreign Trade Control Law.
9. The product or peripheral parts may be damaged by a surge in voltage over the absolute maximum ratings or malfunction, if pins of the product are shorted by such as foreign substance. The damages may cause a smoking and ignition. Therefore, you are encouraged to implement safety measures by adding protection devices, such as fuses.

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