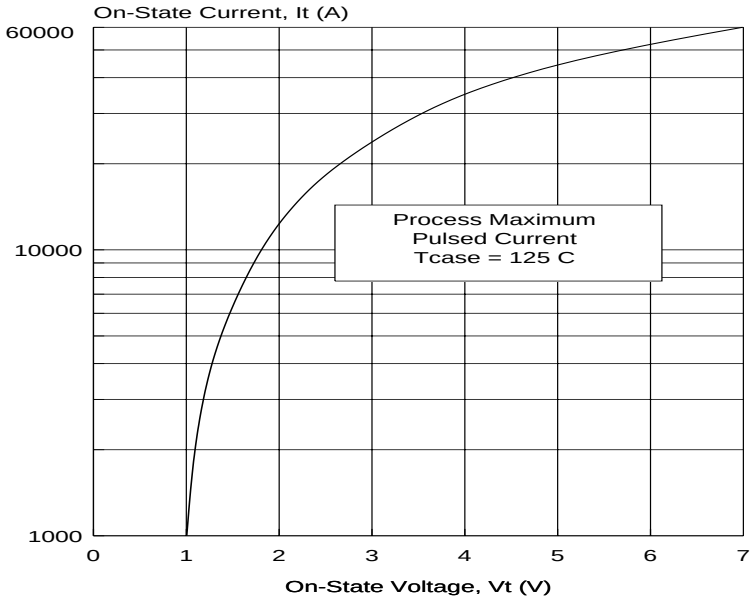
SPT315 100mm THYRISTOR
2500V / 4700A

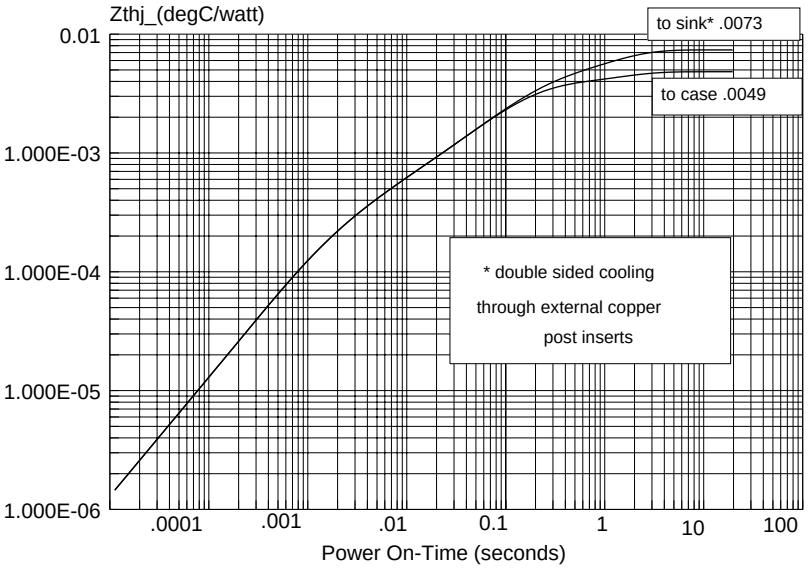
Type SPT315 thyristor is optimized especially for pulse power and static transfer switch applications for which lowest on-state voltage is achieved. The silicon junction design utilizes a second generation pilot gate and a unique orientation of emitter shorts which promote the lateral expansion of conducting plasma resulting in lower spreading losses while achieving high dv/dt withstand. It is supplied in a **reliable plastic light weight package**. The design utilizes a new termination technique which eliminates heavy refractory metal as a substrate but still employs the alloyed anode interface necessary for high surge current duty. External posts are available for adjoining commercially available heat dissipators using clamping hardware.

ON-STATE CHARACTERISTIC
Process Maximum



01A

THERMAL IMPEDANCE vs. ON-TIME



Maximum Off-State & Reverse Blocking Voltage Ratings

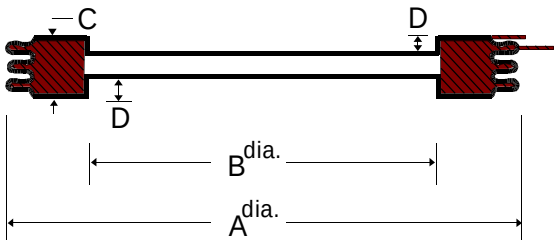
T_J = 0 to 115°C

	V_{DRM} (volts)	V_{RRM}
SPT315DK	2500	2500
SPT315DH	2400	2400
SPT315DF	2300	2300
SPT315DD	2200	2200
SPT315DB	2100	2100
SPT315TT	2000	2000

External clamping force
15000 - 18000 lb

Optional external posts drw.# 0215B8331
Ni plated copper, 0.350" thick each.
Compressed thickness including external posts
0.885"

Weight: 10 oz
2 lb 9 oz with posts



Nominal Dimensions

	inch	mm
A dia.	5 3/8	136.5
B dia.	3 11/32	85
C	51/64	20.24
D	0.306	7.77

02/15/01

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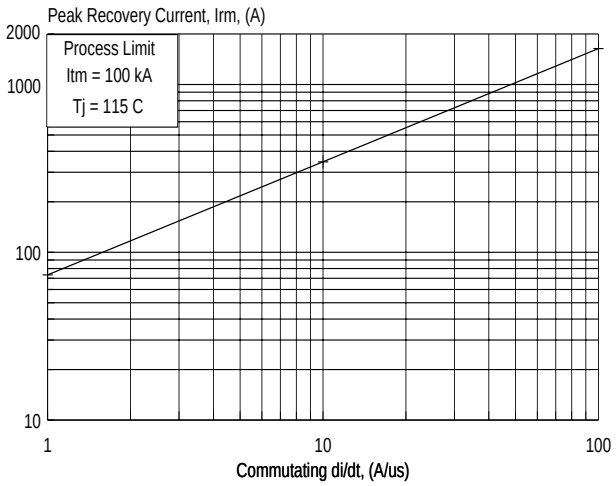
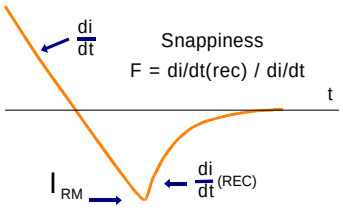
175 GREAT VALLEY PKWY. MALVERN, PA 19355
USA

Repetitive peak off-state & reverse volts	V_{DRM} V_{RRM}	T_J=0 to 115°C	up to 2600	V
Repetitive peak off-state & reverse current	I_{DRM} I_{RRM}	T_J=0 to 115°C	300 300	ma
Average on-state current	$I_{T(AV)}$	T_{case}= 70°C	4700	A
Peak half-cycle non-rep surge current	I_{TSM}	8.3 ms 1.5 ms T_J=115°C	60 90	kA
On-state voltage	V_{TM}	I_T=4000A T_J=115°C	1.3	V
Critical gate trigger current / voltage	I_{GT} V_{GT}	V_D = 12 V T_J = 25°C	200 5	ma V
Non-trigger gate current	I_{GD}	V_D = 2000V T_J= 90°C	15	ma
Maximum peak recovery current	I_{RM}	di/dt = 2 A/us T_J = 115°C	117 snappiness	A F = 2-3
Critical rate of rise of on-state current	di/dt rep	T_J=115°C 60 Hz with 60A snubber discharge	100	A/us
Critical rate of rise of off-state voltage	dv/dt	T_J=90°C V_D= 67% V_{DRM}	1000	V/us
Turn-on delay	t_d	V_D= 50%V_{DRM} T_J=115°C	3	us
Turn-off time	T_{off}	5A/us, -100V 20V/us to 2000V	300	us

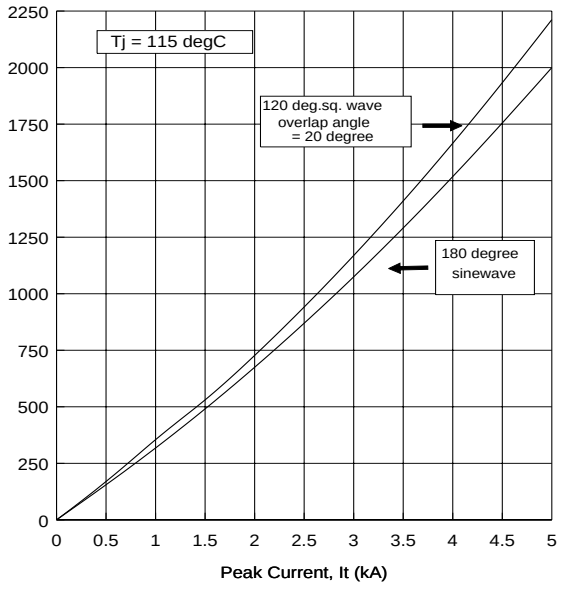
Peak Recovery Current Relationship
with Commutating di/dt





Recommended gate drive to sustain turn-on di/dt rating
V_{OC} = 40 V
I_{SS} = 4 A
rise time = 0.5 us
duration 10 - 20 us

FULL CYCLE AVERAGE POWER LOSS
versus
PEAK CURRENT at 50/60 Hz
(plasma spreading and conduction loss)



FULL CYCLE AVERAGE POWER LOSS
50 / 60 Hz T_J = 115°C

I_T (peak)	half-sine 180°	3ph 120°
amperes	watts	watts
500	153	162
1000	316	336
1500	489	524
2000	673	725
2500	868	939
3000	1073	1167
3500	1289	1408
4000	1516	1663
4500	1753	1930
5000	2000	2212