SILICON POWER

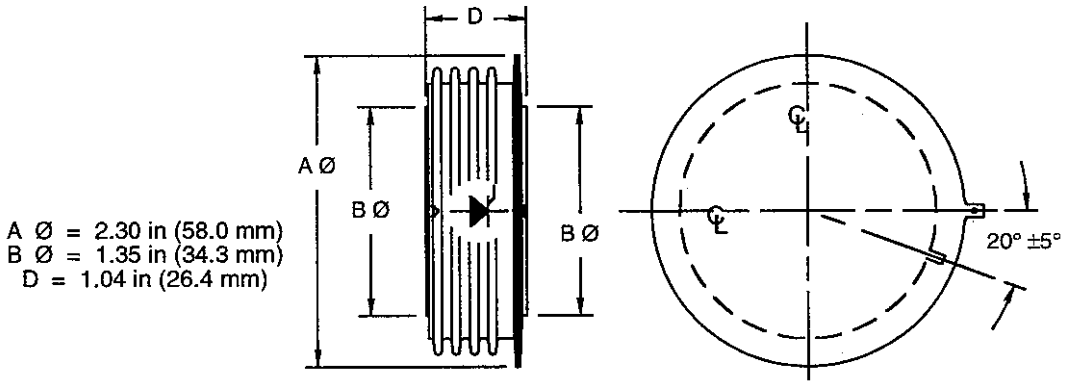
C612
40 mm Inverter Thyristor
2000V / 735A / 60us

The C612 is ideal for forced commutation. It is processed by multi-diffusion, utilizing 40mm diameter silicon with a unique involute pilot gate. It is supplied in a disk package ready to mount using commercially available heat dissipators and mechanical clamping hardware.

MAXIMUM ALLOWABLE RATINGS

TYPE	V_{DRM}/V_{RRM} [1] REPETITIVE T_J = -40°C to +125°C	V_{DRM}/V_{RRM} [1] REPETITIVE T_J = 0°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE [1] V_{RSM} T_J = -40°C to +125°C
C612L	2000 Volts	2100 Volts	2100 Volts
C612PT	1900	2000	2000
C612PN	1800	1900	1900
C612PS	1700	1800	1800
C612PM	1600	1700	1700
C612PE	1500	1600	1600

Peak One-Cycle Surge On-State Current, I_{TSM} (8.3 msec) . . . . . 9000 Amperes
Maximum Rate-of-Rise of Anode Current Turn-On Interval[2] . . . . . Switching from 1200 Volts, 500 A/μsec
Repetitive Rate-of-Rise of Anode Current . . . . . 200 A/μsec
I^2t (for fusing) (at 1.5 milliseconds) (See Figure 9) . . . . . 155,000 Ampere^2 Seconds
Peak Gate Power Dissipation, P_{GM} . . . . . 100 Watts
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 5 Watts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 20 Volts
Storage and Operating Temperature, T_{stg} and T_J . . . . . -40°C to +125°C
Mounting Force Required . . . . . 3500 – 4200 Lbs.
15.6 – 18.7 Kn



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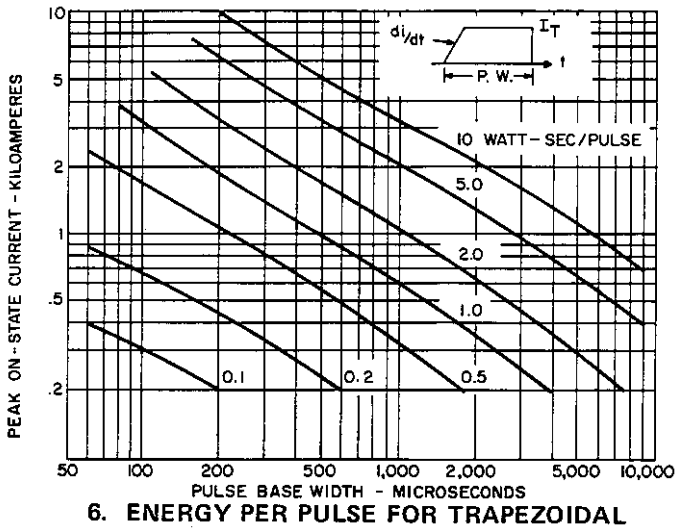
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	–	10	15	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Peak Off-State and Reverse Currents	I_{DRM} and I_{RRM}	–	45	60	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance Junction-to-Case, $R_{\theta JC}$	DC	–	–	.045	°C/watt	Double-Side Cooled
Critical Linear Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching)	dv/dt	200	–	–	V/μsec	T_J = +125°C, V_{DRM} = .80 Rated, Gate Open[1]
Delay Time	t_d	–	1.5	3.0	μsec	Switching from 1000 Volts, 20 Volt, 10 Ohm Gate 0.5 μsec Rise Time, T_J = 25°C
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	See Figure 7.
Gate Trigger Current (See Figure11)	I_{GT}	–	120	150	mAdc	T_C = 25°C, V_D = 10 Vdc, R_L = 3 Ohms
		5.0	30	–		T_C = +125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Gate Trigger Voltage (See Figure11)	V_{GT}	–	3.0	5.0	Vdc	T_C = 25°C, V_D = 10 Vdc, R_L = 3 Ohms
		.3	–	–		T_C = 125°C, V_D = .5 x Rated, R_L = 1000 Ohms
Peak On-State Voltage	V_{TM}	–	–	2.21	Volts	T_C = +125°C, I_T = 2000 Amps. Peak Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time(1) (With Reverse Voltage)	t_q –	–	55	60	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R ≥ 50 Volts (4) Rate-of-Rise of Forward Blocking Voltage = 200V/μsec to 80% of V_{DRM} or 400V/μsec to 70% of V_{DRM} (5) Gate Bias = Open During Turn-Off Interval = 0 Volts, 100 Ohms (6) Duty Cycle ≤ 0.01%
Conventional Circuit Commutated Turn-Off Time(1) (With Feedback Diode)	t_q	–	60	65	μsec	(1) T_C = +125°C (2) I_T = 500 Amps. (3) V_R = 5 Volts Min. (4) Rate-of-Rise of Forward Blocking Voltage = 400V/μsec to 70% of V_{DRM} (5) Gate Bias = Open During Turn-Off Interval (6) Duty Cycle ≤ 0.01%

(1) Turn-off times are measured on a go/no-go basis using LEM test equipment. Experimental determination of critical t_q may lead to device degradation.

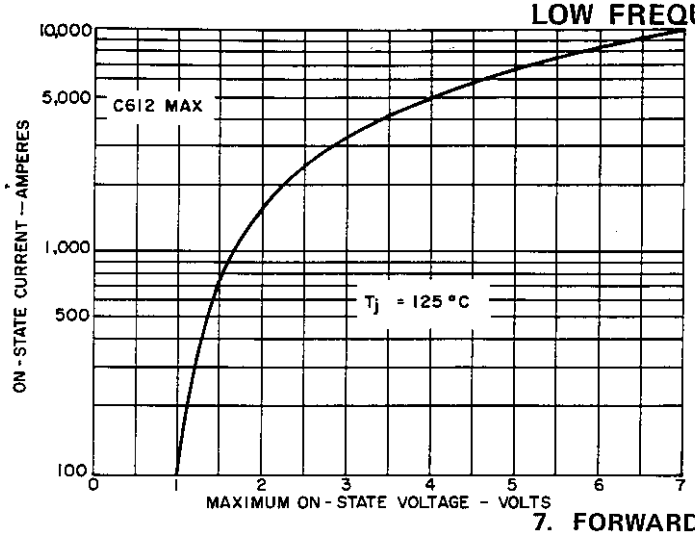


6. ENERGY PER PULSE FOR TRAPEZOIDAL CURRENT WAVEFORMS FOR 100 A/μSEC RISING DI/DT

NOTES:

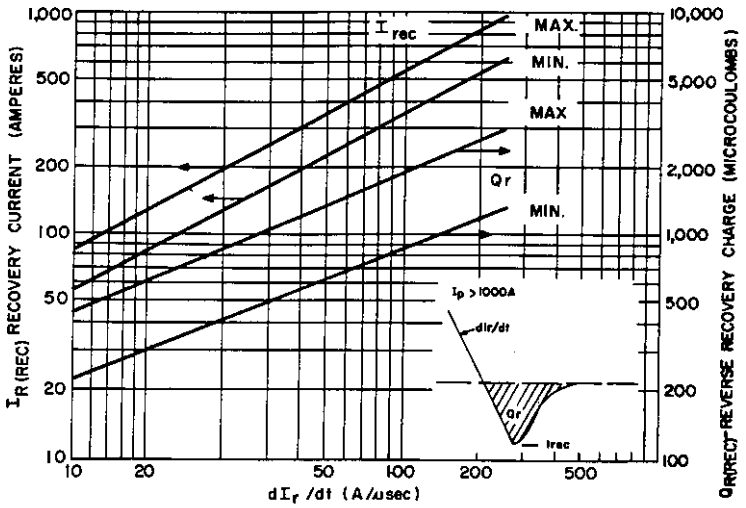
1. Switching voltage range: V_D = 15V – 0.8 V_{DRM}.
2. Peak snubber discharge current ⩽ 50A. RC ⩽ 10μsec.
3. High gate drive: 20V/10 Ohms, 0.5μsec. rise time.
4. Reverse voltage ⩽ 50V.

LOW FREQUENCY DATA



7. FORWARD CONDUCTION CHARACTERISTIC ON-STATE

NOTES:	VOLTAGE (Volts)	CURRENT (Amps)
	1.040	100
	1.153	200
	1.232	300
	1.300	400
	1.363	500
	1.422	600
	1.480	700
	1.537	800
	1.594	900
	1.650	1000
	1.706	1100
	1.762	1200
	1.818	1300
	1.873	1400
	1.929	1500
	2.210	2000
	2.781	3000
	3.363	4000
	3.954	5000
	4.552	6000
	5.157	7000
	5.767	8000
	6.382	9000
	7.000	10000

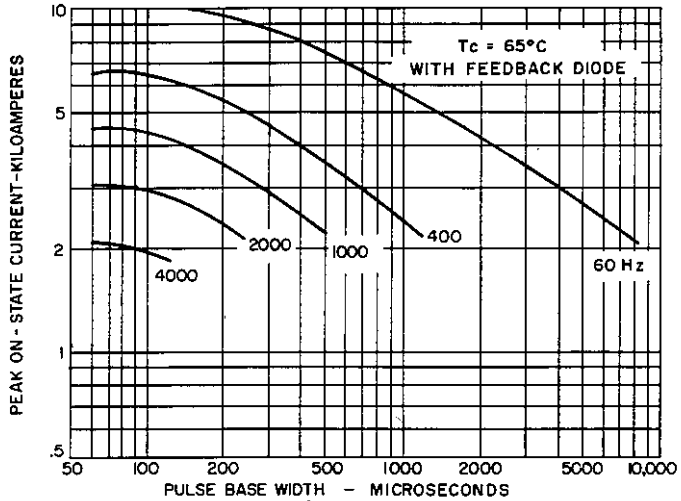


8. REVERSE RECOVERY CHARACTERISTICS (125°C)

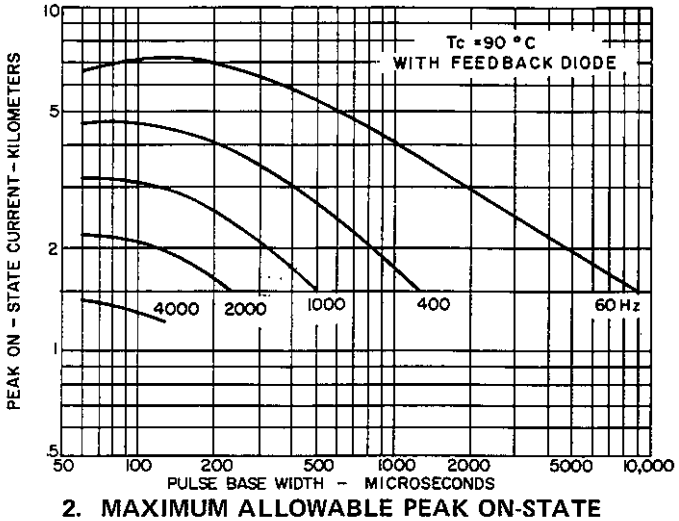
NOTES:

Curves are based upon production tests of I_{rec}. Q_r is a close approximation based upon calculation using appropriate value of I_{rec} and an emperical formula.

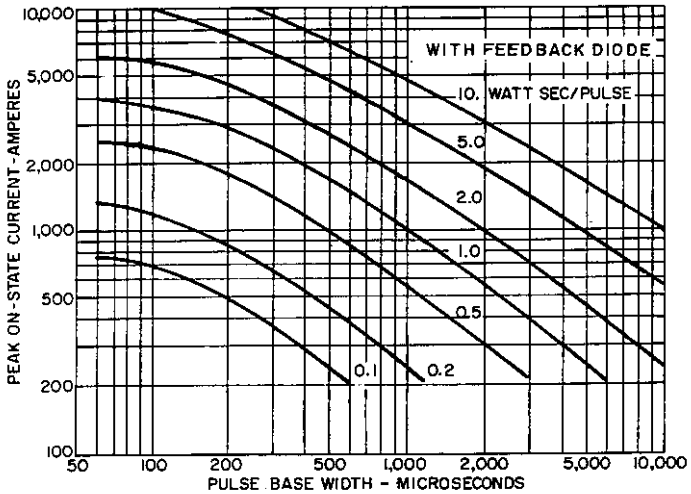
SINE WAVE DATA



1. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH (T_C = 65°C)



2. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT VS. PULSE WIDTH (T_C = 90°C)

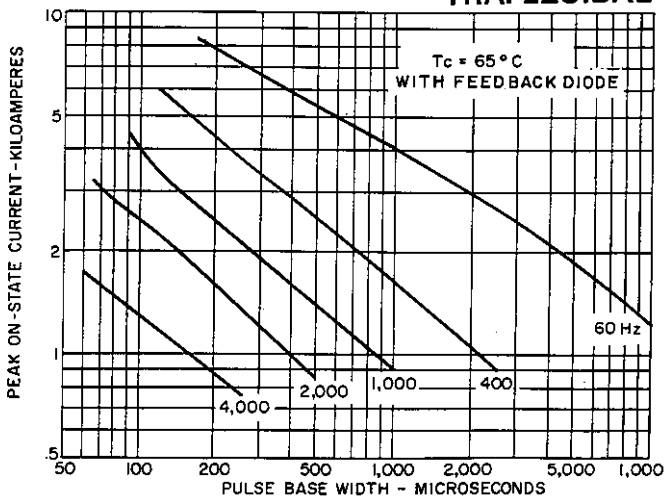


3. ENERGY PER PULSE FOR SINUSOIDAL PULSES

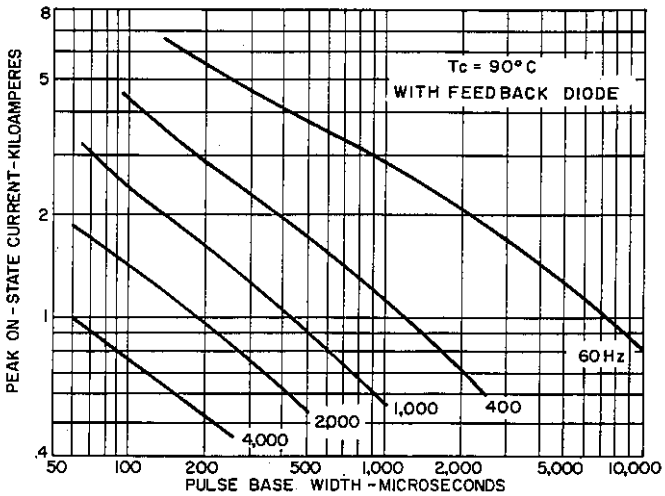
NOTES:

1. Switching voltage range: V_D = 15V – 0.8 V_{DRM}.
2. Peak snubber discharge current ⩽50A. RC⩽10μsec.
3. High gate drive: 20V/10 Ohms, 0.5μsec. rise time.
4. Reverse voltage < 50V. If no bypass diode is used, recovery switching losses must be added.

TRAPEZOIDAL WAVEFORM DATA



4. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING DI/DT = 100 A/μSEC (T_C = 65°C)



5. MAXIMUM ALLOWABLE PEAK ON-STATE CURRENT FOR RISING DI/DT = 100 A/μSEC (T_C = 90°C

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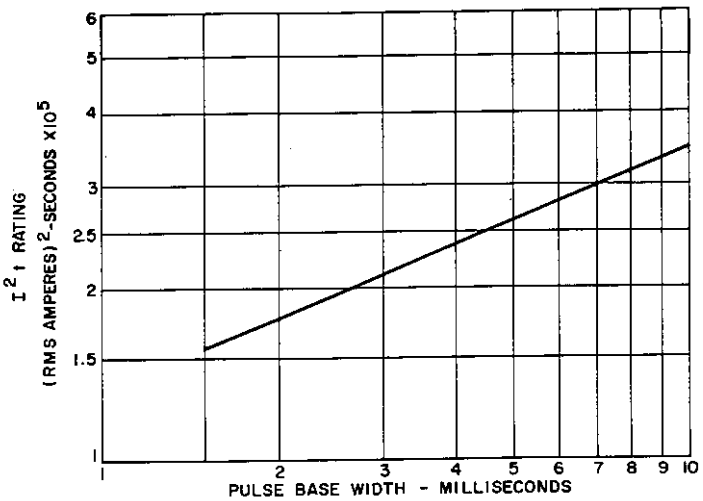
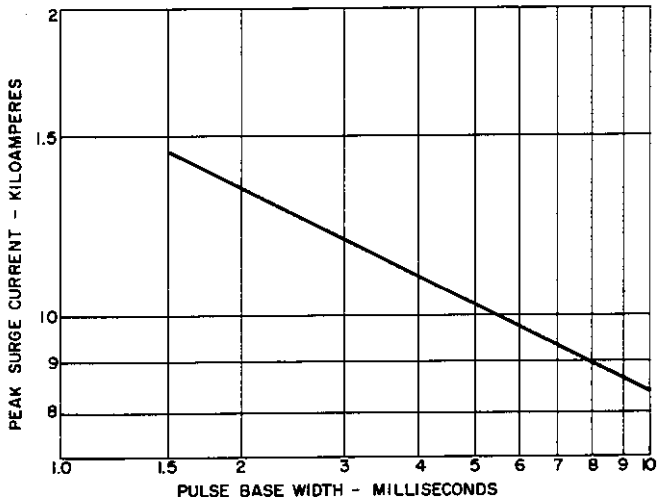
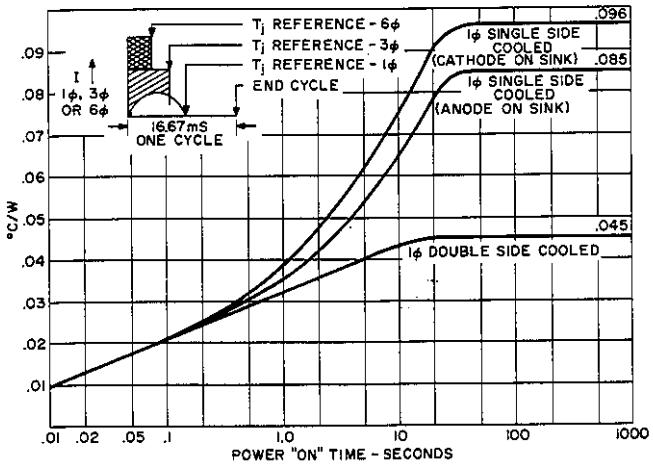




9. SUB-CYCLE SURGE AND I^2t RATING FOLLOWING RATED LOAD CONDITIONS (Sinusoidal Waveform)



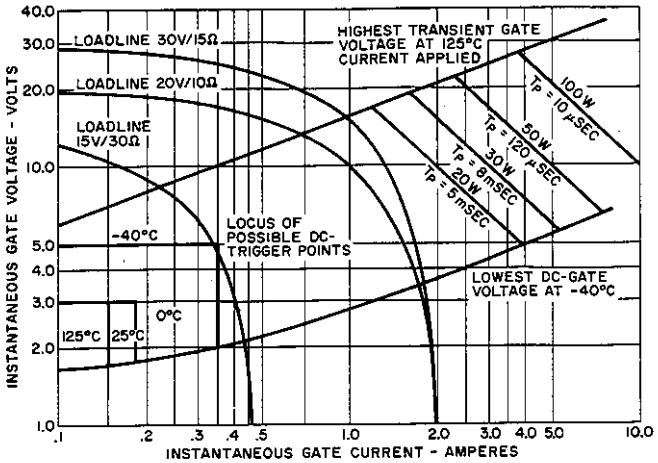
NOTES:

For 3ϕ thermal resistance add .0037°C/W along entire curve length.

For 6ϕ thermal resistance add .001°C/W along entire curve length.

For DC thermal resistance subtract .005°C/W along entire curve length.

10. TRANSIENT THERMAL IMPEDANCE – JUNCTION-TO-CASE



NOTES:

1. Maximum allowable gate dissipation = 3 watts.
2. The locus of possible DC-trigger points lies outside the boundaries shown at various junction temperatures.
3. Loadlines 30V/15 Ω, 20V/10 Ω and similar are recommended as minimum gate drives for most inverter application: rise time $\leq 0.5\,\mu$sec; $T_p \geq 10\,\mu$sec.
4. Loadline 15V/30 Ω is the minimum usable gate drive. Snubber resistances must be $> 30\ \Omega$ when turning on from ≥ 800V bias. Delay-time may be increased. di/dt rating ≤ 100A/μsec.

11. MAXIMUM ALLOWABLE PEAK GATE POWER VS. GATE PULSE WIDTH