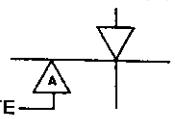
SILICON POWER

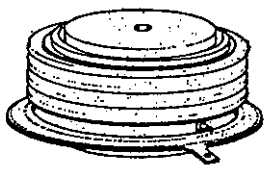
High Power Silicon Controlled Rectifier

1800 Volts 750A Avg.

C441



The C441 Silicon Controlled Rectifier is designed for phase control applications. This is an all-diffused Press-Pak device employing the field-proven amplifying gate.



FEATURES:

- High di/dt Ratings
- High dv/dt Capability with Selections Available
- Excellent Surge and I^2t Ratings Providing Easy Fusing
- Guaranteed Maximum Turn-Off Time with Selections Available
- Rugged Hermetic Glazed Ceramic Package Having 1" Creepage Path

IMPORTANT: Mounting instructions on the last page of this specification must be followed.

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM}[1] T_J = -40°C to +125°C	REPETITIVE PEAK REVERSE VOLTAGE, V_{RRM}[1] T_J = -40°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V_{RSM}[1] T_J = +125°C
C441PC	1300 Volts	1300 Volts	1470 Volts
C441PD	1400	1400	1580
C441PE	1500	1500	1700
C441PM	1600	1600	1790
C441PS	1700	1700	1920
C441PN	1800	1800	2040

[1] Half sinewave waveform, 10 msec max. pulse width.

Average On-State Current, $I_{T(AV)}$ . . . . . Depends on Conduction Angle (See Charts 1 and 2)
Peak One-Cycle Surge (Non-Repetitive) On-State Current, I_{TSM} (60 Hz) . . . . . 11,000 Amperes
Peak One-Cycle Surge (Non-Repetitive) On-State Current, I_{TSM} (50 Hz) . . . . . 10,000 Amperes
Critical Rate-of-Rise of On-State Current (Non-Repetitive)† . . . . . 150 A/μs
Critical Rate-of-Rise of On-State Current (Repetitive)† . . . . . 75 A/μs
I^2t (for fusing) (for times $\geq$ 1.5 milliseconds) See Figure 7 . . . . . 280,000 (RMS Ampere)^2 Seconds
I^2t (for fusing) (at 8.3 milliseconds) . . . . . 500,000 (RMS Ampere)^2 Seconds
Peak Gate Power Dissipation, P_{GM} . . . . . 200 Watts @ 40 μsec Pulse
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 5 Watts
Storage Temperature, T_{stg} . . . . . -40°C to +150°C
Operating Temperature, T_J . . . . . -40°C to +125°C
Mounting Force Required . . . . . 3000 Lbs. – 3500 Lbs.
13.3 Kn – 15.6 Kn

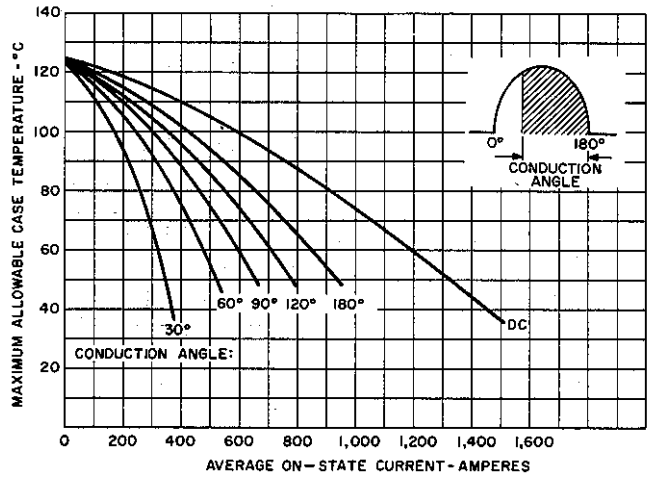
NOTE:

† di/dt ratings established in accordance with EIA-NEMA Standard RS-397, Section 5.2.2.6 for conditions of $V_{DRM} \leq 1300V$; 20 volts, 20 ohms gate trigger source with 0.5 μs short circuit trigger current rise time.

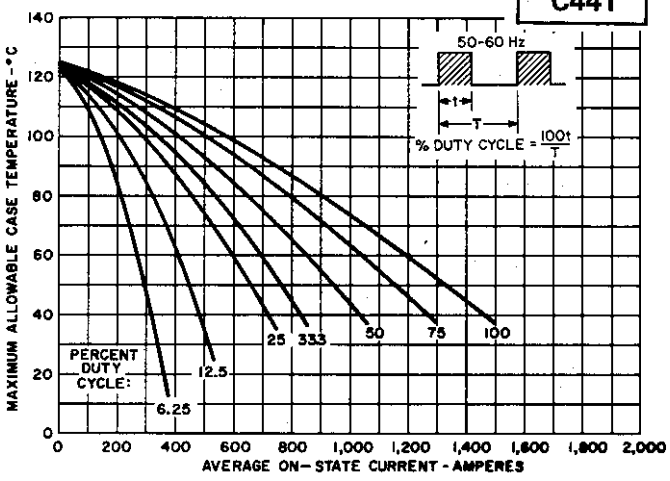
CHARACTERISTICS

TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Repetitive Peak Reverse and Off-State Currents	I_{RRM} and I_{DRM}	–	10	15	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Repetitive Peak Reverse and Off-State Current	I_{RRM} and I_{DRM}	–	15	35	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Thermal Resistance	$R_{\theta JC}$	–	–	0.04	°C/Watt	Junction-to-Case (Double-Side Cooling)
Critical Rate-of-Rise of Off-State Voltage (Higher values may cause device switching)	dv/dt	200	–	–	V/μsec	T_J = +125°C, 0.8 x V_{DRM} Applied, Using Linear Exponential Rising Waveform, Gate Open. Exponential dv/dt = $0.8 \frac{V_{DRM}}{\tau}$ (.632)
Higher minimum dv/dt selection available – consult factory.						
DC Holding Current	I_H	–	500	–	mAdc	T_C = +25°C, Anode Supply = 24 Vdc, Initial On-State Current = 2 Amps.
DC Latching Current	I_L	–	.25	–	Adc	T_C = +25°C, Anode Voltage = 24 Vdc, Load Resistance 12 Ohms Max.
Turn-On Delay Time	t_d	–	0.7	–	μsec	T_C = +25°C, I_T = 50 Adc. Gate Supply: 20 Volts, 20 Ohms, 0.1 μsec max. rise time
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	T_C = +25°C. Gate Supply: 10 Volt Open Circuit, 5 Ohms, 0.1 μsec rise time
DC Gate Trigger Current See Figure 10 for Recommended Gate Drive Conditions	I_{GT}	–	–	150	mAdc	T_C = +25°C, V_D = 6 Vdc, R_L = 3 Ohms
		–	–	300		T_C = -40°C, V_D = 6 Vdc, R_L = 3 Ohms
		–	–	125		T_C = +125°C, V_D = 6 Vdc, R_L = 3 Ohms
DC Gate Trigger Voltage See Figure 10	V_{GT}	–	–	5	Vdc	T_C = -40°C to +125°C, V_D = 6 Vdc, R_L = 3 Ohms
		.15	–	–		T_C = +125°C, V_D = Rated V_{DRM}, R_L = 1000 Ohms
Peak On-State Voltage	V_{TM}	–	–	2.0	Volts	T_C = +25°C, I_T = 3000 Amps. Peak. Duty Cycle ≤ 0.01%
Circuit Commutated Turn-Off Time	t_q*	–	125	–	μsec	(1) T_C = +125°C (2) I_{TM} = 500 Amps (3) V_R = 50 Volts Min. (4) 0.8 V_{DRM} Reapplied (5) Rate-of-Rise of Reapplied Off-State Voltage = 20 V/μsec (linear). (6) Commutation di/dt = 25 Amps/μsec (7) Repetition Rate = 1 pps (8) Gate Bias During Turn-Off Interval = 0 Volts, 100 Ohms

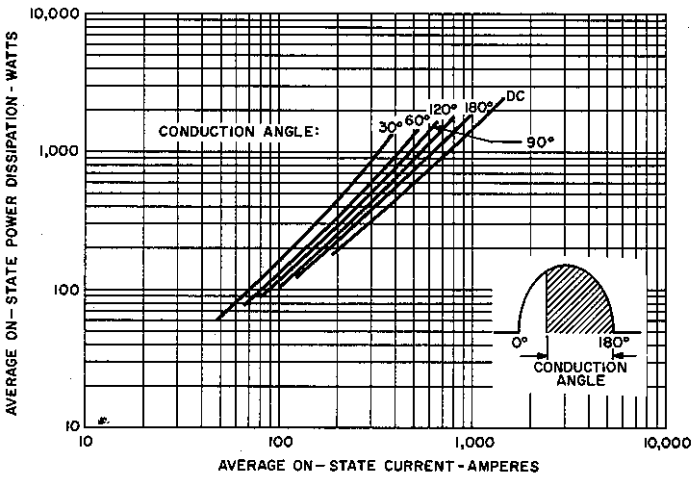
*Contact factory for maximum t_q specification.



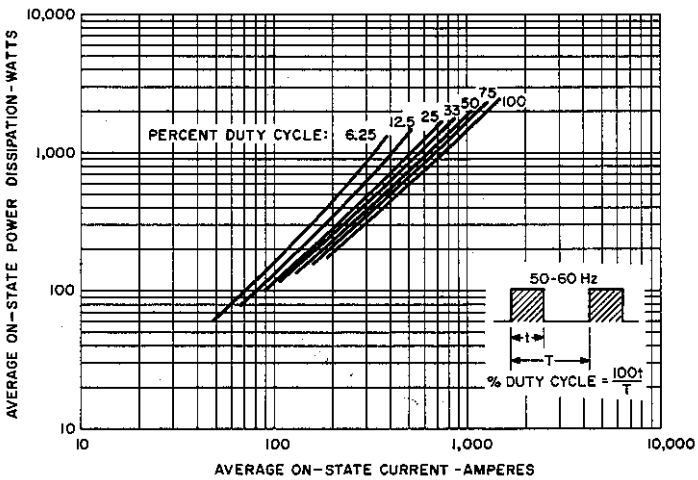
1. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM – DOUBLE-SIDE COOLED



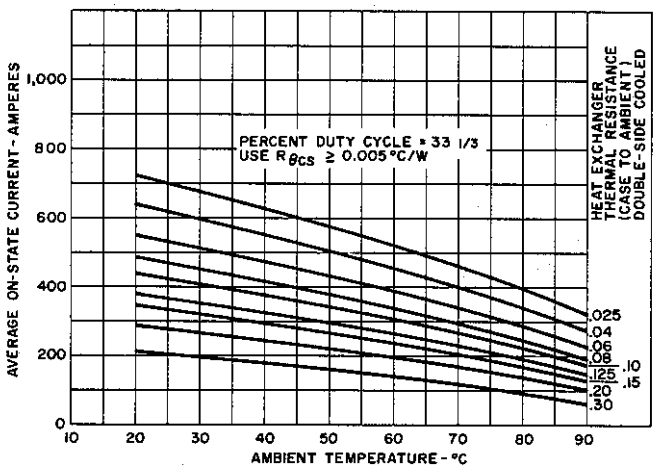
2. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM – DOUBLE-SIDE COOLED



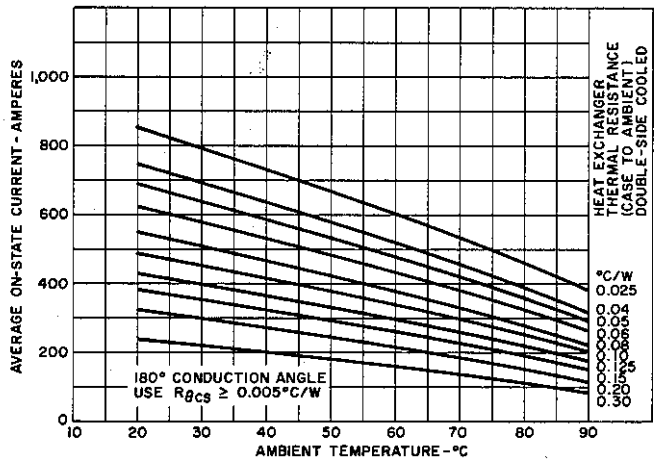
3. MAXIMUM ON-STATE POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



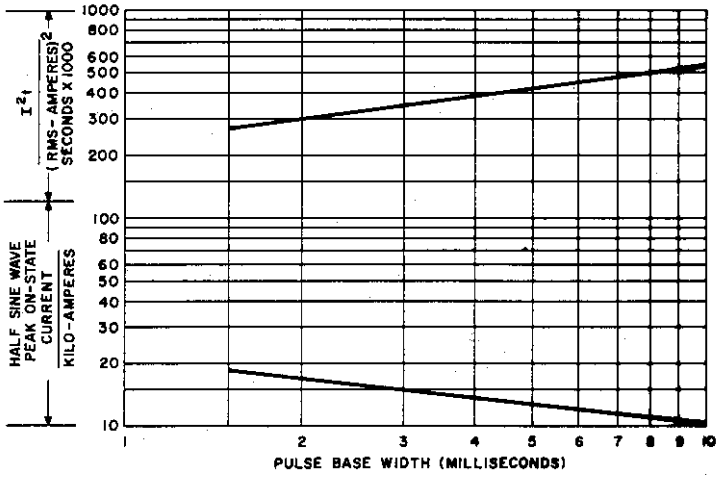
4. MAXIMUM ON-STATE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



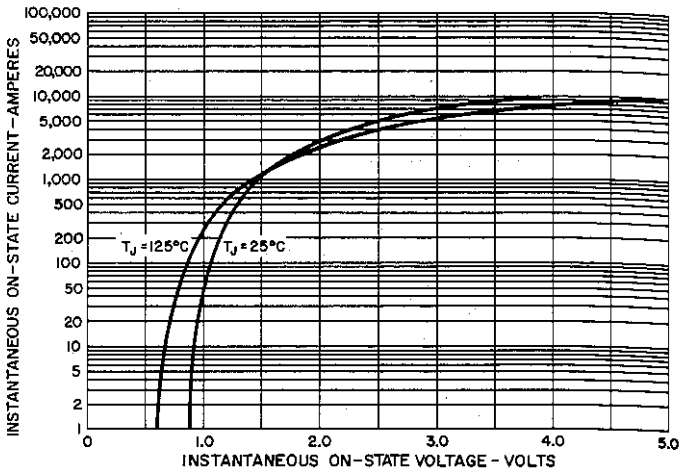
5. MAXIMUM RECTANGULAR ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



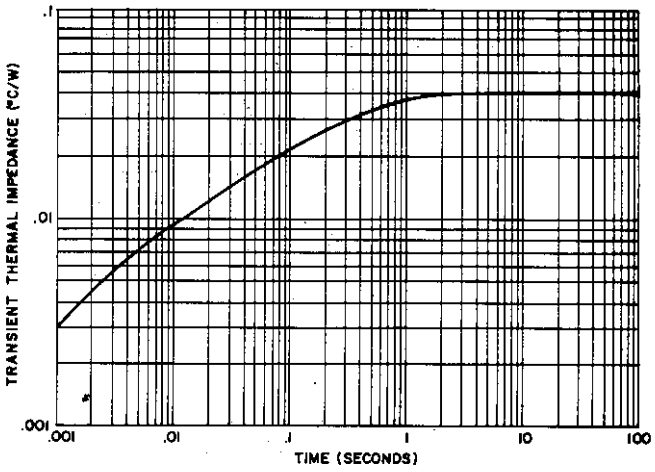
6. MAXIMUM HALF SINEWAVE ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



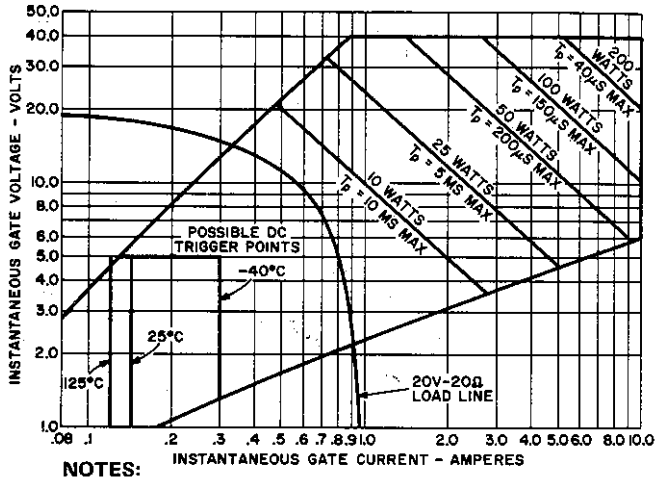
7. SUB-CYCLE SURGE (NON-REPETITIVE) ON-STATE AND I^2t RATING



8. MAXIMUM ON-STATE CHARACTERISTICS



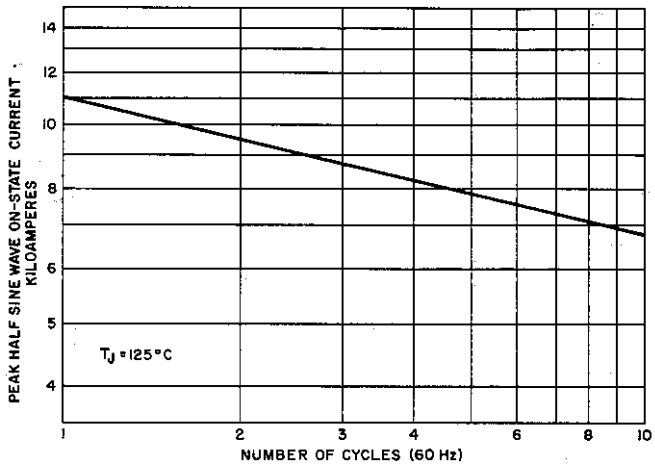
9. TRANSIENT THERMAL IMPEDANCE — JUNCTION-TO-CASE (DOUBLE-SIDE COOLED)



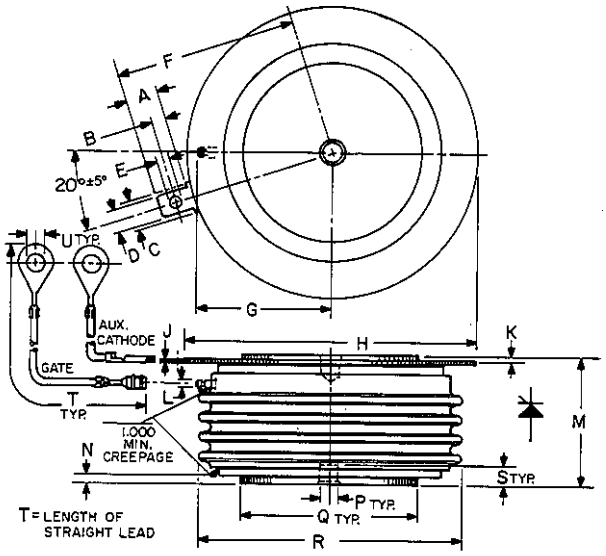
NOTES:

1. Maximum allowable average gate dissipation = 5 watts.
2. The locus of possible DC trigger points lies outside the boundaries shown at various case temperatures.
3. Tp = Rectangular Gate Current Pulse Width.

10. GATE TRIGGERING CHARACTERISTICS



11. MAXIMUM ALLOWABLE SURGE (NON-REPETITIVE) ON-STATE CURRENT



SYM	DECIMAL INCHES MIN.	DECIMAL INCHES MAX.	METRIC M.M. MIN.	METRIC M.M. MAX.
A	.240	.260	6.096	6.604
B	.110	.130	2.794	3.302
C	.245		6.223	
D	.186	.191	4.724	4.851
E	.060	.075	1.524	1.905
F		1.430		36.32
G		1.065		27.051
H	2.200	2.500	55.88	63.50
J	.011	.019	2.794	3.483
K	.030	.130	.762	3.302
L	.056	.060	1.422	1.524
M	1.000	1.065	25.40	27.05
N	.030	.096	.762	2.438
P	.130	.150	3.302	3.810
Q	1.300	1.345	33.02	34.16
R		2.150		54.61
S	**.067**	**.083**	**1.702**	**2.110**
T	12.200	12.360	309.9	313.9
U	.137	.153	3.480	3.886

SUGGESTED MOUNTING METHODS FOR PRESS-PAKS TO HEAT DISSIPATORS

When the Press-Pak is assembled to a heat sink in accordance with the following general instructions, a reliable and low thermal interface will result.

1. Check each mating surface for nicks, scratches, flatness and surface finish. The heat dissipator mating surface should be flat within .0005 inch/inch and have a surface fiffish of 63 micro-inches.

2. It is recommended that the heat dissipator mounting surfaces be plated with nickel, tin, or silver. Bare aluminum or copper surfaces will oxidize in time resulting in excessively high thermal resistance.

3. Sand each surface **lightly** with 600 grit paper just prior to assembly. Clean off and apply silicon oil (GE SF1154, 200 centistoke viscosity) or silicone grease (GE G322L or Dow Corning DC 3, 4, 340 or 640). Clean off and apply again as a **thin** film. (A thick film will adversely affect the electrical and thermal resistances.)

4. Assemble with the specified mounting force applied through a self-leveling, swivel connection. The force has to be evenly distributed over the full area. Center holes on both top and bottom of the Press-Pak are for locating purposes only.

HEAT SINK SELECTION MADE EASY

The C441 specification sheet marks the introduction of two new characteristic curves which should greatly facilitate heat sink selection. Figures 5 and 6 plot allowable average current versus ambient temperature and case-to-ambient thermal resistance for the two most frequently encountered waveforms, 1/3 duty cycle rectangular current and 180° sinusoidal current waveforms. As soon as the average forward current and maximum ambient temperature are known, the designer can specify a heat sink thermal resistance. Note that the graphs span the range of heat sinks from water-cooled ($R_{\theta CA}$ = .03°C/W) to free-air convection ($R_{\theta CA}$ = 0.3°C/W). It is possible to linearly interpolate between the curves for $R_{\theta CA}$.

These curves have been derived from the following basic equation:

$$T_J = T_A + P_{AVG} \times R_{\theta JA}$$

where: $T_J = 125°C$

For increased reliability, the usual practice is to derate T_J 15-30 degrees. Figures 5 and 6 can perform this function by the simple expedient of raising T_A by a like amount.