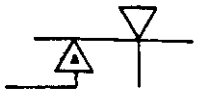
SILICON POWER

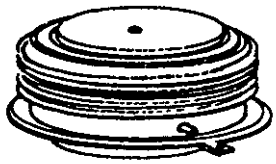
High Power Silicon Controlled Rectifier

C750

1600 A Avg. Up To 1400 Volts AMPLIFYING GATE



The C750 is designed specifically for phase control applications like DC motor control and power supplies, cycloconverters and current regulated inverters.



FEATURES:

- High repetitive di/dt.
- High dv/dt with higher selections available.
- Excellent surge and I^2t current ratings for ease of fusing.
- Rugged hermetic ceramic package with 1" creep and strike.
- Guaranteed turn-off time selections of 100 µsec. available.
- Mounting hardware, water cooled & air cooled assemblies available.

MAXIMUM ALLOWABLE RATINGS

TYPE	REPETITIVE PEAK OFF-STATE VOLTAGE, V_{DRM} T_J = -40°C to +125°C	REPETITIVE PEAK REVERSE VOLTAGE, V_{RRM} T_J = -40°C to +125°C	TRANSIENT PEAK REVERSE VOLTAGE, V_{RSM}[1] T_J = +125°C
C750E1,2	500 Volts	500 Volts	600 Volts
C750M1,2	600	600	700
C750S1,2	700	700	800
C750N1,2	800	800	900
C750T1,2	900	900	1000
C750P1,2	1000	1000	1150
C750PA1,2	1100	1100	1250
C750PB1,2	1200	1200	1400
C750PC1,2	1300	1300	1470
C750PD1,2	1400	1400	1580

[1] Half Sine Wave Waveform, 10 msec. Maximum Pulse Width.

Average Forward Current, On-State (8.3 milliseconds) . . . . . Depends on Conduction Angle (see Charts 1,2,7 and 8)
Peak One-Cycle Surge On-State Current, I_{TSM}, C750-1 . . . . . 28,500 Amperes
C750-2 . . . . . 25,000 Amperes
Maximum Rate-of-Rise of Anode Current Switching from 1000 V . . . . . 400 A/µsec
JEDEC Test
Repetitive di/dt . . . . . 150 A/µsec
I^2t (for fusing) (for times ≥ 1.5 milliseconds) See Figure 20, C750-1 . . . . . 1,250,000 Ampere² Seconds
C750-2 . . . . . 1,050,000 Ampere² Seconds
I^2t (for fusing) (at 8.3 milliseconds) C750-1 . . . . . 3,370,000 Ampere² Seconds
C750-2 . . . . . 2,590,000 Ampere² Seconds
Peak Gate Power Dissipation, P_{GM} . . . . . 200 Watts @ 40 µsec Pulse
Average Gate Power Dissipation, $P_{G(AV)}$ . . . . . 5 Watts
Peak Reverse Gate Voltage, V_{GRM} . . . . . 5 Volts
Storage and Operating Temperature, T_{stg} and T_J . . . . . -40°C to +125°C
Mounting Force Required . . . . . 5,500 Lbs. + 500 – 0
24.5kN + 2.2 – 0

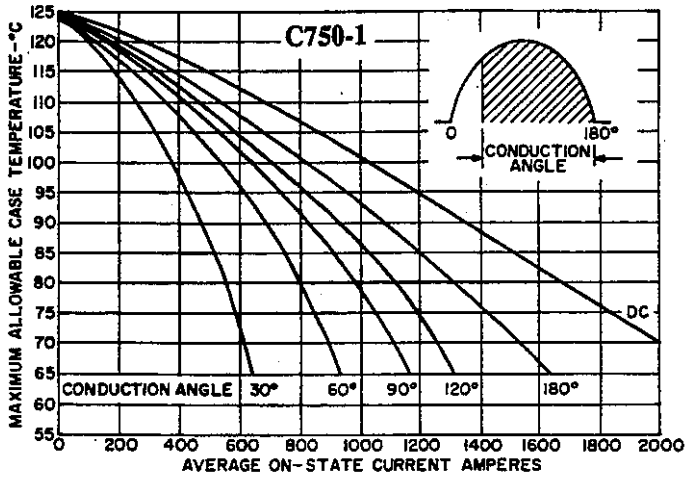
175 Great Valley Pkwy., Malvern, PA 19355, USA

CHARACTERISTICS

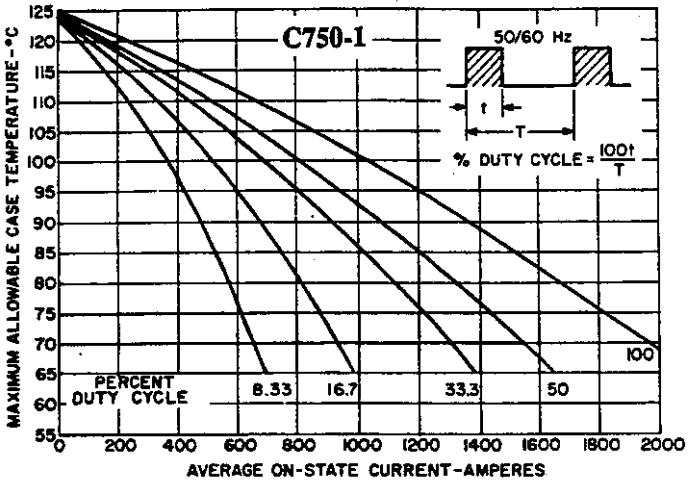
TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Repetitive Peak Off-State and Reverse Blocking Currents	I_{DRM} and I_{RRM}	–	10	20	mA	T_J = +25°C, V = V_{DRM} = V_{RRM}
Repetitive Peak Off-State and Reverse Blocking Currents	I_{DRM} and I_{RRM}	–	35	45	mA	T_J = +125°C, V = V_{DRM} = V_{RRM}
Effective Thermal Resistance (DC)	$R_{\theta JC}$	–	–	.023	°C/Watt	Junction-to-Case – Double-Side Cooling (DC)
Critical Exponential Rate-of-Rise of Forward Blocking Voltage (Higher values may cause device switching.)	dv/dt	400	–	–	V/μsec	T_J = +125°C, Rated V_{DRM}, Gate Open. Contact factory for dv/dt selection of 600, 800 V/μs.
Holding Current	I_H	–	100	500	mAdc	T_J = +25°C, Anode Supply = 24 Vdc., Initial Forward Current = 2 Amps.
Latching Current	I_L	–	1	–	Adc	T_J = +25°C, Anode Voltage = 24 Vdc., Load Resistance 12 ohms max.
Delay Time	t_d	–	0.7	–	μsec	T_J = +25°C, I_T = 50 Adc. Gate Supply: 20 Volts, 20 Ohms, 0.1 μsec max. rise time.
Gate Pulse Width Necessary to Trigger		–	–	10	μsec	T_J = +25°C. Gate Supply: 10 Volt Open Circuit, 5 Ohms, 0.1 μsec. rise time.
Gate Trigger Current. See Figure 19, for Recommended Gate Drive Conditions.	I_{GT}	30	–	200	mAdc	T_J = +25°C, V_D = 20V, R_L = 3 Ohms
		–	–	300		T_J = -40°C, V_D = 20V, R_L = 3 Ohms
		–	–	125		T_J = +125°C, V_D = 20V, R_L = 3 Ohms
Gate Trigger Voltage. See Figure 19	V_{GT}	–	–	5	Vdc	T_J = -40°C to +125°C, V_D = 20 Vdc, R_L = 3 Ohms
		.15	–	–		T_J = +125°C, V_D = Rated V_{DRM}, R_L = 1000 Ohms
Peak On-State Voltage C750-1 C750-2	V_{TM}	–	–	– 1.4 1.65	Volts	T_J = +25°C, I_T = 3,000 Amps Peak. Duty Cycle ≤ 0.01%. Pulse Width = 8.3mS.
Circuited Commutated Turn-Off Time	t_q*	–	150	–	μsec	(1) T_J = +125°C (2) I_T = 2000 Amps, Pulse Width = 1000μsec. (3) V_R = 50 Volts Minimum (4) V_{DRM} (Reapplied) (5) Rate-of-rise of reapplied forward blocking voltage = 200V/μsec (linear). (6) Commutation di/dt = 25 Amps/μsec. (7) Repetition rate = 1 pps. (8) Gate bias during turn-off interval = 0 volts, 100 ohms.

NOTE: T_C = Case Temperature

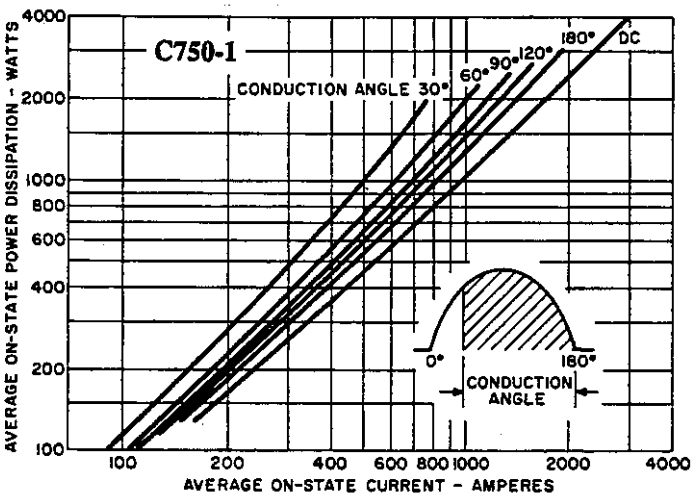
*Contact factory for maximum t_q specification.



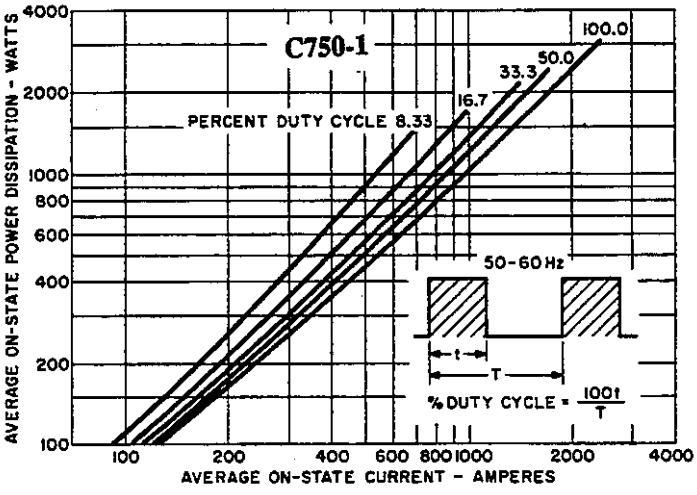
1. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM – DOUBLE-SIDE COOLED



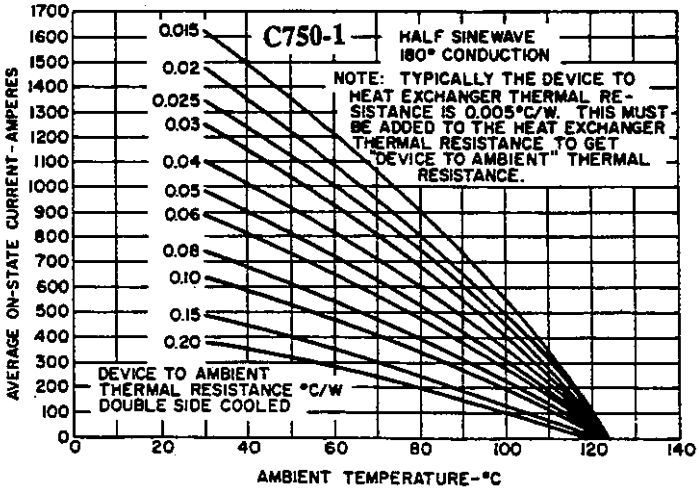
2. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM – DOUBLE-SIDE COOLED



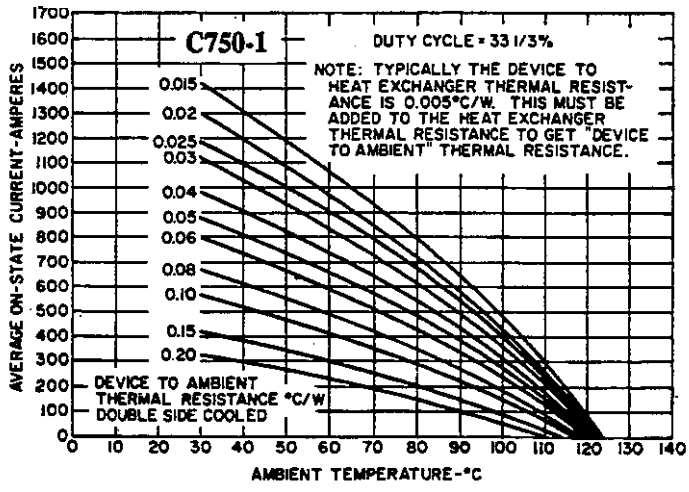
3. AVERAGE ON-STATE POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



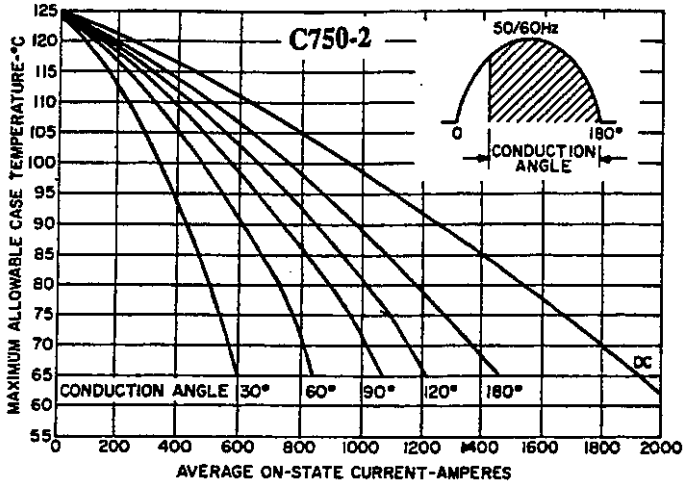
4. AVERAGE ON-STATE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



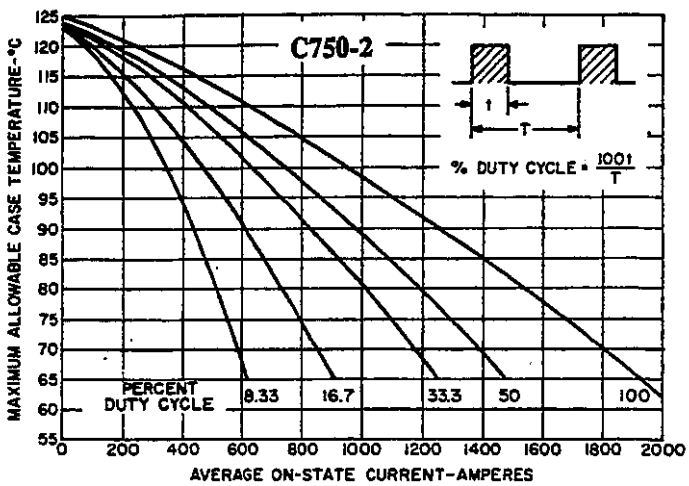
5. AVERAGE HALF SINEWAVE ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



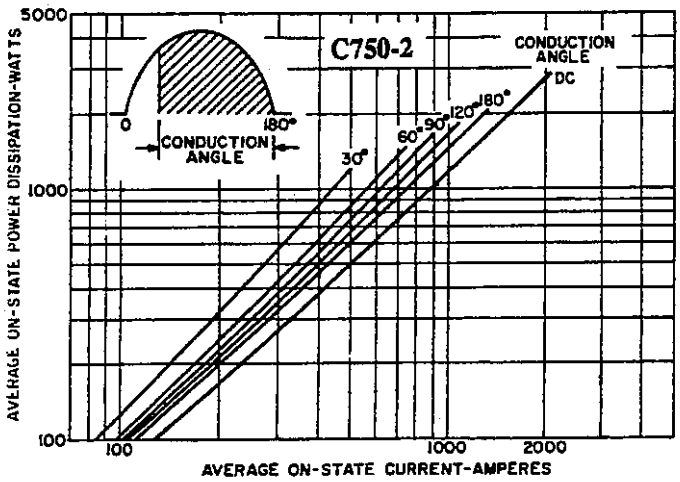
6. AVERAGE RECTANGULAR ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



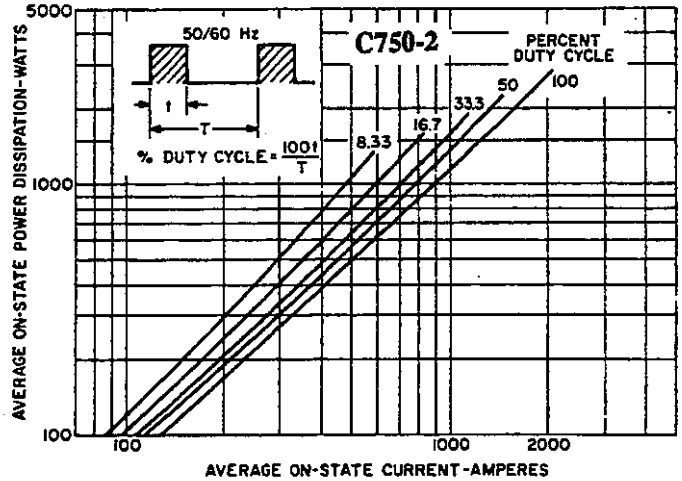
7. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR SINUSOIDAL CURRENT WAVEFORM – DOUBLE-SIDE COOLED



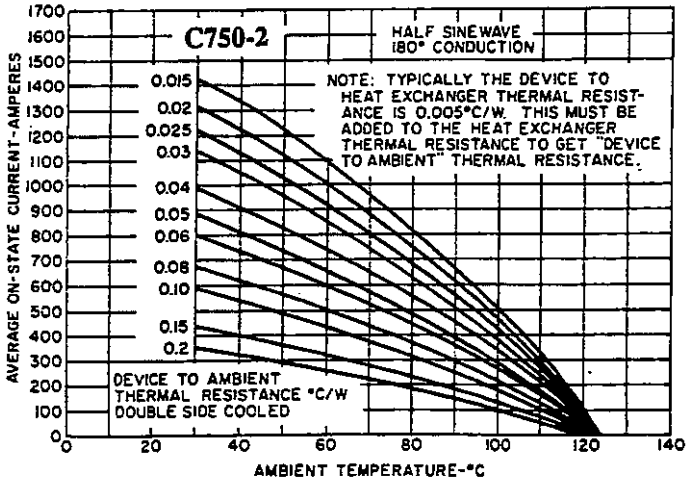
8. MAXIMUM ALLOWABLE CASE TEMPERATURE FOR RECTANGULAR CURRENT WAVEFORM DOUBLE-SIDE COOLED



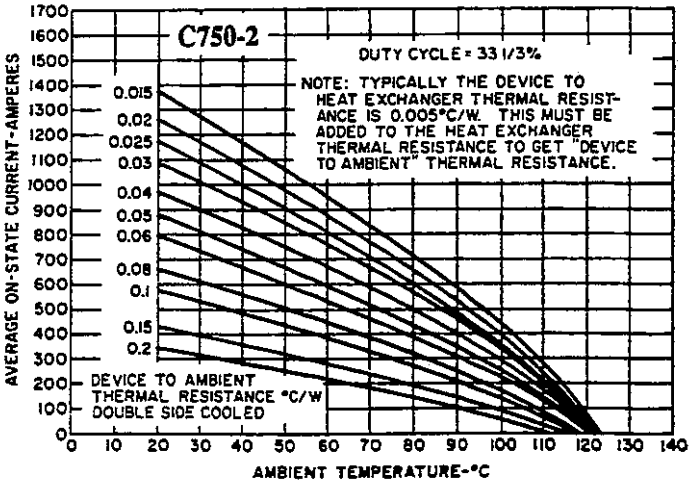
9. AVERAGE ON-STATE POWER DISSIPATION FOR SINUSOIDAL CURRENT WAVEFORM



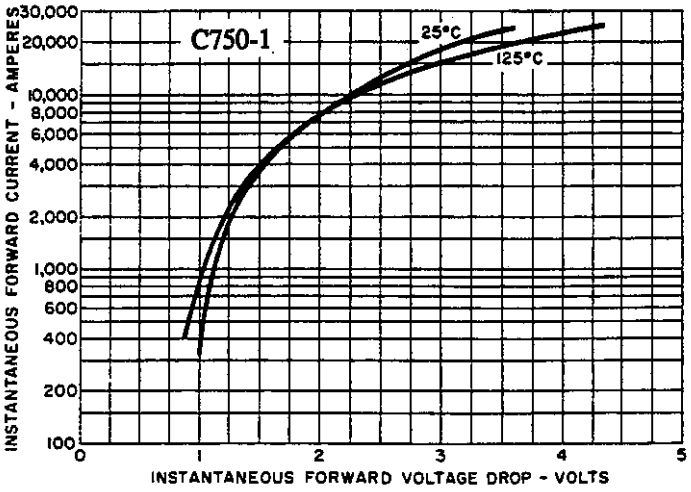
10. AVERAGE ON-STATE POWER DISSIPATION FOR RECTANGULAR CURRENT WAVEFORM



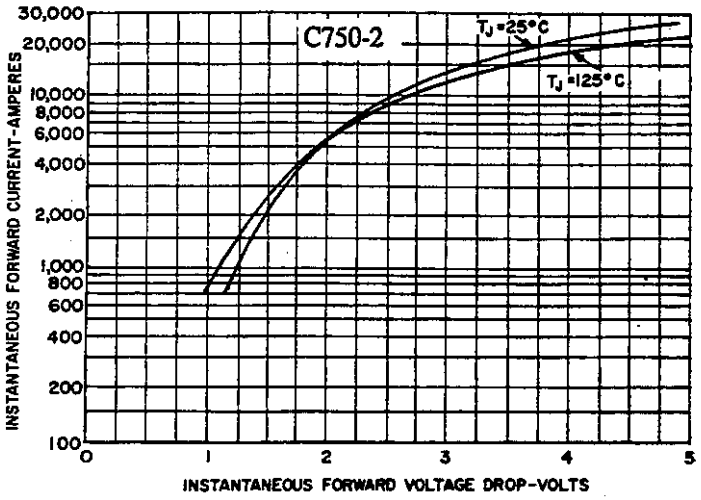
11. AVERAGE HALF SINEWAVE ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



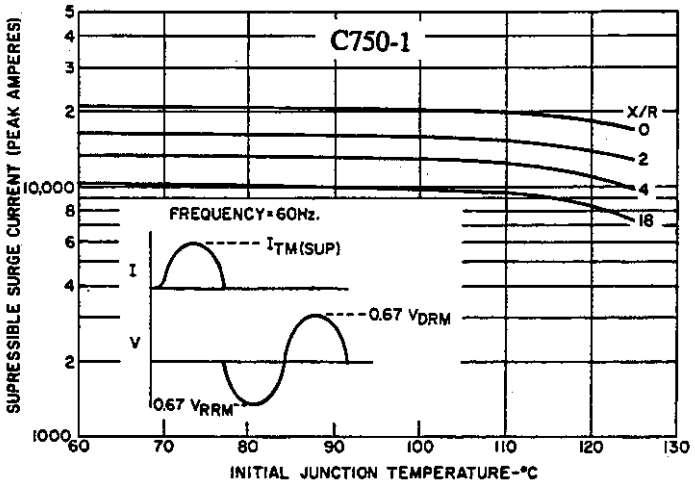
12. AVERAGE RECTANGULAR ON-STATE CURRENT VS. AMBIENT TEMPERATURE WHEN USED WITH VARIOUS HEAT EXCHANGERS



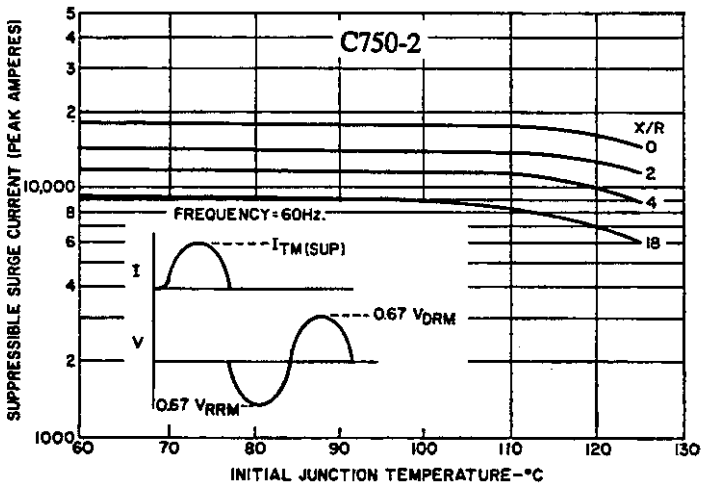
13. MAXIMUM ON-STATE CHARACTERISTICS



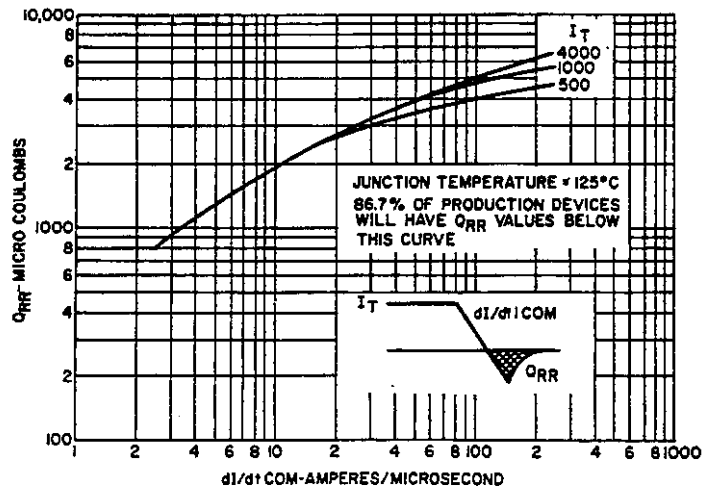
14. MAXIMUM ON-STATE CHARACTERISTICS



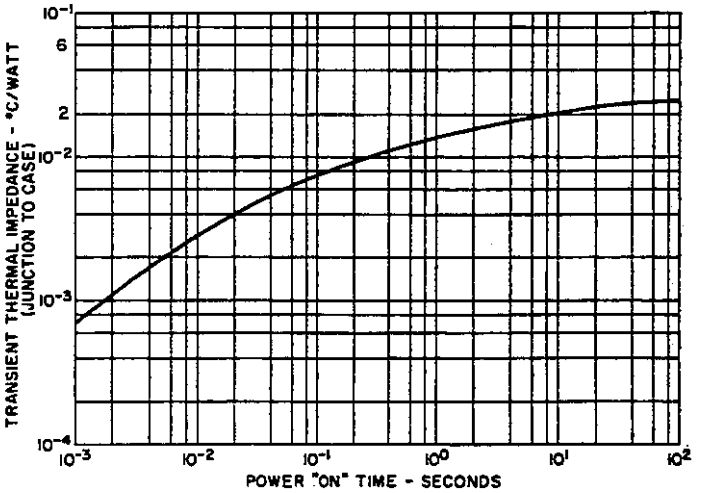
15. SURGE SUPPRESSION RATING



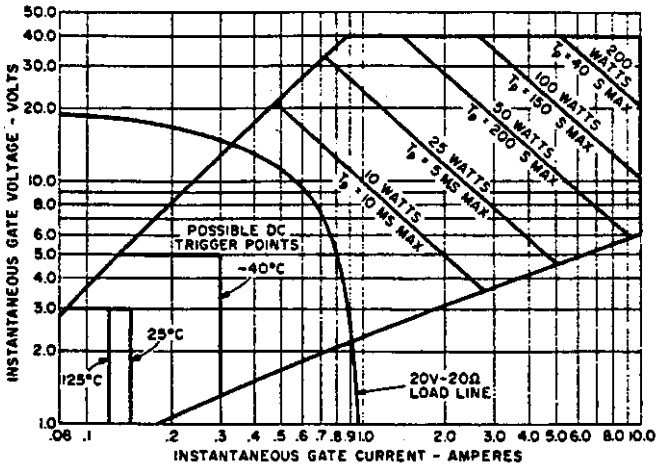
16. SURGE SUPPRESSION RATING



17. TYPICAL REVERSE RECOVERY CHARGE AT T_j = 125° C



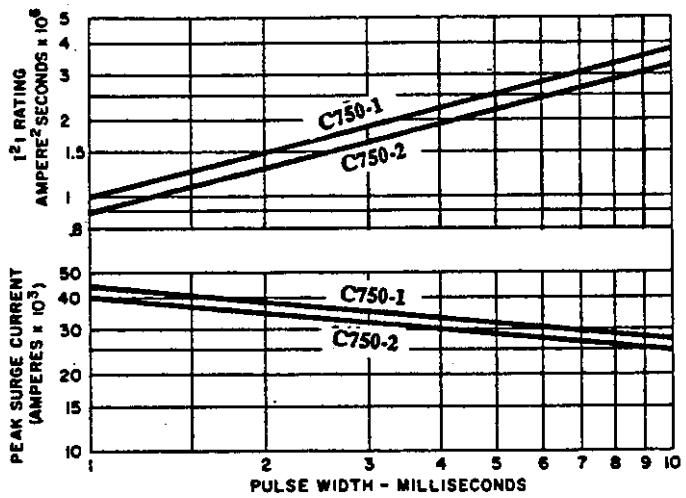
18. TRANSIENT THERMAL IMPEDANCE – JUNCTION-TO-CASE (DOUBLE-SIDE COOLED)



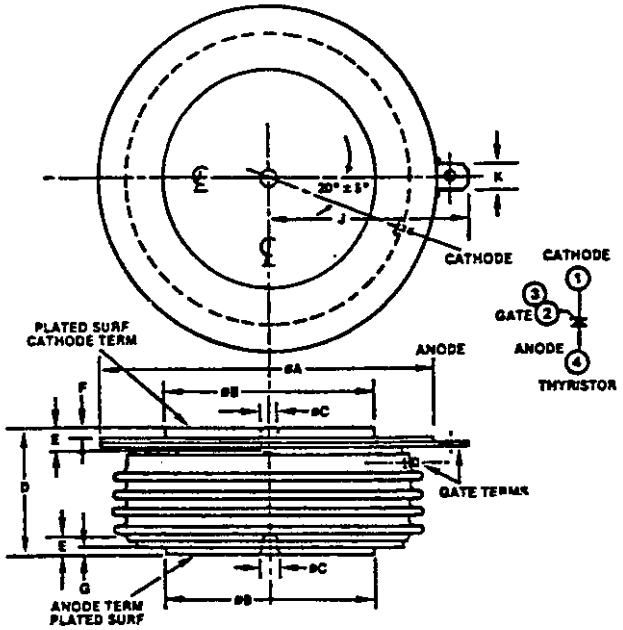
NOTES:

1. Maximum allowable average gate dissipation = 5 watts.
2. The locus of possible DC trigger points lies outside the boundaries shown at various case temperatures.
3. Tp = rectangular gate current pulse width (5μs min. duration, 1.0μs max. rise time).
4. Maximum long-term, repetitive anode di/dt = 400 Amps/μs with 20V – 20Ω gate source.

19. GATE TRIGGERING CHARACTERISITCS



20. I^2T AND I_{TSM} FOLLOWING RATED LOAD CONDITIONS



SYMBOL	INCHES		MILLMETERS	
	MIN.	MAX.	MIN.	MAX
øA	—	2.960	—	75.18
øB	1.800	1.900	45.72	48.26
øC	0.136	0.146	3.45	3.71
D	1.000	1.070	25.40	27.18
E	.070	0.1000	1.78	2.54
F	.030	—	1.78	2.54
G	.005	.057	0.13	1.70
H	—	—	—	—
J	1.680	1.710	42.67	43.43
K	.186	.189	4.72	4.80

Anode-Cathode Pole Faces (4)(1) Nickel Plated Copper.
Mating Surface Requirement TIR≤.0005 inch Finish 32.
Mounting Force, 5000-6000 Lb., 22.4-26.7 KN.
Electrical Insulation, Glazed Ceramic, Creepage 1 in. (25.4mm). Strike 5/8 in. (15.9mm)
Gate Leads (2)(3) 18 in. #22 Terminated with #8 Ring Terminal, Cathode Wire-Red, gate Wire-White.