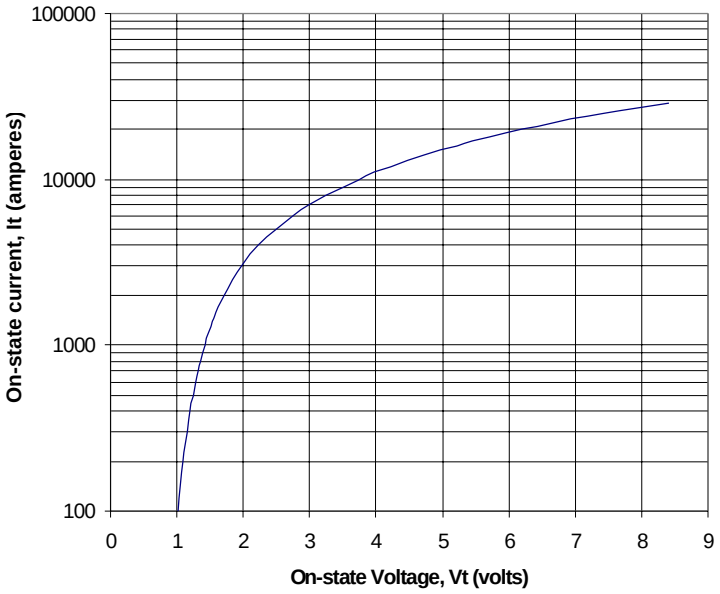
C783
77mm / 3800V THYRISTOR

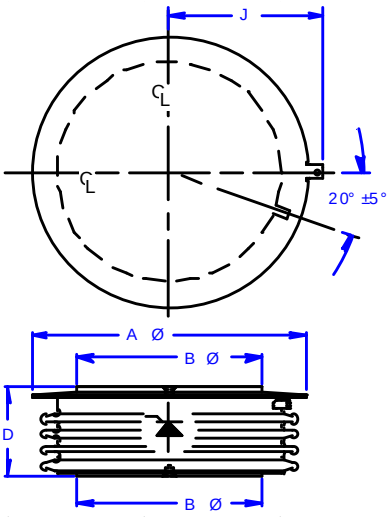
Type C783 reverse blocking thyristor features a 77mm silicon junction design having the exclusive linear amplifying type gate manufactured by the proven multi-diffused process.

It is supplied as a Presspak ready to mount using commercially available heat dissipators or factory-certified, double-sided, cooled assemblies.

ON-STATE CHARACTERISTIC



MECHANICAL OUTLINE



AF = 4.35 in (110.5 mm)
BF = 2.88 in (73.2 mm)
D= 1.45 in (36.8 mm)

PRINCIPAL RATINGS AND CHARACTERISTICS

OPERATING JUNCTION TEMPERATURE RANGE
-40 to +125°C

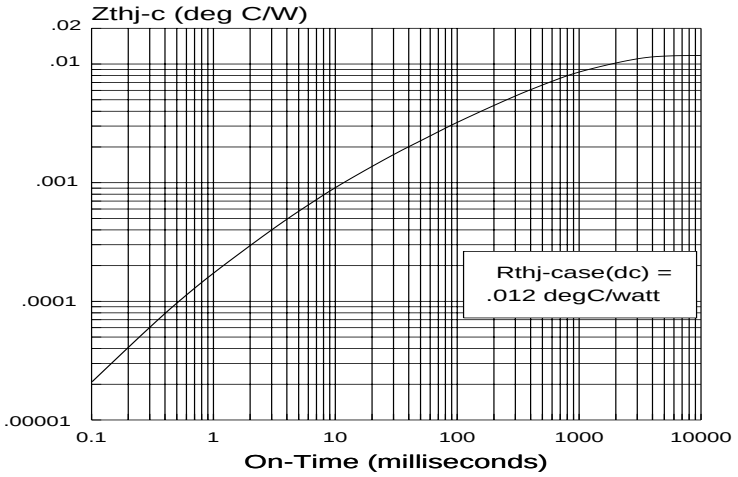
. Repetitive peak off-state and reverse voltage	V_{DRM} V_{RRM}	to 3800V
. Average on-state current @T_C=70°C	$I_{T(AV)}$	1800A
. Peak half cycle surge current for Vr = 0 V	I_{TSM}	8.3 ms / 10.0 ms 29 kA / 27 kA
. On-state Voltage @I_T=2000A, 125°C	V_{TM}	1.71V
. Critical rate of rise of current @V_D=2000V	di/dt	100A/us
. Critical rate of rise of off-state voltage	dv/dt	500V/us to 0.8V_{DRM}
. Max peak recovery current @ Tj = 125°C	I_{RM}	2A/us / 10A/us 66A / 250A
. Circuit commutated turn-off time (typ)	t_q	300us

Model No.	V_{DRM} /V_{RRM} -40°C	0 to +125°C
C783CS	3700 V	3800 V
C783CM	3600	3700
C783CE	3500	3600
C783CD	3400	3500
C783CC	3300	3400
C783CB	3200	3300

GATE DRIVE REQUIREMENTS
Open circuit voltage / short circuit current 30V / 3A
Short circuit risetime 0.5us
Minimum pulse duration 10us

EXTERNALLY REQUIRED CLAMPING FORCE
8000 - 9000 lbs. / 35.6 - 40.0 kN

THERMAL IMPEDANCE vs. ON-TIME



SILICON POWER CORPORATION
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TEST	SYMBOL	MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
Peak Reserse and off-state blocking current	I_{DRM} I_{RRM}			10 100	mA mA	V = V_{DRM} = V_{RRM} T_J = 25°C T_J = 125°C
Effective thermal resistance, junction to case - double-sided cooling	$R_{\Theta JC}$ DC	-	-	0.012	°C/W	Double-sided cooling - (add 0.002 °C/W for interfaces case to sink)
Critical exponential rate of rise of forward blocking voltage (higher values may cause destructive switching)	dv/dt	500 1500			V/µs V/µs	T_J = +125°C; V_{DM} = 0.8V_{DRM} - open gate standard selection - open gate special selection
Delay time	t_d		3 4	3.5 5	µs	Gate source 30V / 10Ω rise time 0.5µs; T_J = 25-125°C - Bias V_{DM} = 1800V - Bias V_{DM} = 500V
Gate pulse amplitude (operational)						- T_C = 40 to +125°C - Gate source voltage 30 - 40V - Gate source imdedance ~10Ω - Current rise time ~ 0.5µs
Gate pulse width (operational)				10	µs	See triggering characteristics
DC gate trigger current (non-operational *)	I_{GT}	20		300	mAdc	- T_C=25°C, V_D=10Vdc, R_L=3Ω - T_C=125°C, V_D=0.5V_{DRM}, R_L=1kΩ
DC gate trigger voltage (non-operational *)	V_{GT}	0.5		4.5	Vdc	- T_C=25°C, V_D=10Vdc - T_C=125°C, V_D=0.5V_{DRM}, R_L=1kΩ
Peak on-state voltage	V_{TM}		- -	1.71 1.93	V	I_T = 2000A duty cycle <= 0.01% - T_C=125°C - T_C=25°C
Suppressible surge current	$I_{TM(sup)}$		24 22		kA	- 60Hz T_C = 115°C - 50Hz resistive circuit sinusoidal blocking voltage applied after completion of surge 0.5V_{RRM} 0.5V_{DRM}
Circuit commutated turn-off time	t_q	-	200	300	µs	T_C = 125°C, I_{TM} = 500A - Commutating di/dt = 25A/µs - Min. reverse voltage V_R = 50V - Reapplied off state voltage 20V/µs to 0.8V_{DRM} - Gate bias during turn-off interval zero volts/100
* characteristic only, di/dt rating does not apply.						