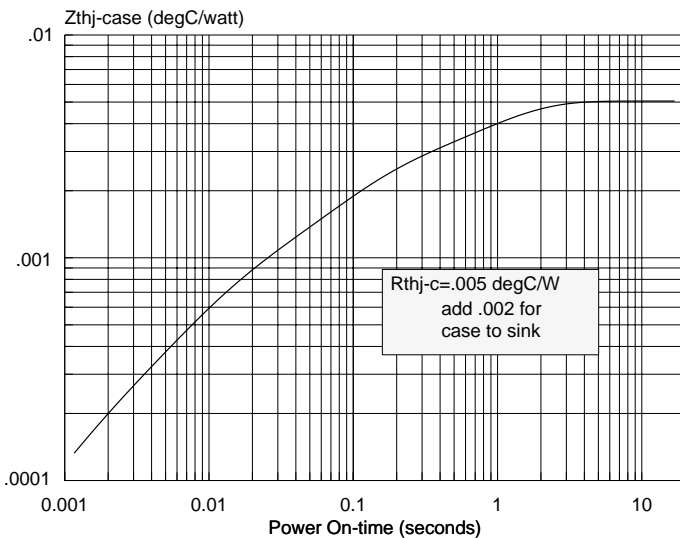
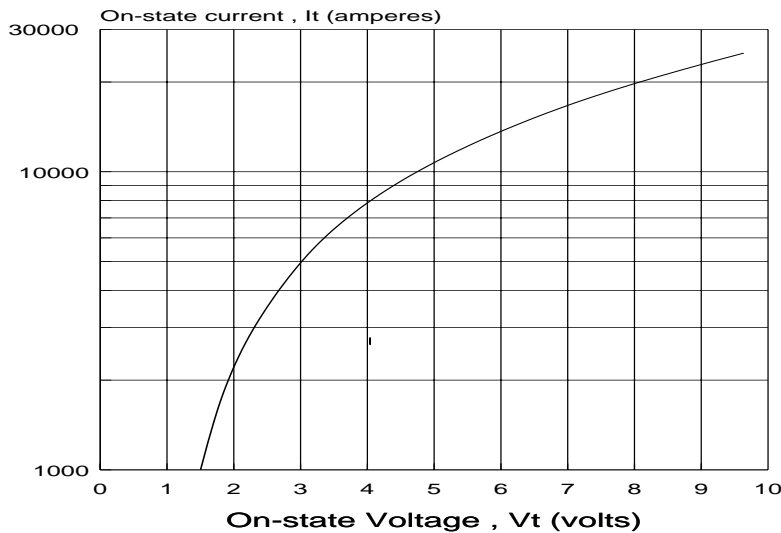


Type C792 thyristor is suitable for phase control applications such as for HVDC valves, static VAR compensators and synchronous motor drives. The silicon junction design utilizes a second generation pilot gate and a unique orientation of emitter shorts which promote the lateral expansion of conducting plasma resulting in lower spreading losses while achieving high dv/dt withstand. It is supplied in an industry accepted disc-type package, ready to mount using commercially available heat dissipators and mechanical clamping hardware.

**MAXIMUM ON-STATE CHARACTERISTIC**  
Initial TJ=105 degC / 8ms pulse



o1a:t305tau

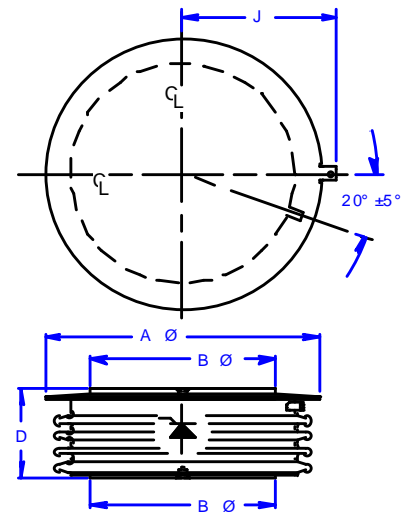
175 GREAT VALLEY PKWY. MALVERN, PA 19355  
USA

REPETITIVE PEAK REVERSE  
AND OFF-STATE BLOCKING

VOLTAGE  
 $T_j = 0 \text{ to } 115^\circ\text{C}$

MODEL	$V_{DRM}$ (volts)	$V_{RRM}$ (volts)
C792FP	6000	6000
C792ET	5900	5900
C792EN	5800	5800
C792ES	5700	5700
C792EM	5600	5600
C792EE	5500	5500

MECHANICAL OUTLINE



AF = 5.65 in (143.5 mm)  
BF = 3.92 in (99.4 mm)  
D = 1.45 in (36.8 mm)

ELECTRICAL  
CREEPAGE / STRIKE  
1.6 / 1.0 in  
40.6 / 25.4 mm  
CLAMPING FORCE  
(range)  
17000-19000 lb.

## LIMITING CHARACTERISTICS AND RATINGS

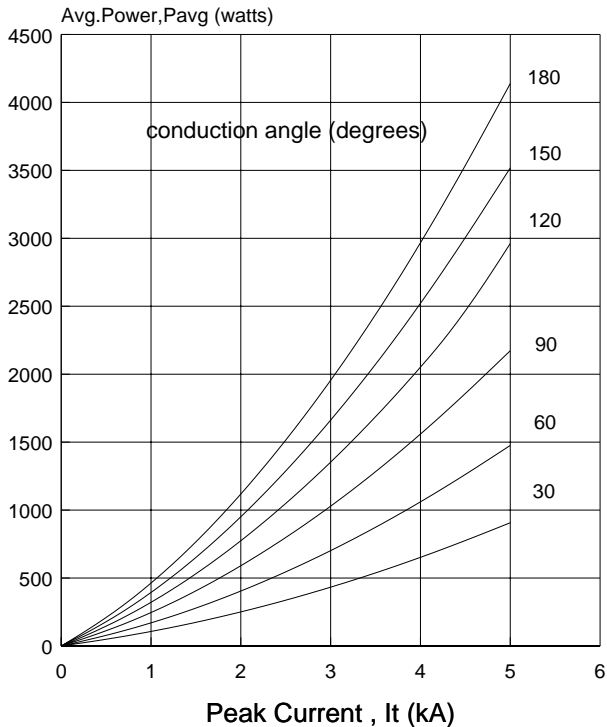
PARAMETER	SYMBOL	TEST CONDITIONS	MAXIMUM VALUES	UNIT S
Repetitive peak off-state and reverse voltage	$V_{DRM}$ $V_{RRM}$	$T_j=0$ to $+115^\circ\text{C}$	see table	V
Repetitive working crest voltage	$V_{DWM}$ $V_{DRM}$	$T_j=0$ to $115^\circ\text{C}$	.8V <sub>DRM</sub> .8V <sub>RRM</sub>	V
Rep. off-state and reverse leakage current	$I_{DWM}$ $I_{RRM}$	$V_{DWM}$ $V_{RRM}$ $T_j=115^\circ\text{C}$	150 150	ma ma
On-state Voltage	$V_{TM}$	$I_T=2000\text{A}$ $t_p=8.3\text{ms}$ $T_j=115^\circ\text{C}$	1.90	V
Critical DC gate current/voltage to trigger on	$I_{GT}$ $V_{GT}$	$V_D=12\text{VDC}$ $T_j=25^\circ\text{C}$	150 3	ma V
Non-trigger gate current/voltage	$I_{GD}$ $V_{GD}$	$V_D=.8\text{V}_{DRM}$ $T_j=115^\circ\text{C}$	8 —	ma V
Critical rate of rise of off-state	$dv/dt$	$0.67V_{DRM}$ $T_j=115^\circ\text{C}$	2000	V/us
Critical rate of of on-state	$di/dt_{rep}$	$0.67 V_{DRM}$ see req'd gating	100	A/us
Peak recovery current	$I_{RM(rec)}$	$di/dt=2\text{A/us}$ $T_j=115^\circ\text{C}$	118	A
Peak half-cycle non-repetitive surge current	$I_{TSM}$	$t_p=8.3\text{ms}$ $t_p=10\text{ms}$	35 34	kA
Circuit commutated turn-off time	$t_q$	$di/dt=5\text{A/us}$ $dv/dt=20\text{V/us}$	600	us

### GATE CIRCUIT REQUIREMENTS

Open circuit voltage	40 - 50 V
Short circuit current	3 A minimum
Current risetime	0.5 us nominal
Pulse duration	10-20 us

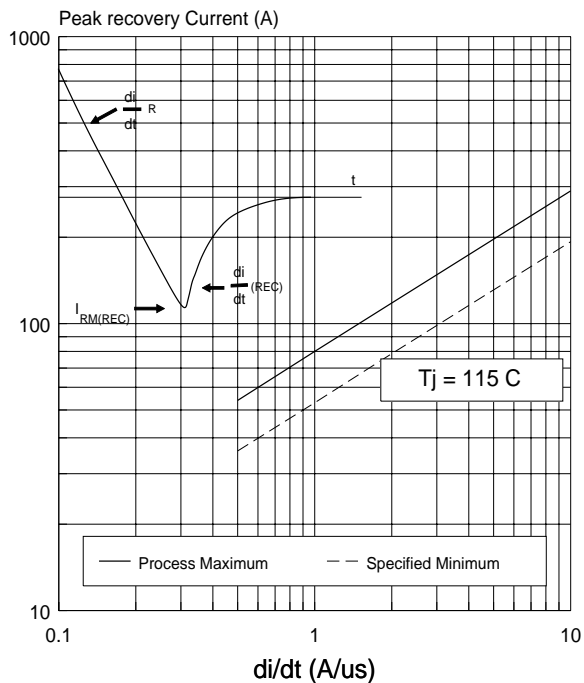
# C792 / 6RT300

FULL CYCLE AVERAGE POWER DISSIPATION  
Sine Wave-includes spread loss

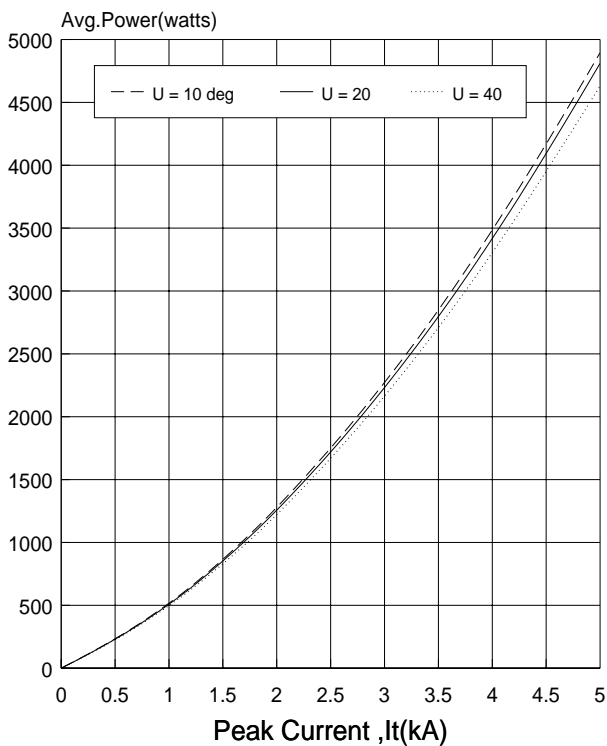


6RT300

PEAK RECOVERY CURRENT  
versus  
COMMUTATING di/dt

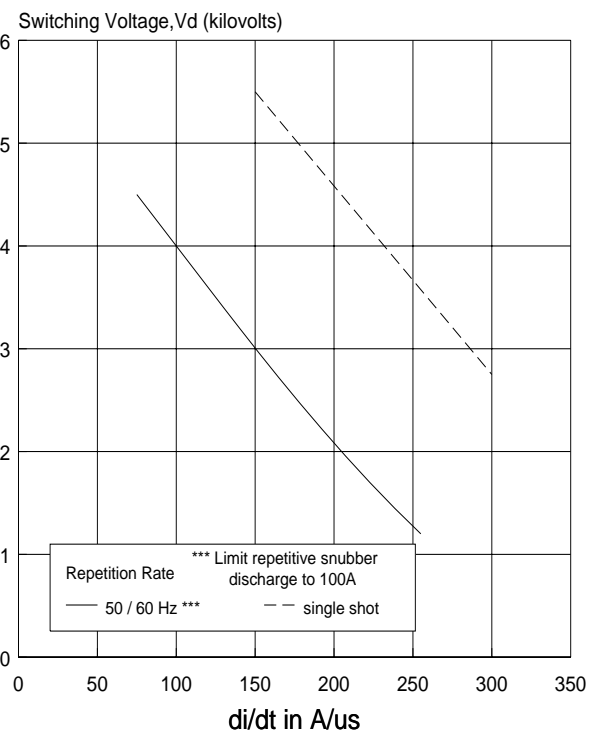


FULL CYCLE AVERAGE POWER DISSIPATION  
120-Deg Conduction-includes spread loss  
as a function of overlap angle, U



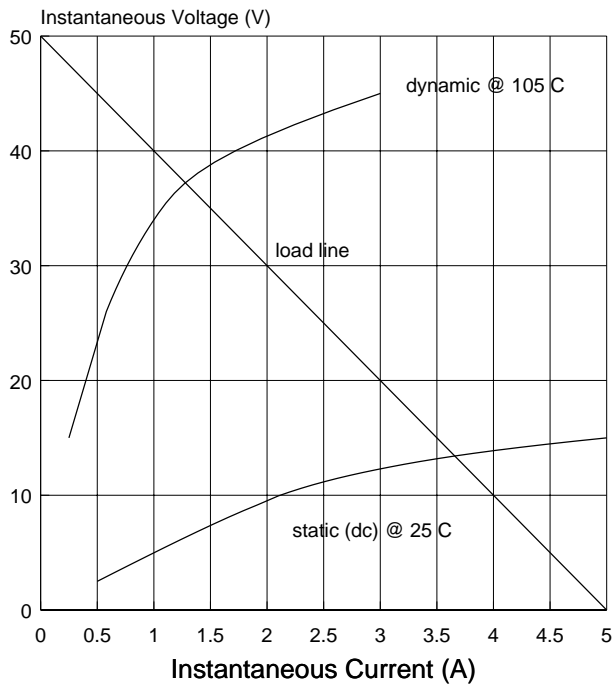
6RT300

INRUSH CURRENT (di/dt) RATING  
versus  
SWITCHING VOLTAGE



T300

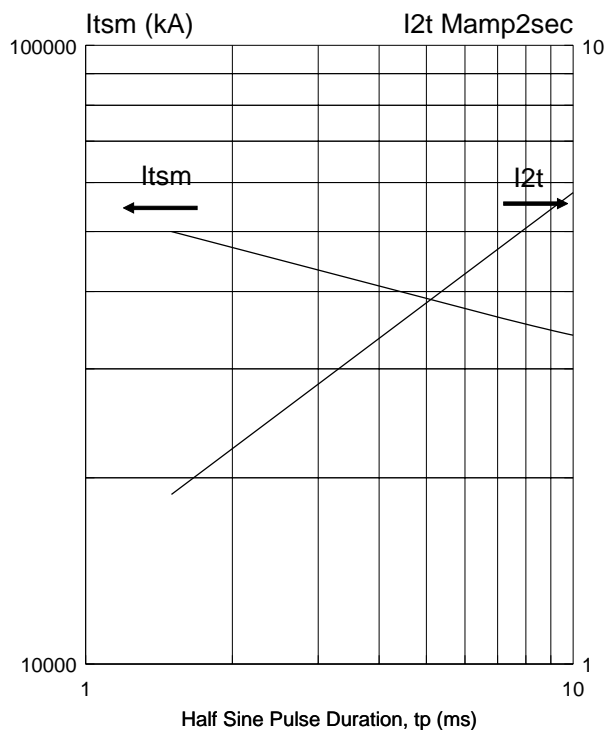
## Gate Characteristics and Gate Supply Requirements



- THYRISTOR GATE IMPEDANCE**  
 Enhanced by fast rising gate voltage, increasing anode bias and junction temperature. It is at a minimum for dc current, zero anode bias and low temperature.
- GATE SUPPLY**  
 Prefer 50V/10 ohm for supporting the di/dt rating and life expectancy. The short circuit current risetime should be nominally 0.5us and the duration longer than the expected delay time for all magnitudes of anode bias. Practically 10-30us is recommended followed by a back porch of 750ma if needed to sustain conduction.
- MINIMUM ACCEPTABLE GATE CURRENT**  
 The intersection of the load line and gate impedance characteristic indicates the minimum value of actual current needed during the delay time interval to support di/dt. A different load line meeting this criterion may be used.
- MAXIMUM GATE RATINGS**  
 Peak gate power,  $P_{gm}(100\mu s) = 300 W$   
 Average gate power,  $P_{g(av)} = 50W$   
 Peak gate current,  $I_{gfm} = 25 A$   
 Peak reverse voltage,  $V_{grm} = 25 V$

T302

## Non-Repetitive Surge Current and I2t for Fusing



01:C792ITSM