Reset Timer IC for Mobile Equipments

NO.EA-280-130423

OUTLINE

The R3200x Series are reset timer ICs with two input signals for mobile equipments which require long interval for reset sequence. The long interval prevents unexpected resets caused by accidental key operations. Internally, each of these ICs consist of a delay generator circuit and output driver transistors.

The R3200x Series have two active-low input pins ($\overline{SR0}$ and $\overline{SR1}$) which generate reset signals after output delay time when both input pins are activated at the same time.

R3200x Series has two versions that are different in output delay time settings and output release method.

- R3200x001x:
  Output delay time selectable (7.5s or 11.25s) by connecting DSR pin to either GND or V_{DD}. The reset signal will be canceled if either of the input pin becomes “H”. Until either input pin becomes “H”, the reset signal will be continually outputted.
- R3200xxx2x or R3200L053B:
  Output delay time is fixed. After the reset signal is being output, it will be released automatically or if either of the input pin becomes “H”, the reset signal will be canceled.

While the reset signals are remaining active or being sent out, the ICs provide ultra-low supply current.

The R3200x Series are available in DFN(PLP)2020-8B and DFN1216-8 packages.

FEATURES

- Supply Current 1 (at standby) ..... Typ. 0.28μA (V_{DD} = 5.5V)
- Supply Current 2 (at active before reset signal output) ... Typ. 3μA (V_{DD} = 5.5V)[*1]
- Supply Current 3 (at active after reset signal output) ..... Typ. 0.45μA (V_{DD} = 5.5V)
- Operating Voltage Range ..... 1.65V to 5.5V (Ta = 25ºC)
- Operating Temperature Range ..... -40 to +85ºC
- Output Delay Time (R3200x001x) ..... Typ. 7.5s or 11.25s
  (R3200x002x) ..... Typ. 7.5s
  (R3200L052B) ..... Typ. 10s
  (R3200L053B) ..... Typ. 10s
- Output Delay Time Accuracy ..... ±20%
- Output Release Time (R3200x002x) ..... Typ. 0.234s
  (R3200L052B) ..... Typ. 0.313s
  (R3200L053B) ..... Typ. 0.078s
- Output Release Time Accuracy (R3200xxx2x) ..... ±20%
- Output Types ..... Nch Open Drain and CMOS
- Packages ..... DFN(PLP)2020-8B, DFN1216-8

[*1] Guaranteed by Design Engineering

APPLICATIONS

- Mobile phone, Smartphone
- E-book, Tablet devices
- Portable Games
- Personal Navigation Devices

BLOCK DIAGRAMS

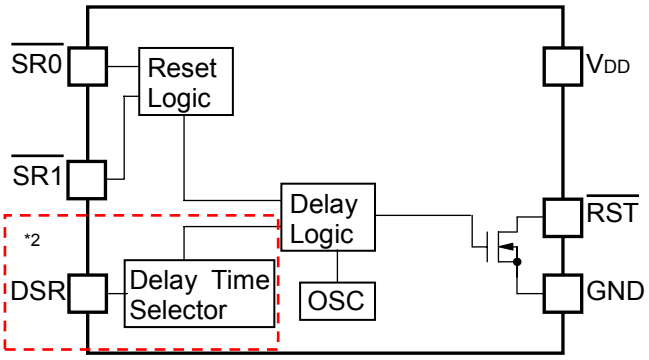


Figure 1. R3200xxxxA

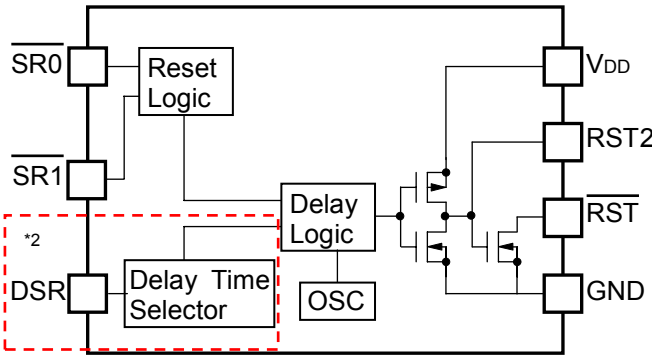


Figure 2. R3200xxxxB

*2 The parts surrounded by red dotted lines apply only to the R3200x001x.

SELECTION GUIDE

The package type, the taping type and the output type for the ICs are user-selectable options.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R3200Kxxx∗-TR	DFN(PLP)2020-8B	5,000 pcs	Yes	Yes
R3200Lxxx∗-E2	DFN1216-8	5,000 pcs	Yes	Yes

xxx: The combination of output delay time settings and output release method can be designated by numbers.

(001) The output delay time of the reset signals selectable from 7.5s or 11.25s.
The reset signal will be canceled if either of the input pin becomes “H”.
Until either input pin becomes “H”, the reset signal will be continually outputted.

(xx2) / (053)
The output delay time of the reset signals is fixed. After reset signal is being output, it will be released automatically or if either of the input pin becomes “H”, the reset signal will be canceled.
For the output delay time and released time of the reset signals, please refer to the following table.

	Output Delay Time	Released Time
002	7.5s	0.234s
052 (R3200L052B only)	10s	0.313s
053 (R3200L053B only)	10s	0.078s

∗: Designation of Output Type
(A) Nch Open Drain
(B) Nch Open Drain and CMOS

PIN CONFIGURATIONS

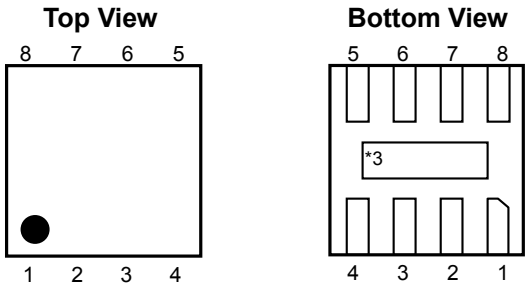


Figure 3. DFN(PLP)2020-8B

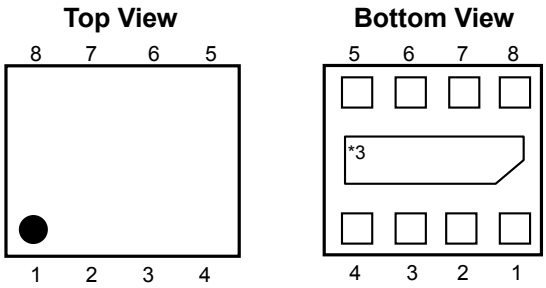


Figure 4. DFN1216-8

*3 Tab is GND level. (They are connected to the reverse side of this IC.) The tab must be connected to the GND pin or left open.

PIN DESCRIPTIONS

R3200K: DFN(PLP)2020-8B/ R3200L: DFN1216-8

Pin No.	Symbol	Description
1	NC	No Connection (R3200xxxxA)
	RST2	CMOS Output Pin, "H" Active (R3200xxxxB)
2	GND	Ground Pin
3	$\overline{SR1}$	2nd Reset Input Pin, "L" Active*4
4	$\overline{RST}$	Nch Open Drain Output Pin, "L" Active*5
5	DSR	Output Delay Time Selection Pin (R3200x001x) (GND: 7.5s, V_{DD}: 11.25s)*6
	TEST2	Test Pin*7 (R3200xxx2x)
6	TEST	Test Pin*7
7	$\overline{SR0}$	1st Reset Input Pin, "L" Active*4
8	V_{DD}	Power Supply Input Pin

*4 In the case of using either the $\overline{SR0}$ or $\overline{SR1}$ pin, the other pin which is not using must be connected to GND.
*5 In the case of not using the $\overline{RST}$ pin such as with R3200xxxxB, $\overline{RST}$ pin must be connected to GND or left open.
*6 DSR pin must be conected to either GND or V_{DD}.
*7 The TEST pin and the TEST2 pin must be connected to GND.
Tab is GND level. (They are connected to the reverse side of this IC.) The tab must be connected to the GND pin or left open.

ABSOLUTE MAXIMUM RATINGS

Symbol	Item	Rating		Unit
V_{DD}	Supply Voltage	GND-0.3 to 6		V
V_{SR0}	Input Voltage (1st Reset Input Pin)	GND-0.3 to 6		V
V_{SR1}	Input Voltage (2nd Reset Input Pin)	GND-0.3 to 6		V
V_{RST}	Output Voltage (1st Reset Output Pin)	GND-0.3 to 6		V
V_{RST2}	Output Voltage (2nd Reset Output Pin)	GND-0.3 to V_{DD}+0.3		V
V_{DSR}	Input Voltage (Output Delay Time Selection Pin) (R3200x001x)	GND-0.3 to 6		V
I_{OUT}	Output Current	20		mA
P_D	Power Dissipation (Standard Land Pattern)[*8]	DFN(PLP)2020-8B	880	mW
		DFN1216-8	625	
Topt	Operating Temperature Range	-40 to +85		°C
Tstg	Storage Temperature Range	-55 to +125		°C

[*8] For more information about Power Dissipation and Standard Land Pattern, please refer to the next page.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

POWER DISSIPATION (DFN(PLP)2020-8B)

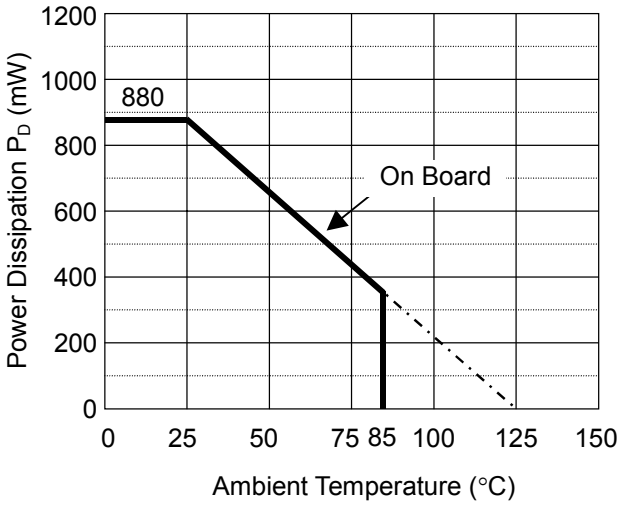
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

Measurement Conditions

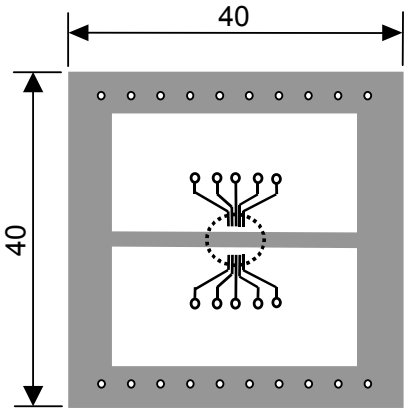
	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mmx40mmx1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.54mm x 30pcs

Measurement Result: (Ta=25°C, Tjmax=125°C)

	Standard Land Pattern
Power Dissipation	880mW
Thermal Resistance	θja = (125-25°C)/0.88W = 114°C/W
	θjc = 22.8°C/W



Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit : mm)

POWER DISSIPATION (DFN1216-8)

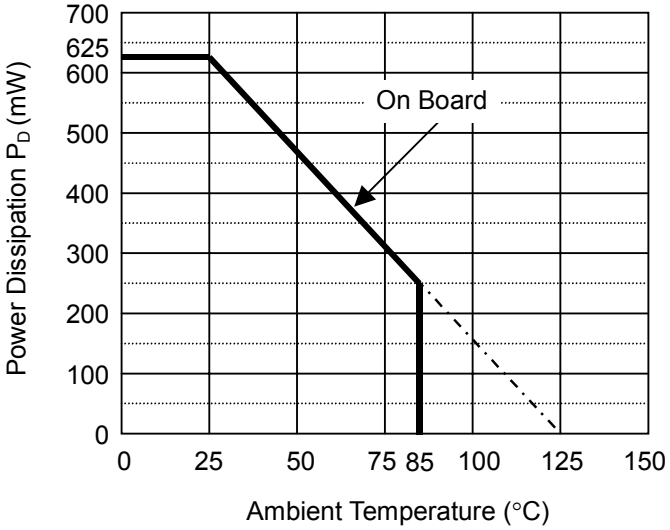
Power Dissipation (P_D) depends on conditions of mounting on board. This specification is based on the measurement at the condition below:

Measurement Conditions

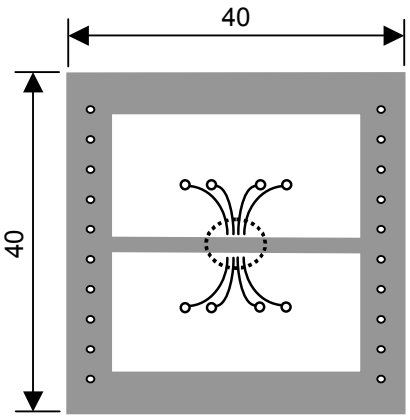
	Standard Land Pattern
Environment	Mounting on Board (Wind velocity=0m/s)
Board Material	Glass cloth epoxy plastic (Double sided)
Board Dimensions	40mm*40mm*1.6mm
Copper Ratio	Top side: Approx. 50%, Back side: Approx. 50%
Through-holes	ϕ 0.5mm * 28pcs

Measurement Result (Ta=25°C, Tjmax=125°C)

	Standard Land Pattern
Power Dissipation	625mW
Thermal Resistance	θja = (125-25°C)/0.625W = 160°C/W
	θjc = 26 °C/W



Power Dissipation



Measurement Board Pattern

IC Mount Area (Unit : mm)

ELECTRICAL CHARACTERISTICS

The specifications surrounded by ☐ are guaranteed by Design Engineering at −40°C ≤ Ta ≤ 85°C.

R3200x001x (Ta=25°C)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage			1.65		5.5	V
I_{SS1}	Supply Current 1*9	V_{DD} = 5.5V (at standby)			0.28	1.35	μA
I_{SS2}	Supply Current 2*10	V_{DD} = 5.5V (at active before reset signal output)			3.0	6.5	μA
I_{SS3}	Supply Current 3*11	V_{DD} = 5.5V (at active after reset signal output)			0.45	1.7	μA
V_{OL}	"L" Output Voltage	V_{DD} ≥ 4.5V	I_{OL} = 8mA			0.3	V
		V_{DD} ≥ 3.3V	I_{OL} = 5mA				
		V_{DD} ≥ 1.65V	I_{OL} = 3mA				
V_{OH}	"H" Output Voltage*12	V_{DD} ≥ 4.5V	I_{OH} = 5mA	V_{DD} x 0.85			V
		V_{DD} ≥ 3.3V	I_{OH} = 2.5mA				
		V_{DD} ≥ 1.65V	I_{OH} = 0.8mA				
I_{LEAKI}	$\overline{SR0}$, $\overline{SR1}$ Input Leakage Current	V_{DD} = 5.5V				0.1	μA
I_{LEAKO}	Output Leakage Current	V_{DD} = 5.5V				0.1	μA
t_{DELAY}	Output Delay Time	DSR = GND		6	7.5	9	s
		DSR = V_{DD}		9	11.25	13.5	s
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltaget					0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltaget			0.85			V

All test items listed under Electrical Characteristics are done under the pulse load condition (Tj≈Ta=25ºC) except Supply Current 2.

*9 Supply current when the IC is active and waiting for the reset input.

*10 Supply current when the both $\overline{SR0}$ and $\overline{SR1}$ inputs are low and the timer operation is running.

*11 Supply current after the completion of timer operation and the output of rest signal.

*12 This applies only to R3200xxxxB (CMOS output).

The specifications surrounded by ⬚ are guaranteed by Design Engineering at –40°C ≤ Ta ≤ 85°C.

R3200xxx2x, R3200L053B (Ta=25ºC)

Symbol	Item	Conditions		Min.	Typ.	Max.	Unit
V_{DD}	Operating Voltage			1.65		5.5	V
I_{SS1}	Supply Current 1[*13]	V_{DD} = 5.5V (at standby)			0.28	1.35	μA
I_{SS2}	Supply Current 2[*14]	V_{DD} = 5.5V (at active after reset signal output)			3.0	6.5	μA
I_{SS3}	Supply Current 3[*15]	V_{DD} = 5.5V (at active after reset signal output)			0.45	1.7	μA
V_{OL}	"L" Output Voltage	V_{DD} ≥ 4.5V	I_{OL} = 8mA			0.3	V
		V_{DD} ≥ 3.3V	I_{OL} = 5mA				
		V_{DD} ≥ 1.65V	I_{OL} = 3mA				
V_{OH}	"H" Output Voltage[*16]	V_{DD} ≥ 4.5V	I_{OH} = 5mA	V_{DD} x0.85			V
		V_{DD} ≥ 3.3V	I_{OH} = 2.5mA				
		V_{DD} ≥ 1.65V	I_{OH} = 0.8mA				
I_{LEAKI}	$\overline{SR0}$, $\overline{SR1}$ Leakage Current	V_{DD} = 5.5V				0.1	μA
I_{LEAKO}	Output Leakage Current	V_{DD} = 5.5V				0.1	μA
t_{DELAY}	Output Delay Time[*17]			t_{DELAY_S} x 0.8	t_{DELAY_S}	t_{DELAY_S} x 1.2	sec
t_{REC}	Output Release Time[*17]			t_{REC_S} x 0.8	t_{REC_S}	t_{REC_S} x 1.2	sec
V_{IL}	$\overline{SR0}$, $\overline{SR1}$ "L" Input Voltaget					0.3	V
V_{IH}	$\overline{SR0}$, $\overline{SR1}$ "H" Input Voltaget			0.85			V

All test items listed under *Electrical Characteristics* are done under the pulse load condition (Tj≈Ta=25ºC) except Supply Current 2.

[*13] Supply current when the IC is active and waiting for the reset input.

[*14] Supply current when the both $\overline{SR0}$ and $\overline{SR1}$ inputs are low and the timer operation is running.

[*15] Supply current after the automatic cancellation of reset signal following the completion of timer operation and the output of rest signal.

[*16] This applies only to R3200xxxxB (CMOS output).

[*17] Refer to *Table 1. Output Delay Time and Output Release Time of R3200x*.

Table 1. Output Delay Time and Output Release Time of R3200x

Product Name	t_{DELAY_S}	t_{REC_S}
R3200x002x	7.5s	0.234s
R3200L052B	10s	0.313s
R3200L053B	10s	0.078s

TYPICAL APPLICATIONS

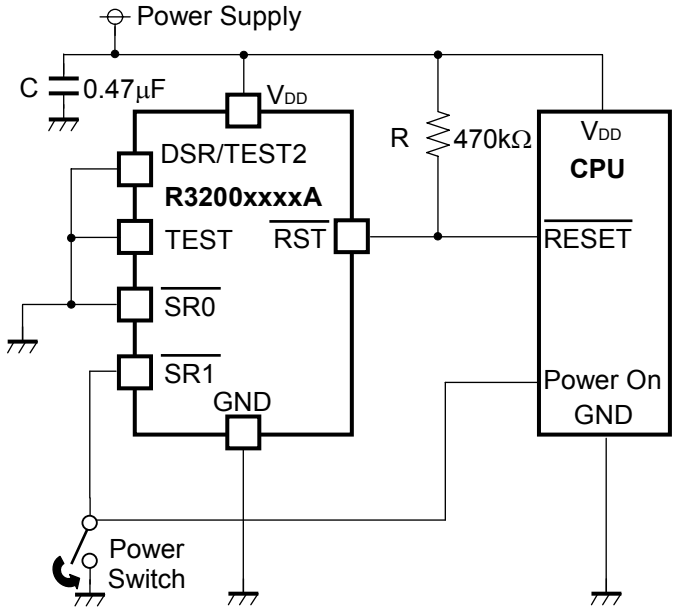


Figure 5. R3200xxxxA

$\overline{\text{RST}}$ pin should be pulled up with a resistor. The recommended value for the resistor is 470kΩ.
In the case of using one active-low input signal-pin, either $\overline{\text{SR0}}$ or $\overline{\text{SR1}}$ pin should be connected to GND.

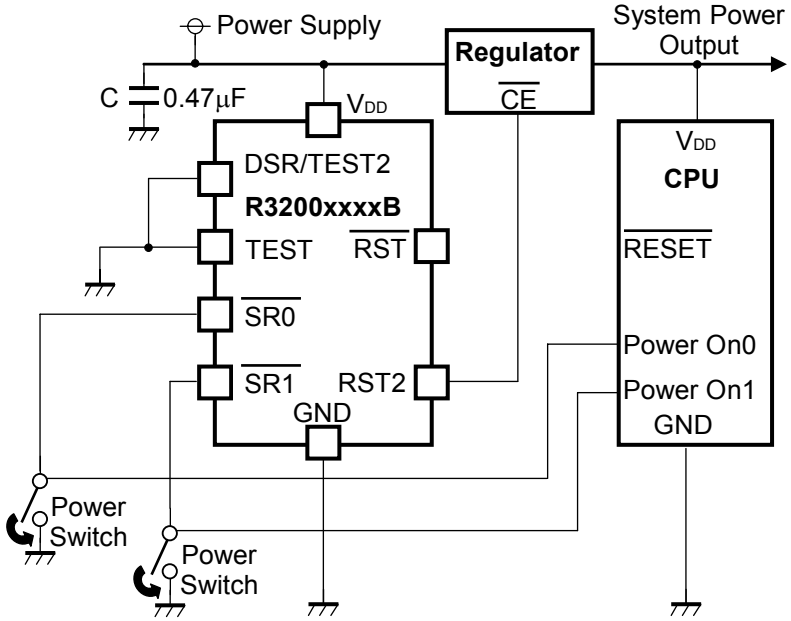


Figure 6. R3200xxxxB

(External Components)

C: Ceramic 0.47μF Ex. Murata GRM155B30J474KE18

TIMING CHART

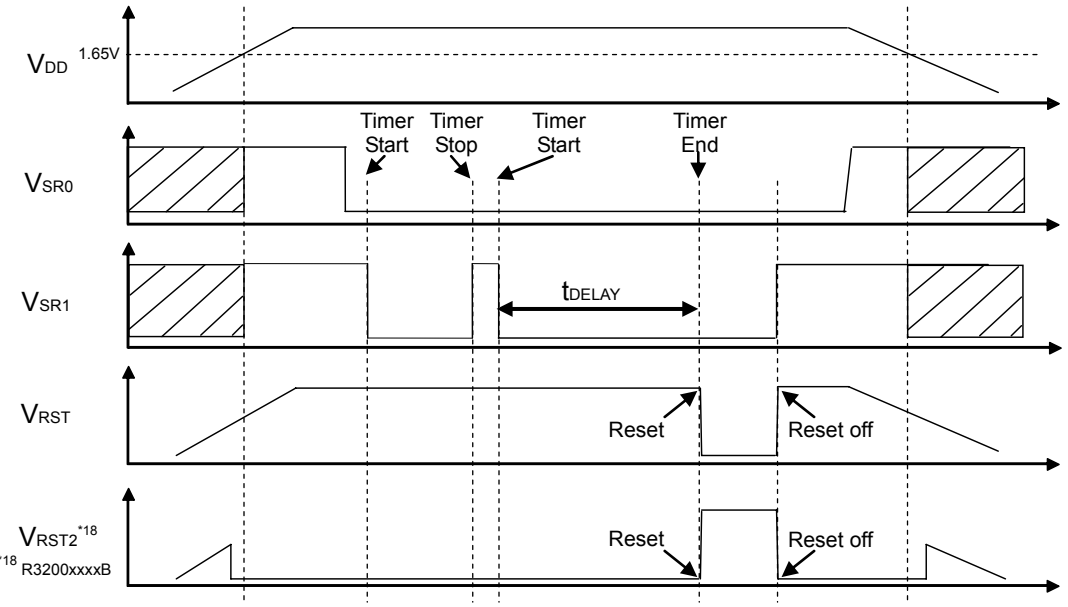


Figure 7. R3200x001x

OPERATION

R3200x001x

When both $\overline{SR0}$ and $\overline{SR1}$ voltages become “L”, the timer operation will start. After the output delay time (t_{DELAY}), the reset signal will be outputted. If either $\overline{SR0}$ or $\overline{SR1}$ voltage become “H”, the timer operation will be stopped.

During the output delay time, if either $\overline{SR0}$ or $\overline{SR1}$ becomes “H”, the timer operation will stop. If both $\overline{SR0}$ and $\overline{SR1}$ voltages become “L” again, after the output delay time (t_{DELAY}) the reset signal will be outputted.

While the reset signal is being outputted, either $\overline{SR0}$ or $\overline{SR1}$ voltage becomes “H”, the reset signal will be canceled. Until either $\overline{SR0}$ or $\overline{SR1}$ voltage becomes “H”, the reset signal will be continually outputted.

OUTPUT DELAY TIME SWITCHING

R3200x001x

The output delay time can be selected 7.5s (Typ.) or 11.25s (Typ.) by connecting DSR pin to either GND or to V_{DD}. However, if DSR is switched during the operations, the output would become unstable and may cause false operations. Switching DSR must be done during power-off. Also, DSR must be connected to either GND or V_{DD} because if DSR pin is not connected to either GND or V_{DD}, the output would become unstable and may cause false operations.

TIMING CHART

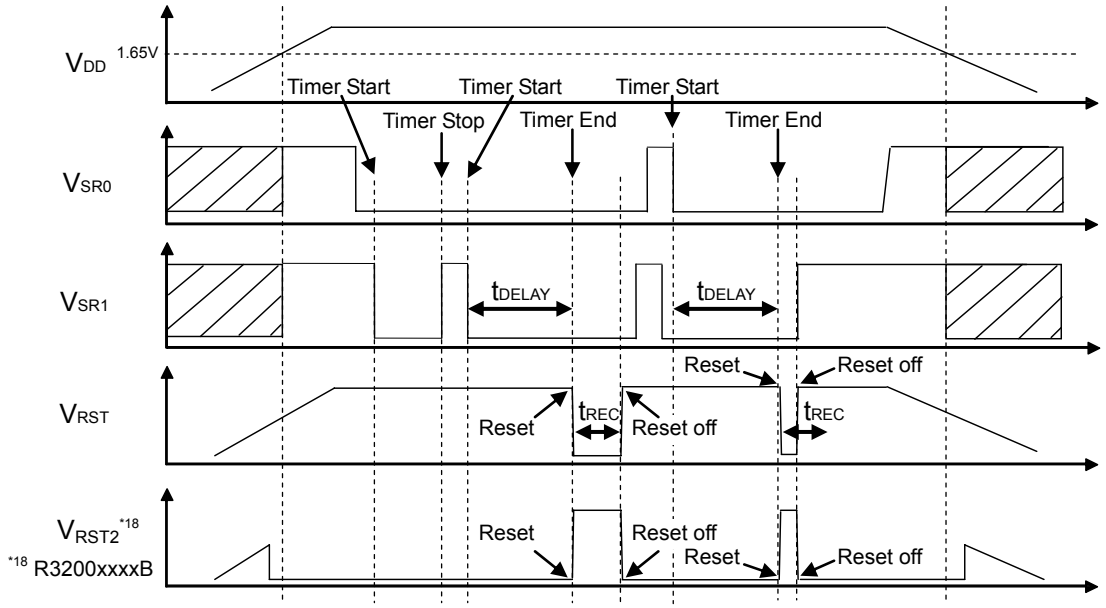


Figure 8. R3200xxx2x

OPERATION

R3200xxx2x, R3200L053B

When both $\overline{SR0}$ and $\overline{SR1}$ voltages become “L”, the timer operation will start. After the output delay time (t_{DELAY}), the reset signal will be outputted. If either $\overline{SR0}$ or $\overline{SR1}$ voltage become “H”, the timer operation will be stopped.

During the output delay time, if either $\overline{SR0}$ or $\overline{SR1}$ becomes “H”, the timer operation will stop. If both $\overline{SR0}$ and $\overline{SR1}$ voltages become “L” again, after the output delay time (t_{DELAY}) the reset signal will be outputted.

After reset signal is being sent, it will be released automatically, or if either SR0 or $\overline{SR1}$ becomes “H”, the reset signal will be canceled.

OUTPUT DELAY TIME GAP

The threshold voltages of $\overline{SR0}$ and $\overline{SR1}$ are between V_{IL} and V_{IH}. Therefore, if the rising or falling slew rate is very slow, the timer will start at the point of crossing the threshold voltage and may cause errors in the output delay time (t_{DELAY}) and the released reset time.

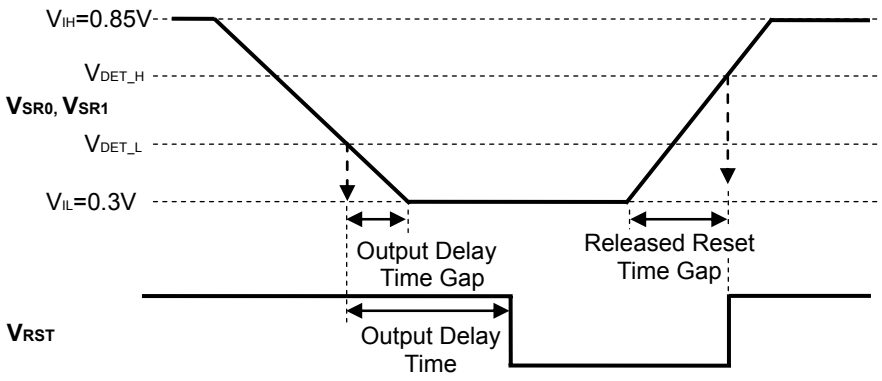


Figure 9. Relation between the Rising and Falling Slew Rate and the Time Gap

PRECAUTIONS: V_{DD} Start-up during Low Input

When starting up V_{DD} at slow slew rate of 0.001V/µs or less with the low $\overline{SR0}$ and $\overline{SR1}$ voltages, the ICs may start the operation at lower than the minimum operating voltage, thus the output delay time may exceed the guaranteed time.

TEST CIRCUITS

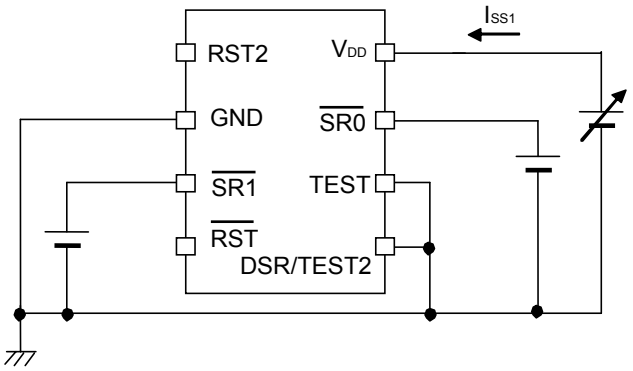


Figure 10. Supply Current Test Circuit

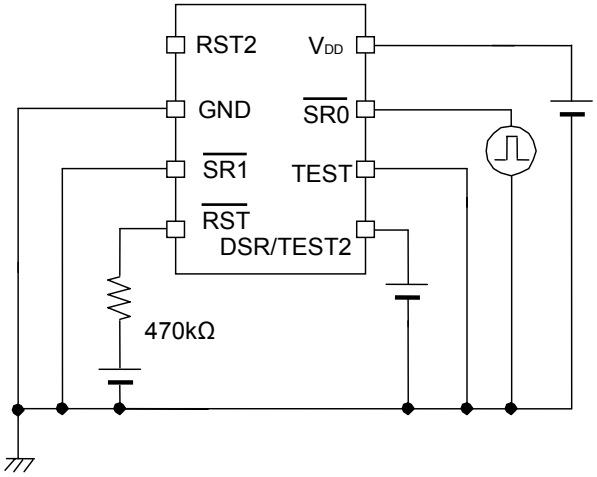


Figure 11. Output Delay Time Test Circuit

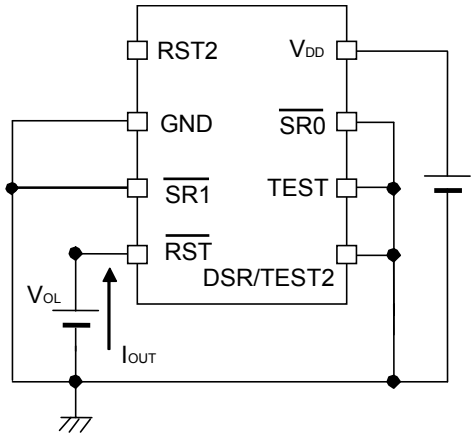


Figure 12. Nch Driver Output Voltage Test Circuit

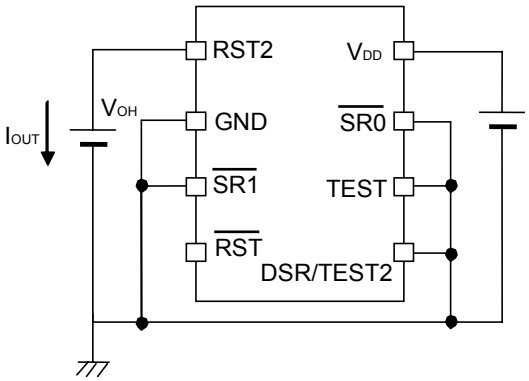


Figure 13. CMOS Driver Output Voltage Test Circuit (This applies only to R3200xxxxB.)

PRECAUTIONS: Circuit Configuration

In the case of applying the following circuit configuration (Figure 14) to the R3200x Series, if the R1 value is high, the ICs own supply current may cause significant voltage drop to V_{DD} pin, and V_{DD} voltage may fall below the minimum operating voltage.

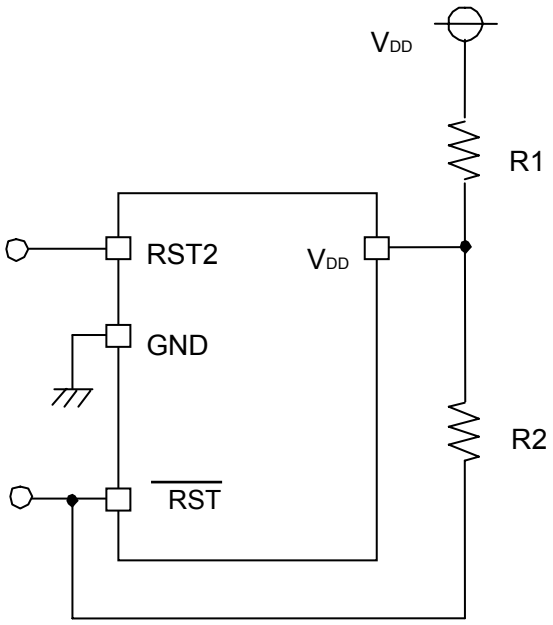
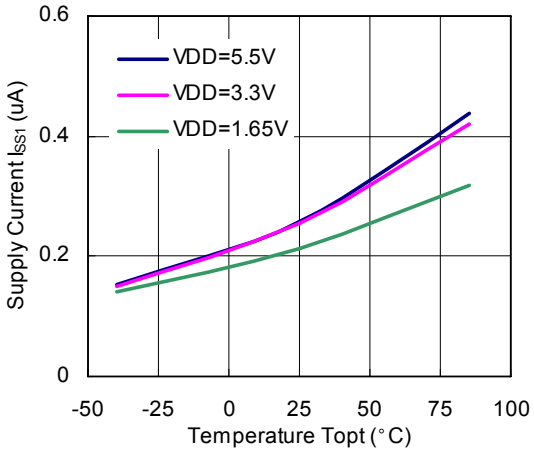


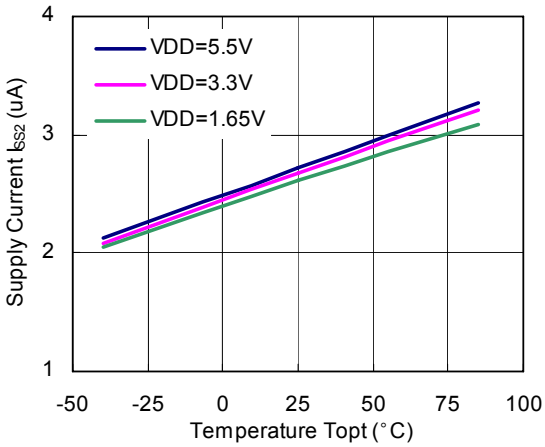
Figure 14. Circuit Configuration Example

TYPICAL CHARACTERISTICS

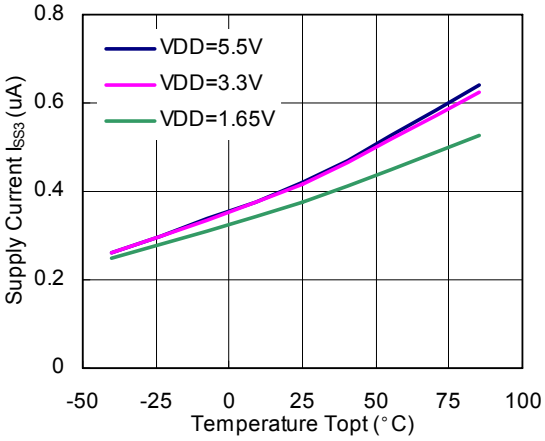
1) Supply Current 1 vs. Temperature
R3200x (at standby)



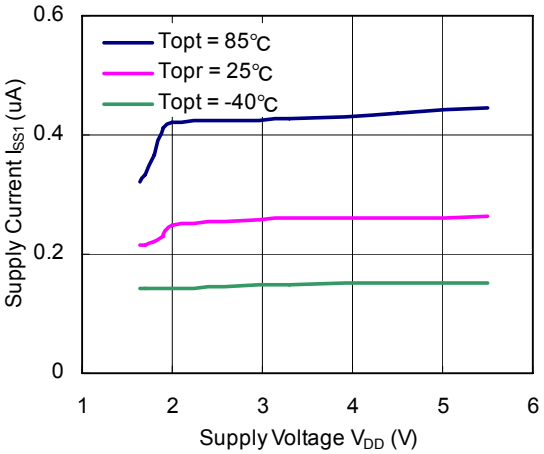
2) Supply Current 2 vs. Temperature
R3200x (before the reset signal output)



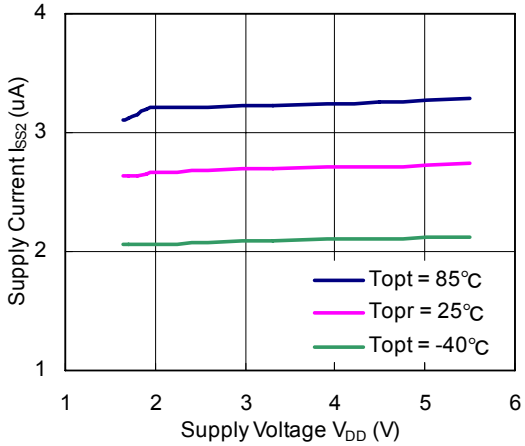
3) Supply Current 3 vs. Temperature
R3200x (after the reset signal output)



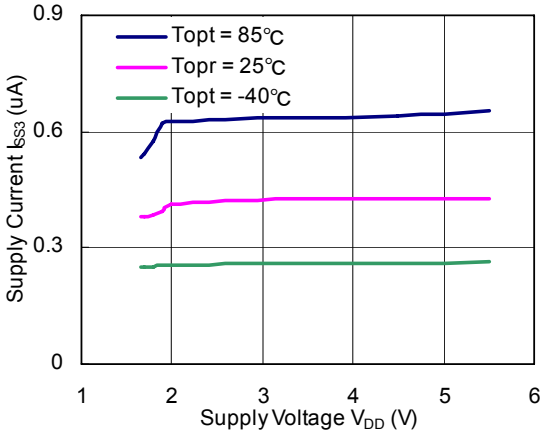
4) Supply Current 1 vs. Supply Voltage
R3200x (at standby)



5) Supply Current 2 vs. Supply Voltage
R3200x (before the reset signal output)

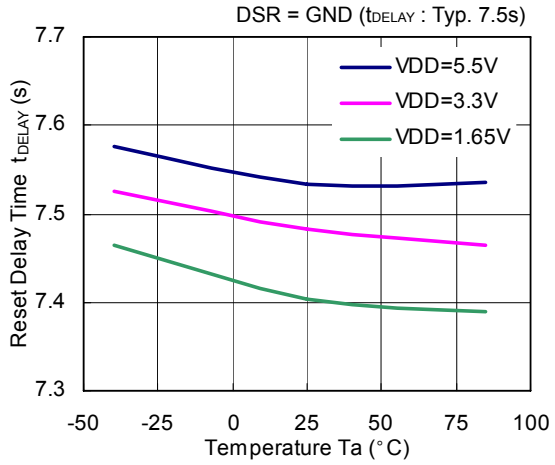


6) Supply Current 2 vs. Supply Voltage
R3200x (after the reset signal output)

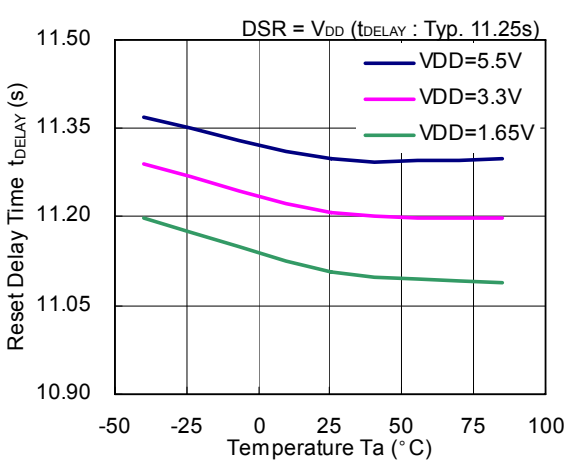


7) Output Delay Time vs. Temperature

R3200x001x

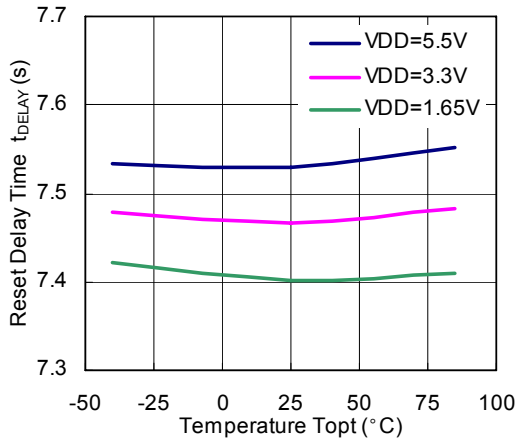


R3200x001x

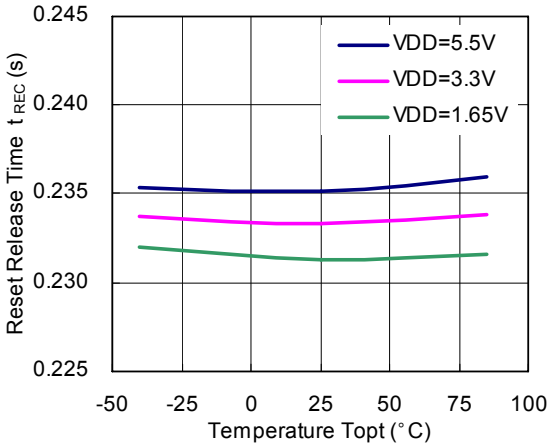


8) Output Release Time vs. Temperature

R3200x002x

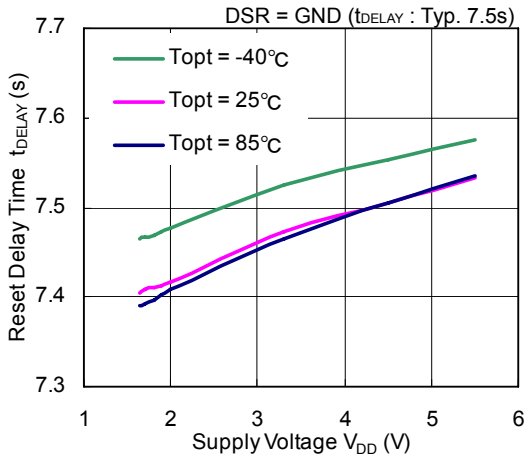


R3200x002x

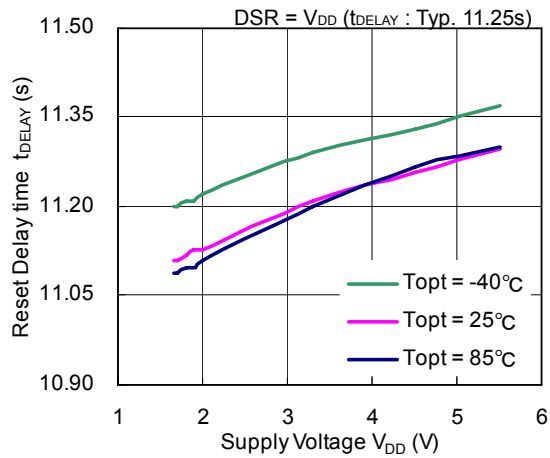


9) Output Delay Time vs. Supply Voltage

R3200x001x

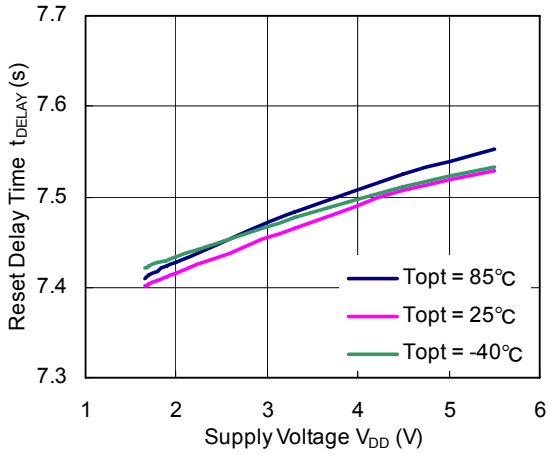


R3200x001x

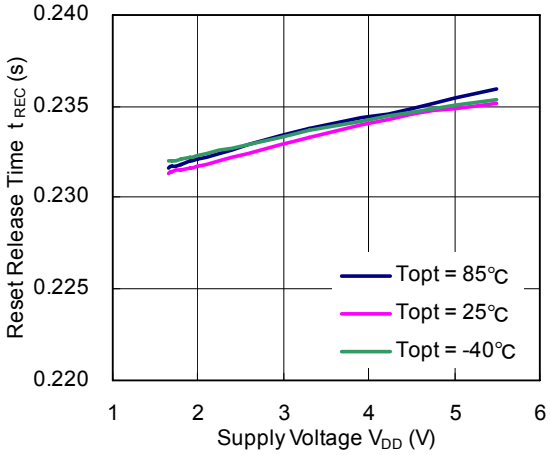


10) Output Release Time vs. Supply Voltage

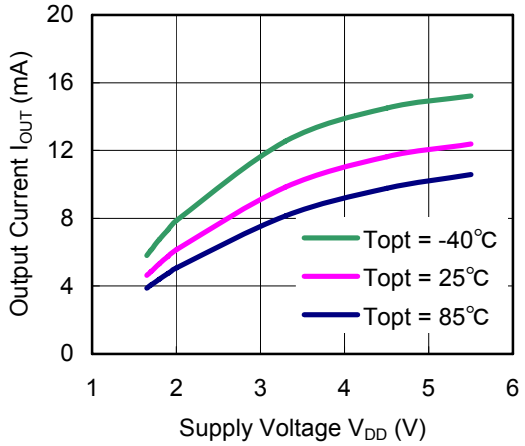
R3200x002x



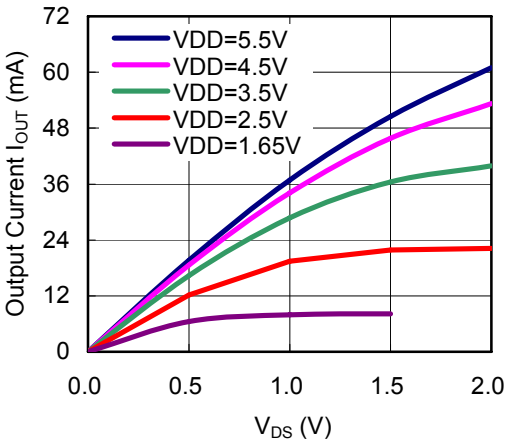
R3200x002x



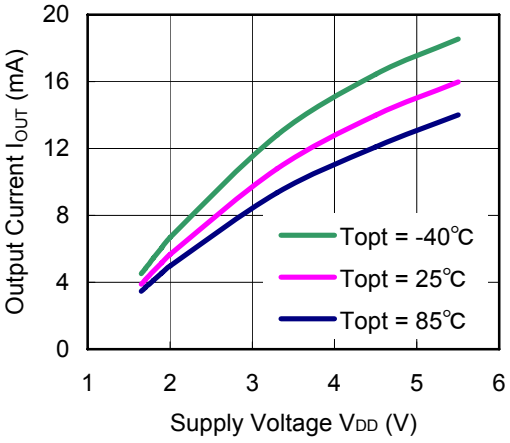
11) Nch Driver Output Current vs. Supply Voltage V_{DS}=0.3V



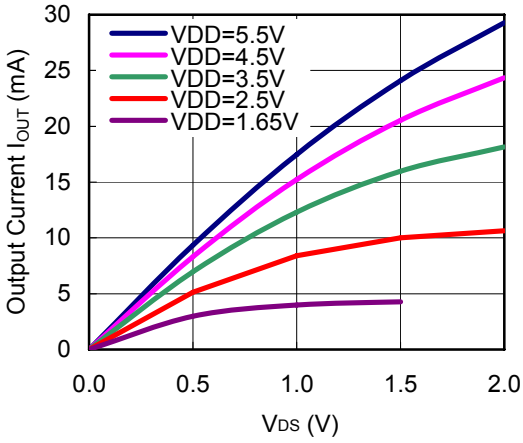
12) Nch Driver Output Current vs. V_{DS}



13) Pch Driver Output Current vs. Supply Voltage V_{DS}=0.9V



14) Pch Driver Output Current vs. V_{DS}



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