RICOH

R1243x SERIES

30V Input 2A Buck DC/DC Converter

NO.EA-206-111123

OUTLINE

The R1243x Series is the CMOS-based Step-Down DC/DC Converter with internal Nch high side Tr. (0.175Ω), which can provide the maximum 2A output current. The IC consists of an Oscillator, a PWM control circuit, a Reference Voltage unit, an Error amplifier, phase compensation circuits, a slope circuit, a soft start circuit, protection circuits, internal voltage regulators, and a switch for bootstrap circuit. The R1243x Series can make up a Step-Down DC/DC Converter with the following external components: an inductor, resistors, a diode, and capacitors.

The R1243x series are current mode operating type DC/DC converter which does not require external current sense resistor, and it works high speed response time, high efficiency and compatible with ceramic capacitors.

There are two types for the oscillator frequency. A/B version's frequency is fixed 1000kHz, and C/D version's frequency is fixed 330kHz.As a protection function, it has cycle by cycle peak current limit function, short protection function, thermal shutdown function and UVLO.

There are two types for short protection, A/C version has latch protection function with 2ms delay time, and B/D version has fold back protection function that keep operating at short condition with lower operating frequency and limiting the Lx current.

The R1243 Series has the built-in soft start time (Typ. 0.4ms). In addition to this, the soft start time is adjustable by adding an external capacitor. The R1243x Series has the FLG pin, which mainly monitors the FB pin voltage and gives the flag output by the Nch open drain if the abnormal condition is detected.

Since the packages for these ICs are HSOP-8E, and DFN(PLP)2527-10, therefore high density mounting of the ICs on boards is possible.

FEATURES

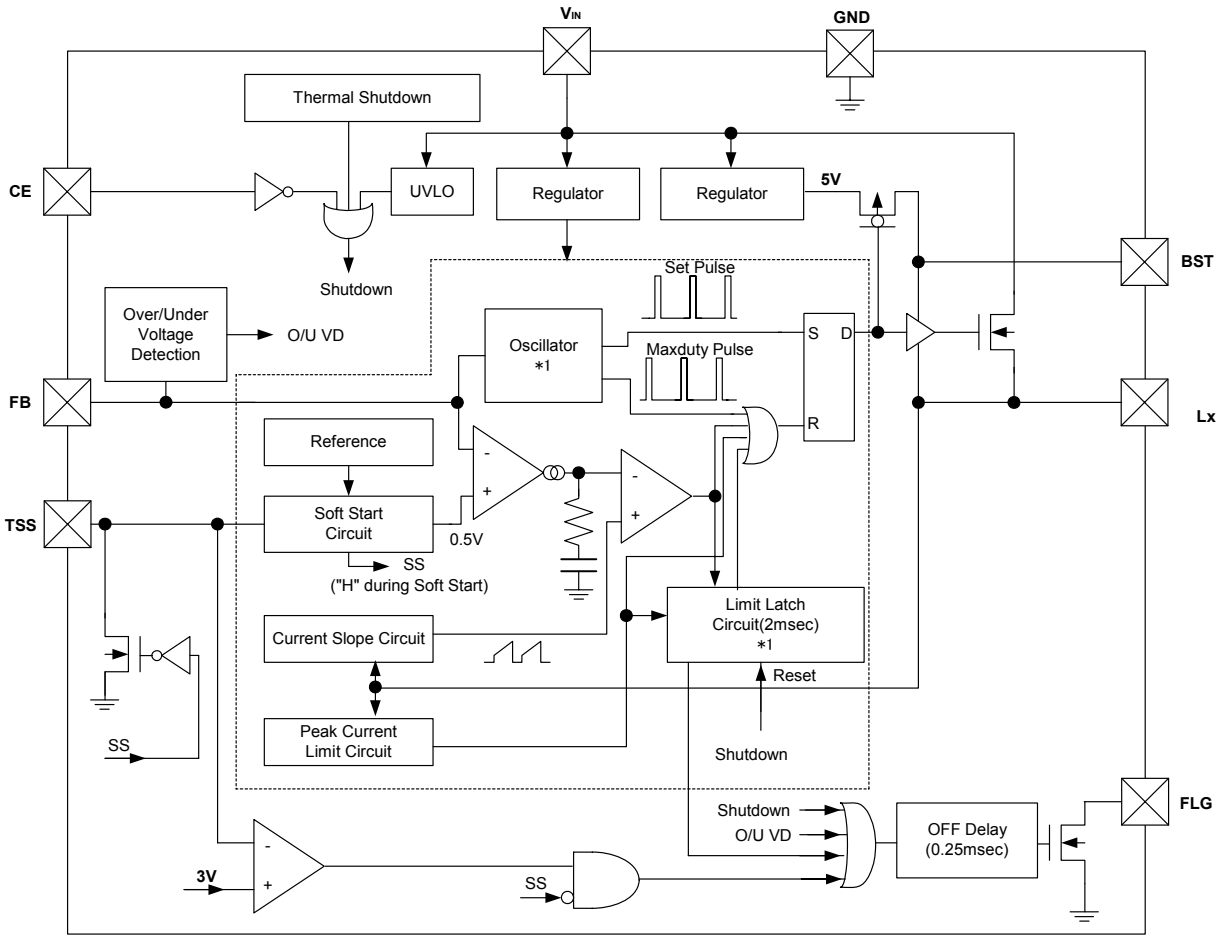
- Operating Voltage ..... 4.5V ~ 30V
- Standby Function ..... Typ. 0μA, Max. 10μA (V_{IN}=30V, CE="L")
- Supply Current ..... Typ. 0.7mA (V_{IN}=30V V_{FB}=1.0V)
- Output Voltage Range..... 0.8V ~ 18V (Adjustable with external resistor)
- Feed Back Voltage..... 0.5V with 1.4% accuracy
- Output Current ..... Max. 2A
- Peak Current Limit Function ..... Typ. 3.8A
- Internal Nch MOSFET Driver ..... Typ. 175mΩ
- Maximum Duty Cycle ..... Min. 85%
- Operating Frequency ..... Ver.A/B 1000kHz, Ver.C/D 330kHz
- Short protection delay time for Output Latch ..... Typ. 2ms : Ver.A/C
- Built-in Foldback Protection and its Frequency ... 1/4 frequency at fold condition : Ver.B/D
  ..... Ver.B 250kHz, Ver.D 82.5kHz
- Internal Soft Start Time ..... Typ. 0.4ms, with TSS pin open
- External Soft Start Time ..... Typ. 12ms, with C_{SS}=0.1μF
- Flag Output Function ..... Typ. 0.25ms, FLG "OFF" delay time
- UVLO Released Voltage ..... Typ. 4.0V
- Thermal Shutdown Function ..... Typ. 160°C, with 35°C hysteresis
- Package ..... HSOP-8E, DFN(PLP)2527-10

∗)This is an approximate value, because output current depends on conditions and external parts.

APPLICATIONS

- Power source for digital home appliance
- Power source for hand-held communication equipment, cameras, video instruments such as VCRs, camcorders.
- Power source for battery-powered equipment.
- Battery Charger

BLOCK DIAGRAMS



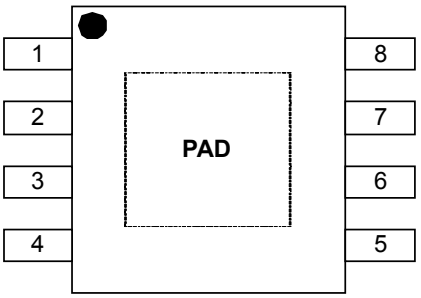
*1

Ver.	fosc	Short Protection
A	1000kHz	Latch
B	1000kHz	Foldback
C	330kHz	Latch
D	330kHz	Foldback

PIN CONFIGURATIONS

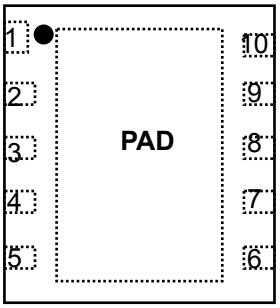
- **HSOP-8E**

Top View

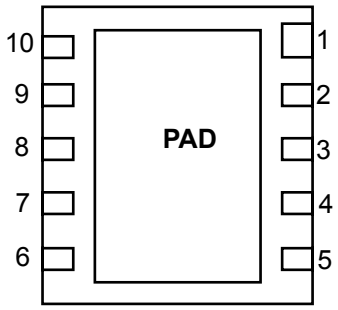


- **DFN(PLP)2527-10**

Top View



Bottom View



PIN DESCRIPTIONS

- **HSOP-8E**

Pin No	Symbol	Pin Description
1	BST	Bootstrap Pin
2	V_{IN}	Power Supply Pin
3	L_X	L_X Switching Pin
4	GND	Ground Pin
5	FB	Feedback Pin
6	FLG	Flag Output Pin
7	CE	Chip Enable Pin (Active with “H”)
8	TSS	Soft Start Pin

* Tab is GND level. (They are connected to the reverse side of this IC.)

- **DFN(PLP)2527-10**

Pin No	Symbol	Pin Description
1	L_X	L_X Switching Pin
2	L_X	L_X Switching Pin
3	GND	Ground Pin
4	FB	Feedback Pin
5	FLG	Flag Output Pin
6	CE	Chip Enable Pin (Active with “H”)
7	TSS	Soft Start Pin
8	BST	Bootstrap Pin
9	V_{IN}	Power Supply Pin
10	V_{IN}	Power Supply Pin

* Tab is GND level. (They are connected to the reverse side of this IC.)

SELECTION GUIDE

In the R1243x Series, type of short protection (Latch or Foldback), frequency (1000kHz, or 330kHz), and package for the ICs can be selected at the user's request.

Product Name	Package	Quantity per Reel	Pb Free	Halogen Free
R1243S001∗-E2-FE	HSOP-8E	1,000pcs	Yes	Yes
R1243K001∗-TR	DFN(PLP)2527-10	5,000pcs	Yes	Yes

∗ : Latch or Foldback, frequency can be selected at the user's request

(A) Fixed frequency 1000kHz, Latch protection
(B) Fixed frequency 1000kHz, Foldback protection
(C) Fixed frequency 330kHz, Latch protection
(D) Fixed frequency 330kHz, Foldback protection

ABSOLUTE MAXIMUM RATINGS

(GND=0V)

Symbol	Item	Rating		Unit
V_{IN}	Input Voltage	-0.3V~32V		V
V_{BST}	Boost Pin Voltage	V_{LX}-0.3V~V_{LX}+6V		V
V_{LX}	Lx Pin Voltage	-0.3V~V_{IN}+0.3		V
V_{CE}	CE Pin Input Voltage	-0.3V~V_{IN}+0.3		V
V_{FB}	VFB Pin Voltage	-0.3V~6V		V
V_{FLG}	FLG Pin Voltage	-0.3V~6V		V
V_{TSS}	TSS Pin Voltage	-0.3V~6V		V
P_D	Power Dissipation (HSOP-8E)*	2900*		mW
	Power Dissipation (DFN(PLP)2527-10) *	Standard Land Pattern	910*	
		High Wattage Land Pattern	1400*	
Ta	Operating Temperature Range	-40~85		ºC
Tstg	Storage Temperature Range	-55~125		ºC

*) For Power Dissipation, please refer to PACKAGE INFORMATION to be described.

ABSOLUTE MAXIMUM RATINGS

Electronic and mechanical stress momentarily exceeded absolute maximum ratings may cause the permanent damages and may degrade the life time and safety for both device and system using the device in the field. The functional operation at or over these absolute maximum ratings is not assured.

ELECTRICAL CHARACTERISTICS

(Otherwise notified in Conditions, V_{IN}=12V,Ta=25ºC)

Symbol	Item	Conditions	MIN.	TYP.	MAX.	Unit
V_{IN}	Operating Input Voltage		4.5		30	V
Istandby	Standby Current	V_{IN}=30V, V_{CE}=0V		0	10	μA
I_{IN}	V_{IN} Consumption Current	V_{IN}=30V, V_{FB}=1.0V		0.7	1.0	mA
V_{UVLO1}	UVLO Detector Threshold	Falling	3.6	3.8	4.0	V
V_{UVLO2}	UVLO Released Voltage	Rising	3.8	4.0	4.2	V
$V_{UVLOHYS}$	UVLO Hysteresis	V_{UVLO2}-V_{UVLO1}		0.2		V
V_{FB}	Feedback Voltage		0.493	0.500	0.507	V
$\Delta V_{FB}/\Delta T$	Feedback Voltage Temperature Coefficient	-40ºC ≤ Ta ≤ 85ºC		±100		ppm /ºC
fosc	Oscillator Frequency (Ver.A,B)		900	1000	1100	kHz
	Oscillator Frequency (Ver.C,D)		290	330	370	kHz
f_{FLB}	Fold back Frequency (Ver.B,D)	V_{FB}<0.35V, fosc ratio		25		%
Maxduty	Oscillator Maximum Duty Cycle	V_{IN}=6V	85	90	95	%
I_{TSS}	TSS Pin Current	V_{TSS}=0V		4.0		μA
t_{SS0}	Soft Start Time	TSS=open	0.2	0.4	0.8	ms
t_{SS1}	Soft Start Time	C_{SS}=0.1μF	6	12	18	ms
t_{DLY}	Delay Time For Latch Protection (Ver.A,C)	V_{IN}=5.0V		2.0		ms
I_{LXHOFF}	High side switch Leakage Current	V_{IN}=30V, V_{CE}=0V		0	10	μA
R_{LXH}	High side switch ON Resistance	V_{BST}-V_{LX}=4.5V		175		mΩ
I_{LIMLXH}	High side switch Limited Current	V_{BST}-V_{LX}=4.5V	2.8	3.8		A
V_{CEH}	CE “H” Input Voltage	V_{IN}=30V	1.4			V
V_{CEL}	CE “L” Input Voltage	V_{IN}=30V			0.4	V
I_{CEH}	CE “H” Input Current	V_{IN}=30V, V_{CE}=30V	-1.0	0	1.0	μA
I_{CEL}	CE “L” Input Current	V_{IN}=30V, V_{CE}=0V	-1.0	0	1.0	μA
I_{FBH}	FB “H” Input Current	V_{FB}=2.0V	-1.0	0	1.0	μA
I_{FBL}	FB “L” Input Current	V_{FB}=0.0V	-1.0	0	1.0	μA
t_{TSD}	Thermal Shutdown Detect Temperature	Hysteresis 35ºC		160		ºC
V_{FLGL}	FLG “L” Voltage	I_{FLG}=1mA			0.4	V
I_{FLGOFF}	FLG “OFF” Current	V_{FLG}=5.5V		0.0	1.0	μA
t_{FLGOFF}	FLG “OFF” Delay Time		0.05	0.25	0.60	ms
V_{OVD}	Over Voltage Detect Voltage	V_{FB}	0.55	0.60	0.65	V
V_{UVD}	Under Voltage Detect Voltage	V_{FB}	0.35	0.40	0.45	V

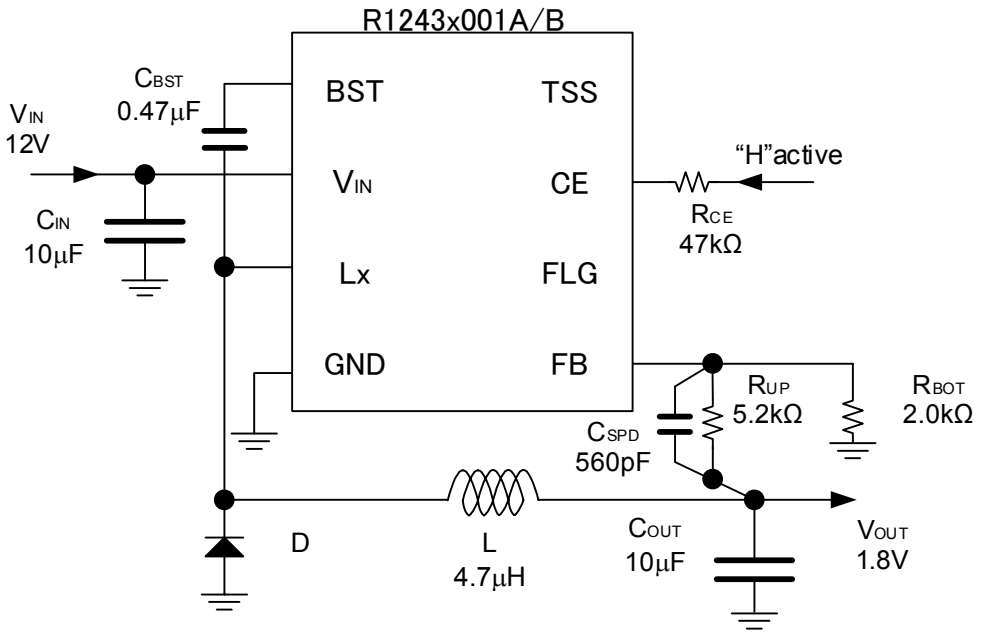
RECOMMENDED OPERATING CONDITIONS (ELECTRICAL CHARACTERISTICS)

All of electronic equipment should be designed that the mounted semiconductor devices operate within the recommended operating conditions. The semiconductor devices cannot operate normally over the recommended operating conditions, even if when they are used over such conditions by momentary electronic noise or surge. And the semiconductor devices may receive serious damage when they continue to operate over the recommended operating conditions.

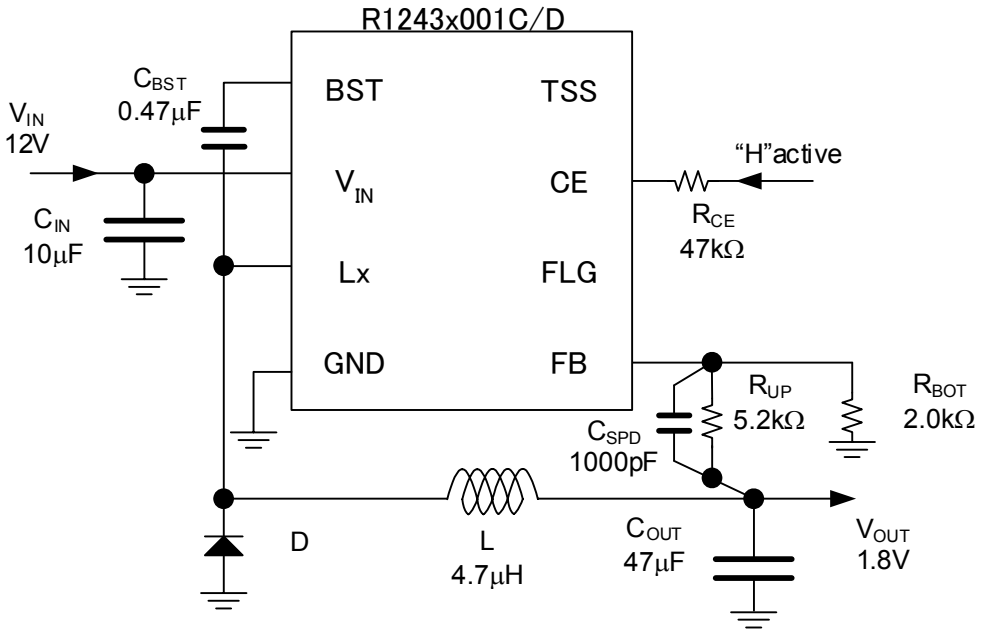
Typical Applications and Notes Concerning External Parts

Typical Applications

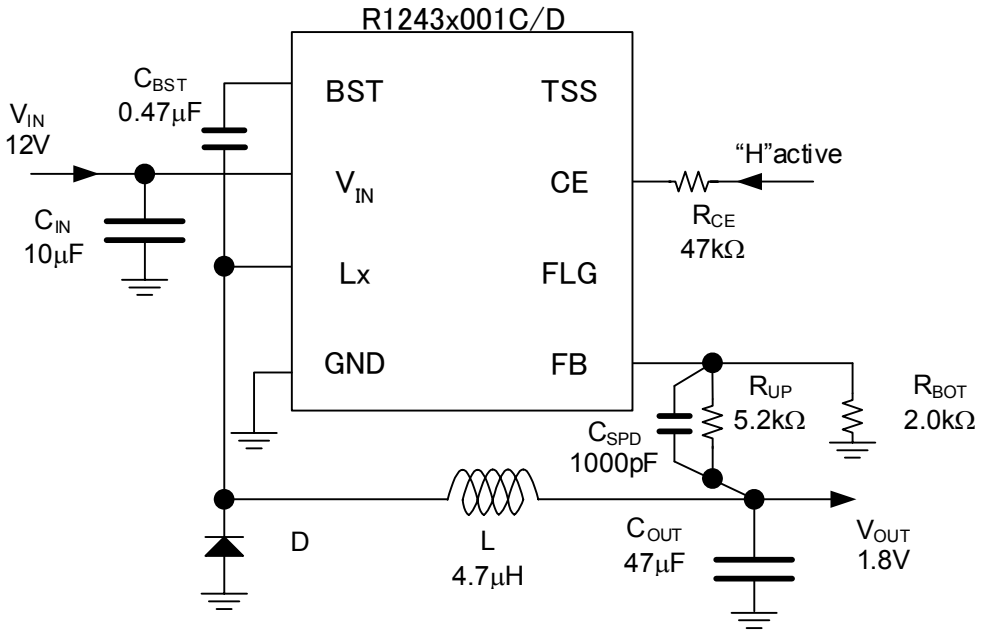
R1243x001A/B, V_{OUT}=1.8V, t_{SS}=0.4ms setting.



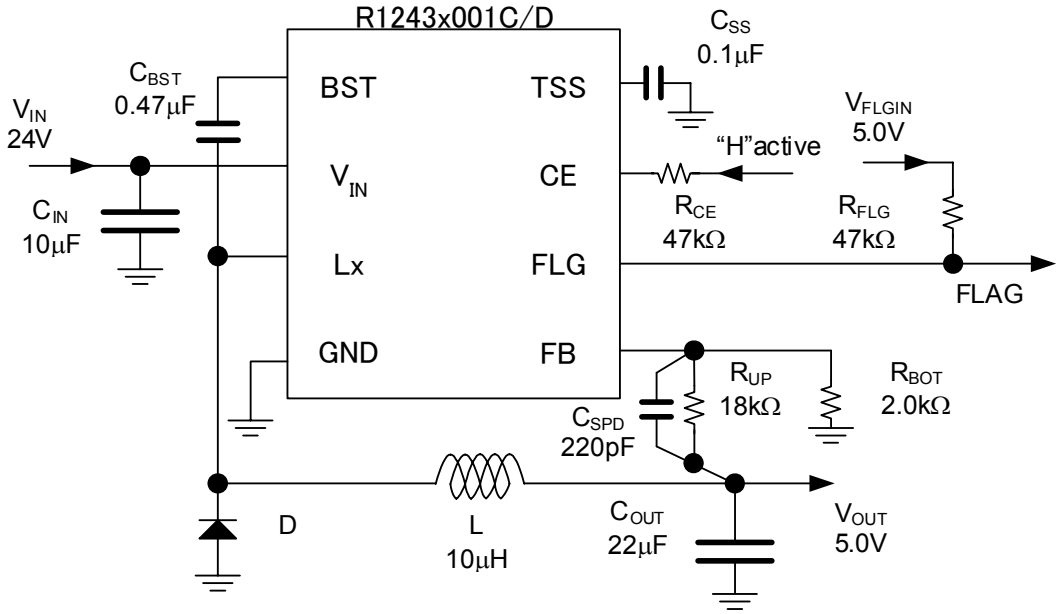
R1243x001C/D, V_{OUT}=1.8V, t_{SS}=0.4ms setting.



R1243x001A/B, V_{OUT}=5.0V, t_{SS}=12ms setting, Flag function using.



R1243x001C/D, V_{OUT}=5.0V, t_{SS}=12ms setting, Flag function using.



FLG pin is open-drain output that is pulled to ground at the conditions below:

·CE="L" (Shut down) ·UVLO (Released voltage Typ.4.0V) ·Thermal Shutdown

·V_{FB} Over Voltage Detection (Typ.0.6V) ·V_{FB} Under Voltage Detection (Typ.0.4V)

·Active Latch function (Ver.A/C)

·T_{SS} pin's Over Voltage Protection after the completion of soft start (Typ.3V)

When the R1243x starts up, without the conditions above, after soft-start time, V_{FB} under voltage detection (Typ. 0.4V) is released, then after the released delay time (Typ. 0.25ms) the output of FLG pin pulled to “H”. However, if V_{OUT} is used as V_{FLGIN}, even if the soft start time hasn't finished, the output of FLG pin becomes “H” or same as V_{OUT} and released delay time disappears.

Therefore, if soft-start time is used for the circuit sequence, the difference of the operation depending on the V_{FLGIN} (connected to V_{OUT} directly or other voltage source) must be cared.

Notes Concerning to External Parts

- External components have to be connected as close as possible to the IC and have to be wired as short as possible. Especially, the capacitor connected between V_{IN} and GND pin must be wired the shortest. If the impedances of the power supply line and the GND line are high, the operation can be unstable due to the switching current, which fluctuates the power line of the inside the IC. The impedances of power supply line and GND line must be as low as possible. It is necessary to give careful consideration to the large current flowing into the power supply, GND, L_X, V_{OUT} and inductor when designing their wirings. The wiring of output voltage setting resistance (R_{UP}) and the wiring of inductor must be separated from load wiring.
- The capacitors to be used in the R1243x Series must be low ESR ceramic capacitors. The C_{IN} capacitor between V_{IN} and GND should be equal or more than 10μF. Please pay attention to the bias-dependent properties and the temperature variability characteristics of the ceramic capacitors.
- The internal phase compensation of this IC is designed within the recommended values of inductor and C_{OUT} ceramic capacitor. If the inductor value is small, the peak values of the switching current increase along with the load current. When the peak value of the switching current reaches to the current limit, the over current protection circuit may start to function.
- If the parasitic capacitor of the schottky diode is large, the operation may result in unstable because of the large switching current when the switch is turned on. Please use the schottky diode with 100pF or less when the reverse voltage is 10V.
- The output voltage (V_{OUT}) can be calculated by this equation: $V_{OUT} = V_{FB} \times (R_{UP}+R_{BOT}) / R_{BOT}$. By changing R_{UP} and R_{BOT}, the output voltage (V_{OUT}) is adjustable. If resistance values of R_{UP} and R_{BOT} are high, the impedance of the FB pins become high, and the IC becomes vulnerable to an influence of noise. R_{BOT} is recommended to be between 1.0kΩ to 4.7kΩ. If the operation become unstable due to the high impedance, it is important to consider lowering the impedance.
- In the IC, ESD protection diode is connected between CE pin and V_{IN} pin. If there is a possibility that the CE pin voltage becomes higher than the V_{IN} pin voltage, it is recommended to insert a 10kΩ resistance or more in order to prevent the large current flowing from CE pin into V_{IN} pin.
- Connect the reverse side of the IC pad to GND. To improve the radiation of heat of the multiple-layered board, it is effective to make the Via on the connection part of the reverse side of the IC pad to release the heat to multiple layers.
- The flag resistor (R_{FLG}) is recommended to be between 10kΩ to 100kΩ. If the flag function is not used, FLG pin has to be left open or connected to GND.
- If the soft start time adjustment function is not used, TSS pin must be left open. In this case, soft start time is set as 0.4ms (Typ.).
- After the completion of the soft start, latch function (Ver.A/C) starts to function. The internal counter starts counting up when the overcurrent protection circuits runs the current limit detection. When the internal counter counts up to 2ms(Typ.), latch function turns off the output. The turned off output can be reset when CE pin is changed to “L”, and also V_{IN} pin voltage became less than 3.8V (Typ.), which is UVLO detecting voltage. If the output voltage becomes more than the setting voltage (FB pin voltage is 0.50V (Typ.) within the latch timer period, the counter restores the default. Therefore, the careful attention is required when the power-supply voltage’s start-up is slow and the output voltage is not reached to the setting voltage within the latch timer period after the completion of the soft start.
- After the completion of the soft start, fold back function (Ver.B/D) starts to function. The fold back function limits the oscillation frequencies into 1/4 when FB pin voltage becomes less than 0.35V (Typ.). Therefore, the careful attention is required when the power-supply voltage’s start-up is slow and the output voltage

is not reached to the 70% (Typ.) of the setting voltage even for a short period of time after the completion of the soft start.

- The quality of the power supply circuit using the R1243x Series largely depends on the external components. The careful attention is required for the external component parameters.
- The careful attention is required for the maximum ratings (voltage, current, and wattage) of the external components, board layout pattern and the IC.
- The table on the next page shows the recommended values for setting output voltage.

Table1 R1243 Recommended value for each Output Voltage

・R1243x001A/B 1000kHz

V_{IN}	V_{OUT}	L[μH]	C_{OUT}[μF]	C_{SPD}*1	C_{BST}[μF]	R_{BOT}[kΩ]
4.5 ≤ V_{IN} ≤ Max	0.8 ≤ V_{OUT} ≤ 1.2	2.2	47	∗1	0.47	2.0
4.5 ≤ V_{IN} ≤ Max	1.2 ≤ V_{OUT} ≤ 1.8	2.2	22	∗1	0.47	2.0
4.5 ≤ V_{IN} ≤ Max	1.8 ≤ V_{OUT} ≤ 2.5	4.7	10	∗1	0.47	2.0
4.5 ≤ V_{IN} ≤ 6	2.5 ≤ V_{OUT} ≤ Maxduty	4.7	22	open	0.47	2.0
6 ≤ V_{IN} ≤ Max	2.5 ≤ V_{OUT} ≤ 5	4.7	10	∗1	0.47	2.0
Min ≤ V_{IN} ≤ Max	5 ≤ V_{OUT} ≤ Maxduty	4.7	10	∗1	0.47	2.0

・R1243x001C/D 330kHz

V_{IN}	V_{OUT}	L[μH]	C_{OUT}[μF]	C_{SPD}*2	C_{BST}[μF]	R_{BOT}[kΩ]
4.5 ≤ V_{IN} ≤ 7.5	0.8 ≤ V_{OUT} ≤ 1.2	4.7	47×2	open	0.47	2.0
4.5 ≤ V_{IN} ≤ 7.5	1.2 ≤ V_{OUT} ≤ Maxduty	10	47×2	open	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	0.8 ≤ V_{OUT} ≤ 1.2	4.7	47×2	∗2	0.47	2.0
7.5 ≤ V_{IN} ≤ 12	1.2 ≤ V_{OUT} ≤ 2.5	10	47	∗2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	1.2 ≤ V_{OUT} ≤ 2.5	4.7	47	∗2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	2.5 ≤ V_{OUT} ≤ 5	10	22	∗2	0.47	2.0
7.5 ≤ V_{IN} ≤ Max	5 ≤ V_{OUT} ≤ 18	10	10×2	∗2	0.47	2.0

∗1 R1243x001A/B 1000kHz C_{SPD}

V_{OUT}[V]	C_{SPD}[pF]	R_{UP}[kΩ]	R_{BOT}[kΩ]
0.8	1800	1.2	2.0
1	1200	2.0	2.0
1.2	1000	2.8	2.0
1.5	820	4.0	2.0
1.8	560	5.2	2.0
2.5	390	8.0	2.0
3.3	220	11.2	2.0
5	150	18.0	2.0
6	120	22.0	2.0
9	82	34.0	2.0
12	56	46.0	2.0
15	47	58.0	2.0
18	47	70.0	2.0

∗2 R1243x001C/D 330kHz C_{SPD}

V_{OUT}[V]	C_{SPD}[pF]	R_{UP}[kΩ]	R_{BOT}[kΩ]
0.8	2700	1.2	2.0
1	2200	2.0	2.0
1.2	1500	2.8	2.0
1.5	1200	4.0	2.0
1.8	1000	5.2	2.0
2.5	560	8.0	2.0
3.3	390	11.2	2.0
5	220	18.0	2.0
6	180	22.0	2.0
9	150	34.0	2.0
12	100	46.0	2.0
15	100	58.0	2.0
18	100	70.0	2.0

Table2 R1243 Recommended external components

C_{IN}	V_{IN}	Cap.	Spec.	Part Name	Manufacturer
	≤ 12.5V	10μF	25V	GRM31CR71E106K	muRata
	≤ 12.5V	10μF	25V	CM316X5R106K25ABH	Kyocera
	all	10μF	50V	UMK325BJ106MM-T	Taiyo Yuden

C_{OUT}	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
	≤ 8V	47μF	16V	GRM32EB31C476KE15	muRata
	≤ 5V	22μF	10V	GRM31CR71A226M	muRata
	≤ 12.5V	10μF	25V	GRM31CR71E106K	muRata
	≤ 8V	22μF	16V	CM316X5R226K16AB	Kyocera
	≤ 12.5V	22μF	25V	CM32X5R226M25AB	Kyocera
	≤ 12.5V	10μF	25V	CM316X5R106K25ABH	Kyocera
	all	10μF	50V	UMK325BJ106MM-T	Taiyo Yuden

C_{BST}	V_{OUT}	Cap.	Spec.	Part Name	Manufacturer
	all	0.47μF	16V	EMK212BJ474KD-T	Taiyo Yuden
	all	0.47μF	16V	C1608JB1C474K	TDK

D	V_{IN}	Spec.	Part Name	Manufacturer
	≤ 15V	15V 2A	SBS010M	SANYO
	≤ 15V	15V 2A	SS20015M	SANYO
	all	40V 3A	CMS16	TOSHIBA

L	Ind.	Spec.	Part Name	Manufacturer
	2.2μH	5.4A	RLF7030T-2R2M5R4	TDK
	4.7μH	3.4A	RLF7030T-4R7M3R4	TDK
	10μH	2.5A	SLF10145T-100M2R5	TDK
	2.2μH	2.7A	NR6020T2R2N	Taiyo Yuden
	4.7μH	2.6A	NR6028T4R7M	Taiyo Yuden
	10μH	2.5A	NR6045T100M	Taiyo Yuden

Soft Start Time Adjustment Function

The soft start time (t_{SS}) of the R1243x Series is adjustable by adding the soft start time adjusting capacitor (C_{SS}) to the TSS pin. The soft start time can be set longer than the internal soft start time (Typ.0.4ms).

For example, if the soft start time adjusting capacitor (C_{SS}) is 0.1µF, the externally adjusted soft start time will be 12ms (Typ.). If there is no need of adjusting the soft start time, leave TSS pin as open so that the internal soft start time (Typ.0.4ms) will be applied.

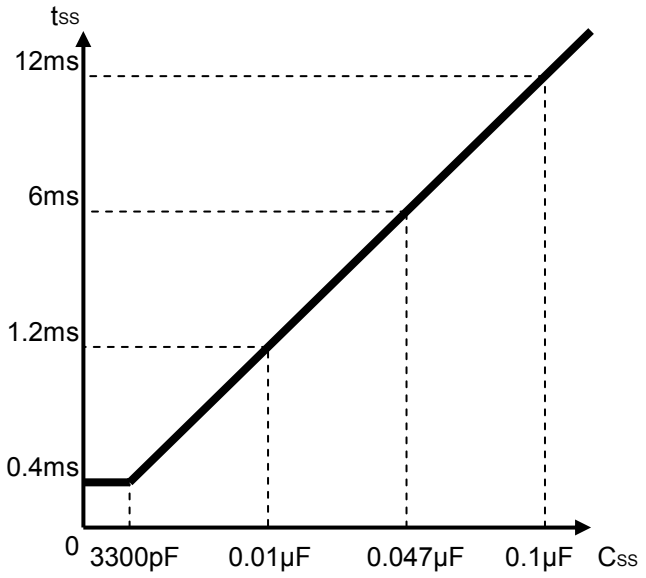


Fig.1 C_{SS} vs t_{SS}(Typ.)

FLAG Function

The R1243 Series has the flag output function by using the Nch open drain. If any abnormal condition is detected, the IC turns the Nch transistor on and turns the FLG pin low. If the condition returns to normal, the IC turns the Nch transistor off and turns the FLG pin high after the flag off delay time (Typ.0.25ms).

The followings are the abnormal conditions the IC can detect.

·CE="L" (Shut down) ·UVLO (Released voltage Typ.4.0V) ·Thermal Shutdown
·V_{FB} Over Voltage Detection (Typ.0.6V) ·V_{FB} Under Voltage Detection (Typ.0.4V)
·Active Latch function (Ver.A/C)
·T_{SS} pin's Over Voltage Protection after the completion of soft start (Typ.3V)

The flag resistors (R_{FLG}) have to be between 10kΩ to 100kΩ. If the flag function is not used, FLG pin has to be left open or connected to GND.

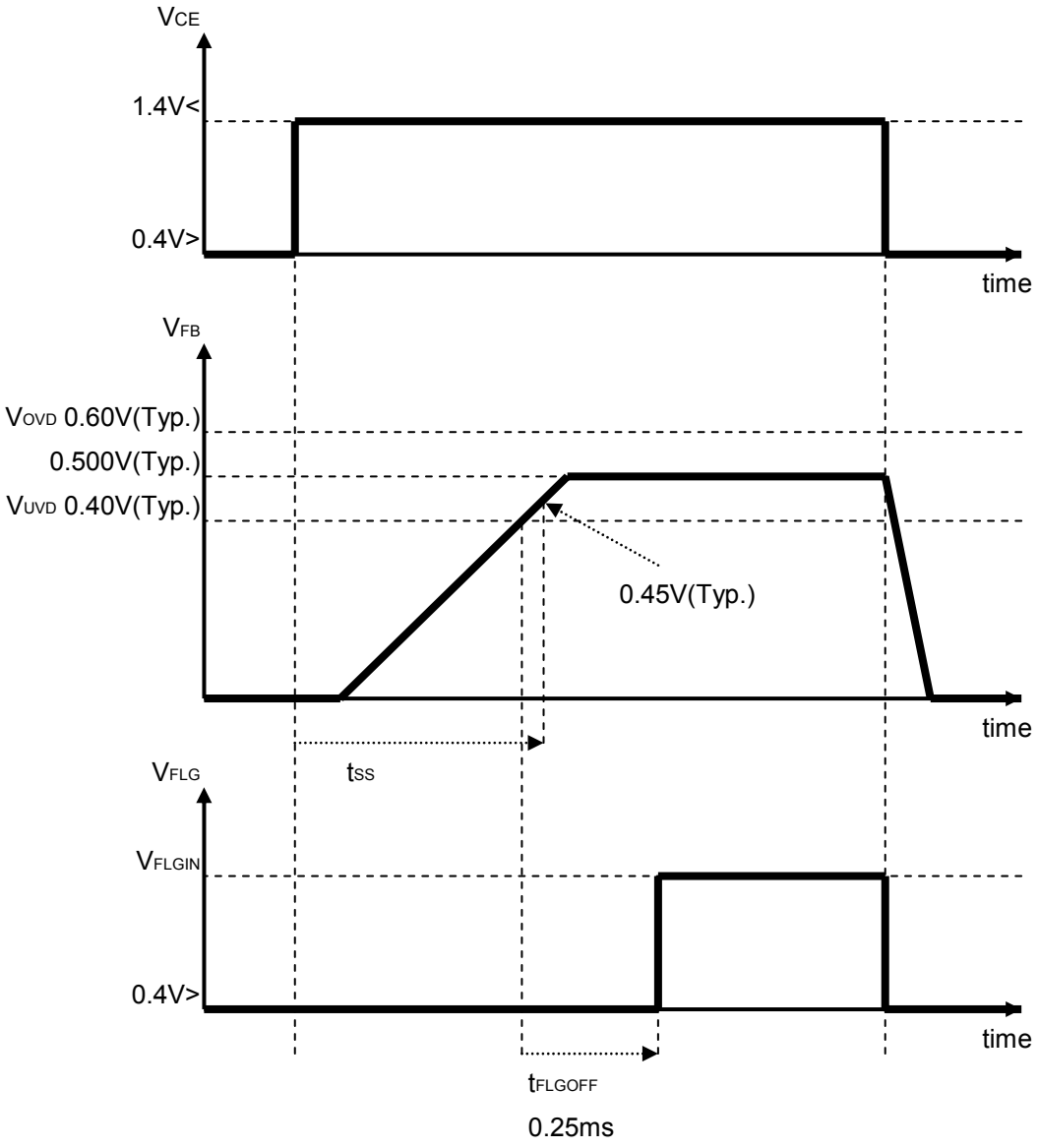
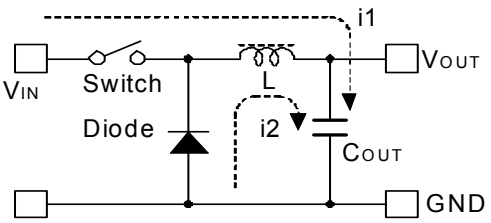


Fig.2 FLAG function sequence

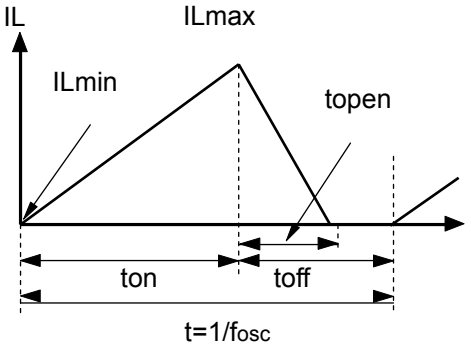
Operation of The Buck Converter and The Output Current

The DC/DC converter charges energy in the inductor when switch is ON, and discharges the energy from the inductor when switch is OFF and controls with less energy loss, so that a lower output voltage than the input voltage is obtained. The operation will be explained with reference to the following diagrams:

< Basic Circuits >



< Current through >



Step 1: Switch turns on and current IL (=i1) flows, and energy is charged into C_{OUT}. At this moment, IL increases from IL_{min} (=0) to reach IL_{max} in proportion to the on-time period (t_{on}) of Switch.

Step 2: When Switch turns off, a rectifier Diode turns on in order that L maintains IL at IL_{max}, and current IL (=i2) flows.

Step 3: IL (=i2) decreases gradually and reaches $IL=IL_{min}=0$ after a time period of t_{open}, and Diode turns off. Provided that in the continuous mode, next cycle starts before IL becomes to 0 because t_{off} time is not enough. In this case, IL value increases from this IL_{min} (>0).

In the case of PWM control system, the output voltage is maintained by controlling the on-time period (t_{on}), with the oscillator frequency (f_{osc}) being maintained constant.

Output Current and Selection of External Components

The relation between the output current and external components is as follows:

When Switch of L_X is ON:

(Wherein, Ripple Current P-P value is described as I_{RP}, ON resistance of Switch and Diode of L_X are respectively described as R_{ONH} and V_F and the DC resistor of the inductor is described as R_L.)

$$V_{IN} = V_{OUT} + (R_{ONH} + R_L) \times I_{OUT} + L \times I_{RP} / t_{on} \quad \text{Equation 1}$$

When Switch is "OFF"(Diode is "ON") as t_{off}:

$$L \times I_{RP} / t_{off} = V_F + V_{OUT} + R_L \times I_{OUT} \quad \text{Equation 2}$$

Put Equation 2 to Equation 1 and solve for ON duty of Switch, $t_{on} / (t_{off} + t_{on}) = D_{ON}$,

$$D_{ON} = (V_{OUT} + V_F + R_L \times I_{OUT}) / (V_{IN} + V_F - R_{ONH} \times I_{OUT}) \quad \text{Equation 3}$$

Ripple Current is as follows:

$$I_{RP} = (V_{IN} - V_{OUT} - R_{ONH} \times I_{OUT} - R_L \times I_{OUT}) \times D_{ON} / f_{OSC} / L \quad \text{Equation 4}$$

The peak current (I_{Lmax}) passing through the inductor and the switch is obtained by the following equation.

$$I_{Lmax} = I_{OUT} + I_{RP} / 2 \quad \text{Equation 5}$$

The valley Current (I_{Lmin}) is obtained by the following equation.

$$I_{Lmin} = I_{OUT} - I_{RP} / 2 \quad \text{Equation 6}$$

If the valley current is smaller than 0 ($I_{Lmin}<0$), the step-down DC/DC converter enters the discontinuous current mode.

The current condition for the discontinuous current mode is as follows.

$$I_{OUT} < I_{RP} / 2 \quad \text{Equation 7}$$

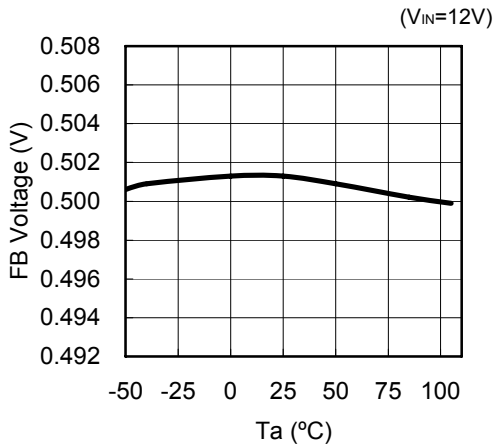
It is important to note the peak current (I_{Lmax}) and the valley current (I_{Lmin}) when making the input/output conditions or selecting the external components.

*The above explanation is based on the ideal operation of the continuous mode.

TYPICAL CHARACTERISTICS

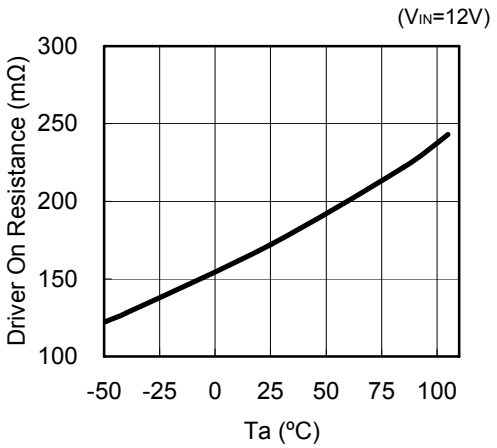
1) FB Voltage vs Temperature

R1243x001x



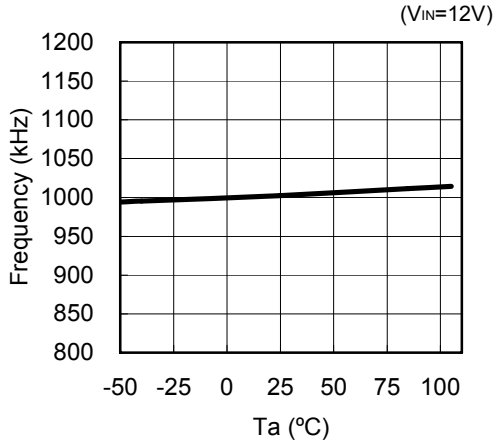
2) Driver On Resistance vs Temperature

R1243x001x



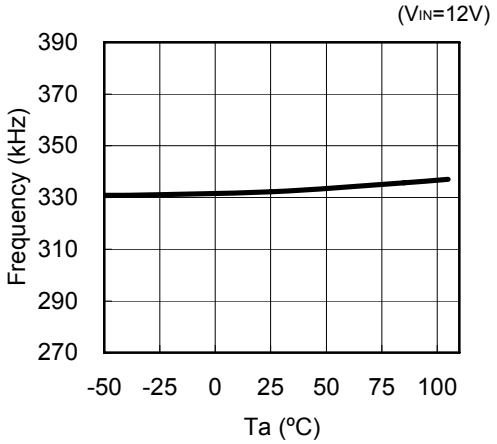
3) Oscillator Frequency vs Temperature

R1243x001A/R1243x001B



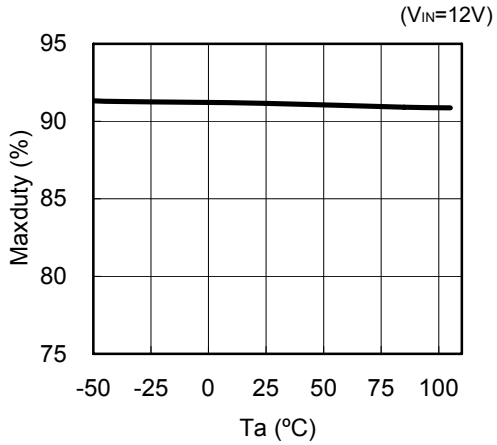
4) Oscillator Frequency vs Temperature

R1243x001C/R1243x001D



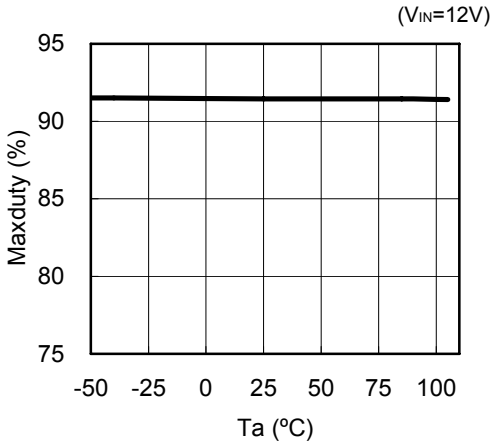
5) Maxduty vs Temperature

R1243x001A/R1243x001B



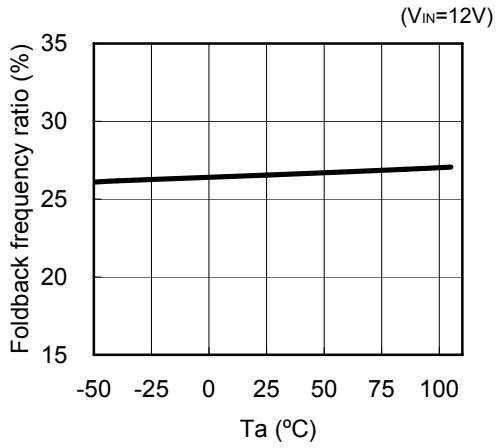
6) Maxduty vs Temperature

R1243x001C/R1243x001D



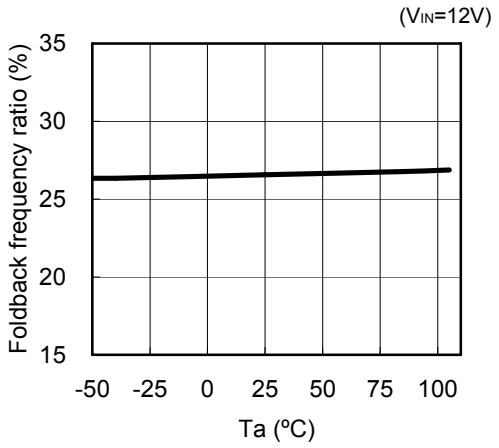
7) Foldback Frequency vs Temperature

R1243x001A/R1243x001B



8) Foldback Frequency vs Temperature

R1243x001C/R1243x001D

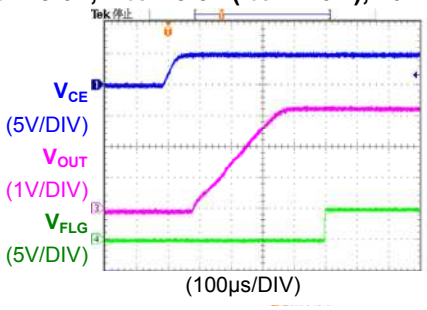


9) Soft Start Waveform

R1243x001x

tSS=0.4ms

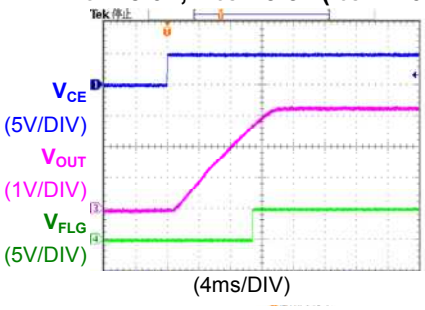
(R1243S001A, VIN=12V, VOUT=3.3V, tSS=open, VFLGIN=5.0V, ROUT=3.3Ω(IOUT=1.0A), Ta=25ºC)



R1243x001x

tSS=12ms

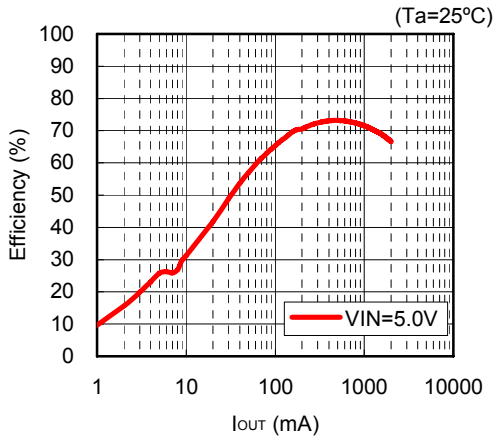
(R1243S001A, VIN=12V, VOUT=3.3V, CSS=0.1µF, VFLGIN=5.0V, ROUT=3.3Ω(IOUT=1.0A), Ta=25ºC)



10) Efficiency vs Load Current

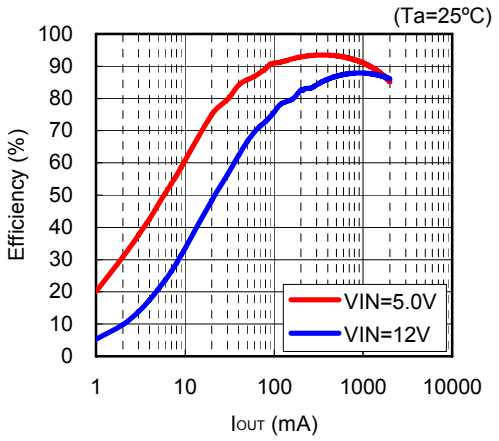
R1243x001A/B

VOUT=0.8V

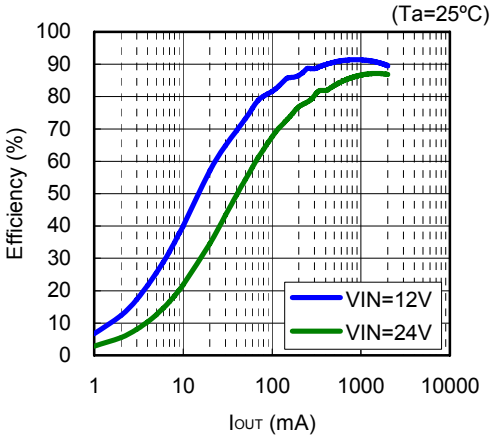


R1243x001A/B

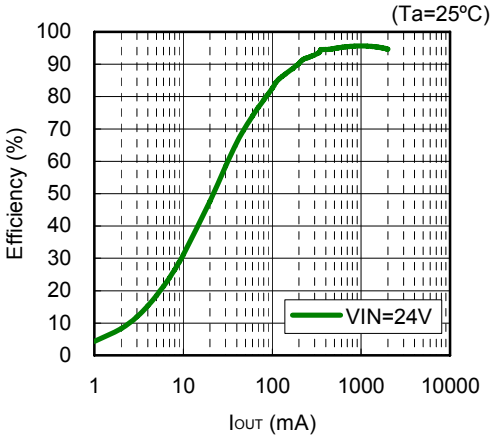
VOUT=3.3V



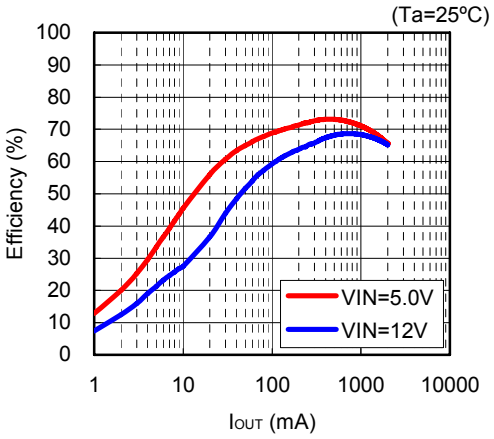
R1243x001A/B
V_{OUT}=5.0V



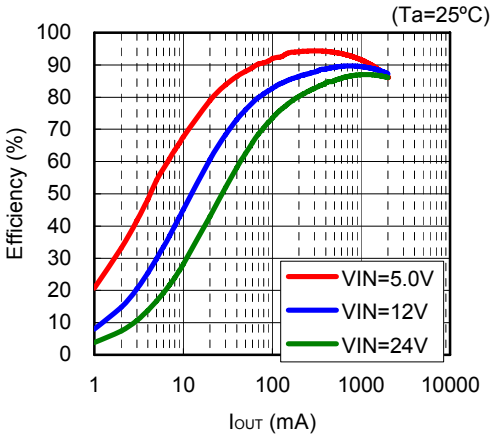
R1243x001A/B
V_{OUT}=18V



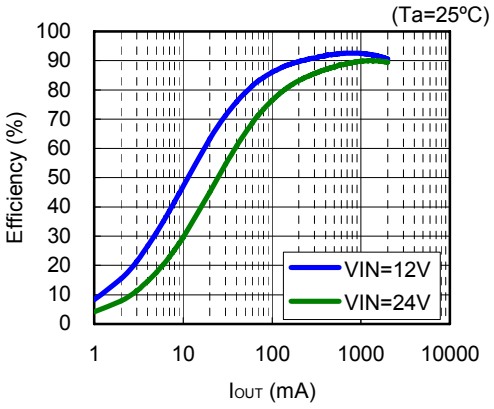
R1243x001C/D
V_{OUT}=0.8V



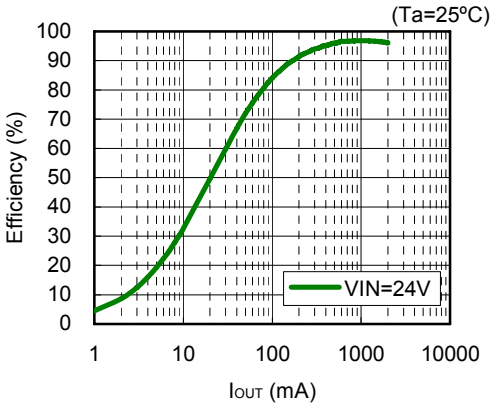
R1243x001C/D
V_{OUT}=3.3V



R1243x001C/D
V_{OUT}=5.0V



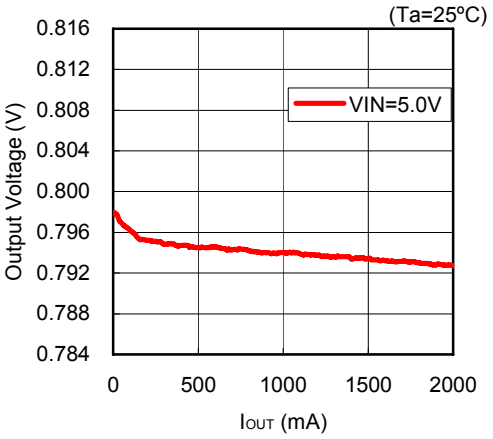
R1243x001C/D
V_{OUT}=18V



11) Load Regulation

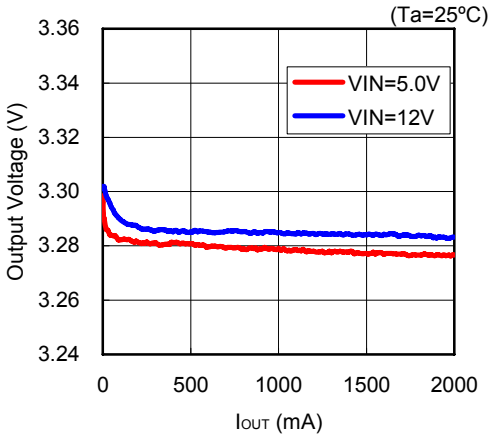
R1243x001A/B

V_{OUT}=0.8V



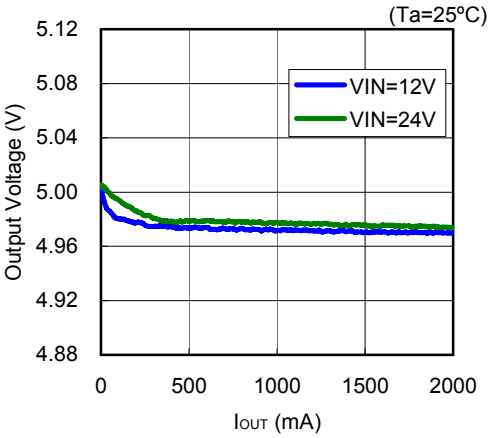
R1243x001A/B

V_{OUT}=3.3V



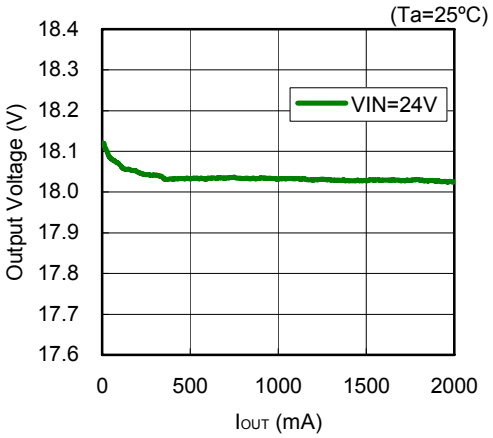
R1243x001A/B

V_{OUT}=5.0V



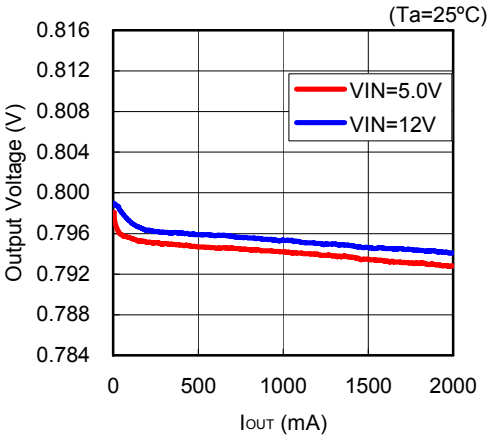
R1243x001A/B

V_{OUT}=18V



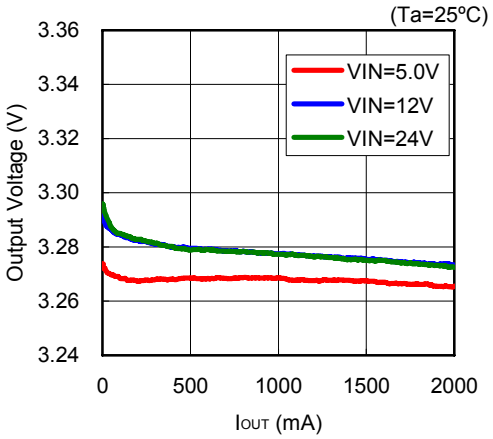
R1243x001C/D

V_{OUT}=0.8V



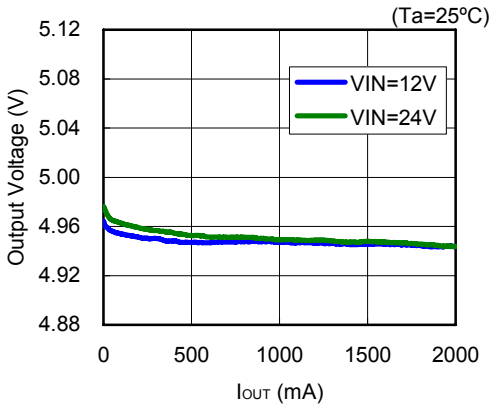
R1243x001C/D

V_{OUT}=3.3V



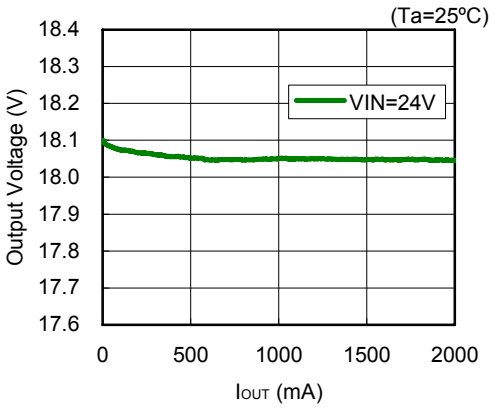
R1243x001C/D

V_{OUT}=5.0V



R1243x001C/D

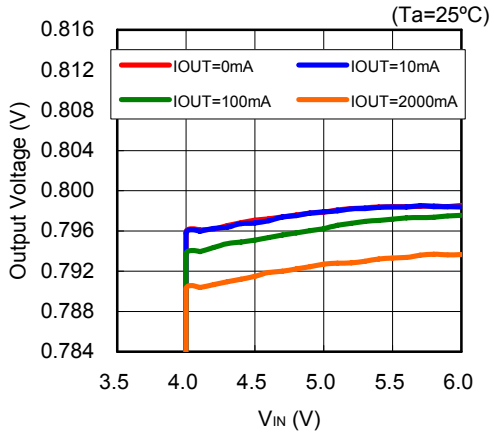
V_{OUT}=18V



12) Line Regulation

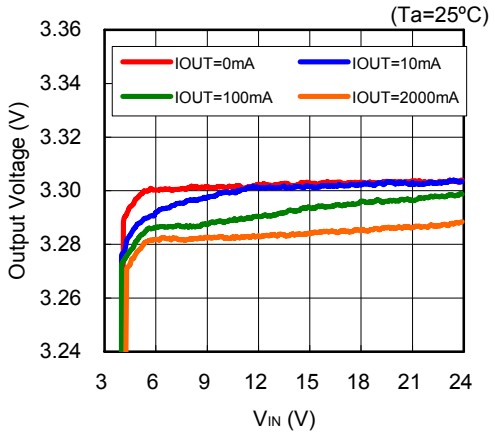
R1243x001A/B

V_{OUT}=0.8V



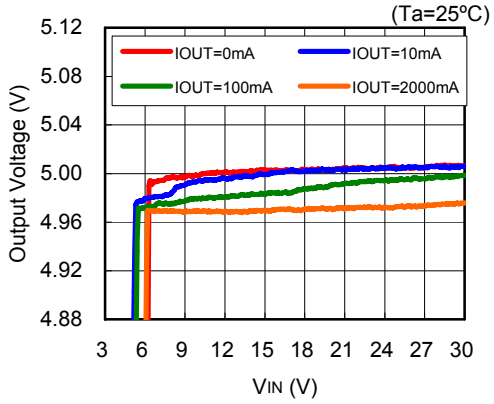
R1243x001A/B

V_{OUT}=3.3V



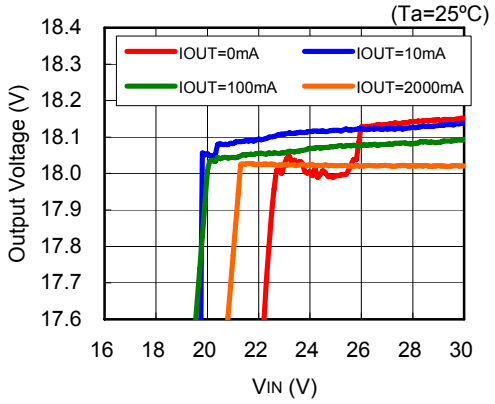
R1243x001A/B

V_{OUT}=5.0V



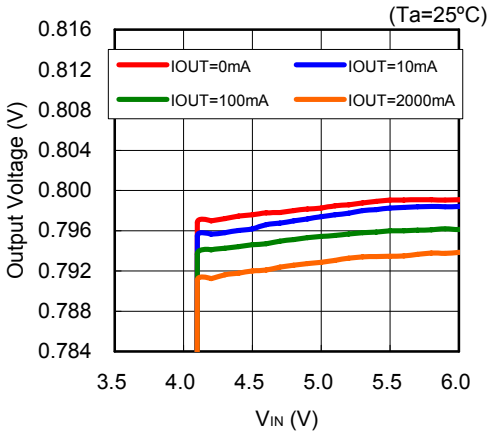
R1243x001A/B

V_{OUT}=18V



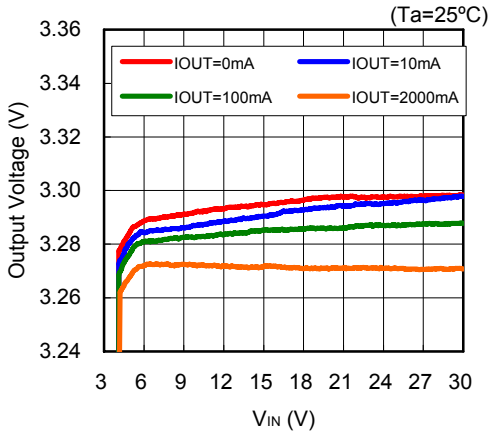
R1243x001C/D

V_{OUT}=0.8V



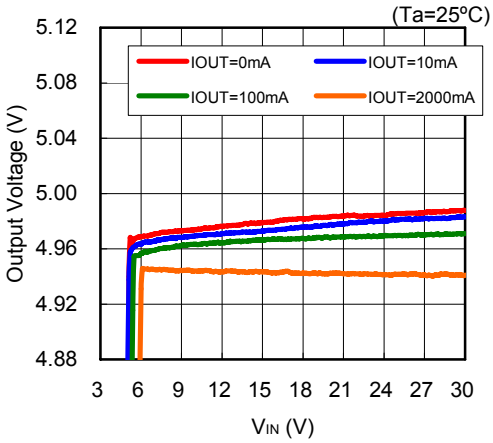
R1243x001C/D

V_{OUT}=3.3V



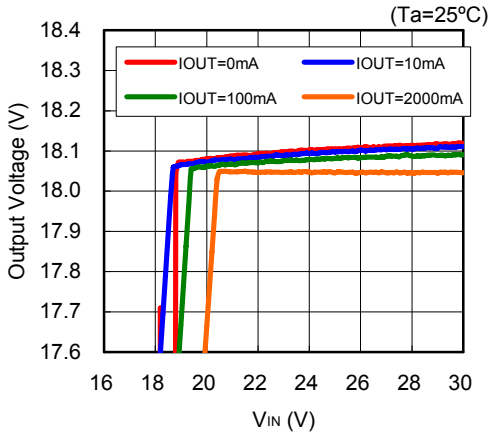
R1243x001C/D

V_{OUT}=5.0V



R1243x001C/D

V_{OUT}=18V



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RICOH COMPANY, LTD.
Electronic Devices Company
● Higashi-Shinagawa Office (International Sales)
3-32-3, Higashi-Shinagawa, Shinagawa-ku, Tokyo 140-8655, Japan
Phone: +81-3-5479-2857 Fax: +81-3-5479-0502

RICOH EUROPE (NETHERLANDS) B.V.
● Semiconductor Support Centre
Prof. W.H.Keesomlaan 1, 1183 DL Amstelveen, The Netherlands
P.O.Box 114, 1180 AC Amstelveen
Phone: +31-20-5474-309 Fax: +31-20-5474-791

RICOH ELECTRONIC DEVICES KOREA Co., Ltd.
11 floor, Haesung 1 building, 942, Daechidong, Gangnamgu, Seoul, Korea
Phone: +82-2-2135-5700 Fax: +82-2-2135-5705

RICOH ELECTRONIC DEVICES SHANGHAI Co., Ltd.
Room403, No.2 Building, 690#Bi Bo Road, Pu Dong New district, Shanghai 201203, People's Republic of China
Phone: +86-21-5027-3200 Fax: +86-21-5027-3299

RICOH COMPANY, LTD.
Electronic Devices Company
● Taipei office
Room109, 10F-1, No.51, Hengyang Rd., Taipei City, Taiwan (R.O.C.)
Phone: +886-2-2313-1621/1622 Fax: +886-2-2313-1623