

CXM3539XR

Description

The CXM3539XR is SP8T antenna switch for Triple bands GSM and Triple bands UMTS dual mode handsets. The CXM3539XR has a 1.8V CMOS compatible decoder. The Sony GaAs junction gate pHEMT (JPHEMT) MMIC process is used for low insertion loss and high linearity. (Applications: Triple bands GSM/Triple bands UMTS Dual Mode Handsets)

Features

- ◆ Low Insertion Loss: 0.30dB (Typ.) Tx1 (GSM Low Band Tx)
0.45dB (Typ.) Tx2 (GSM High Band Tx)
0.60dB (Typ.) TRx1 (UMTS Band I)
- ◆ Low Voltage Operation: $V_{DD} = 2.5V$
- ◆ No DC Blocking Capacitors
- ◆ Small package size: XQFN-24P (2.2mm × 2.9mm × 0.4mm Max.)
- ◆ Lead-Free and RoHS Compliant

Structure

GaAs Junction Gate pHEMT (JPHEMT) MMIC Switch, CMOS Decoder

Absolute Maximum Ratings

($T_a = 25^{\circ}C$)

◆ Bias voltage (V_{DD})	4	V
◆ Control voltage (CTL-A/B/C/D)	4	V
◆ Input power max. (Tx1)	36	dBm (Duty cycle = 12.5 to 50%)
◆ Input power max. (Tx2)	34	dBm (Duty cycle = 12.5 to 50%)
◆ Input power max. (TRx1, 2, 3)	32	dBm
◆ Input power max. (Rx1, 2, 4)	13	dBm
◆ Operating temperature range	-35 to +85	°C
◆ Storage temperature range	-65 to +150	°C

Note on Handling

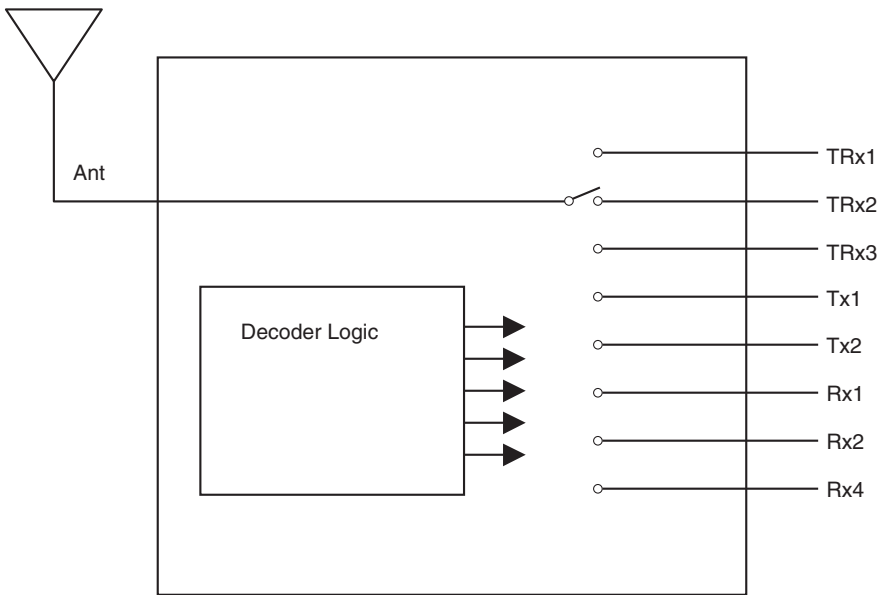
GaAs MMIC's are ESD sensitive devices. Special handling precautions are required.

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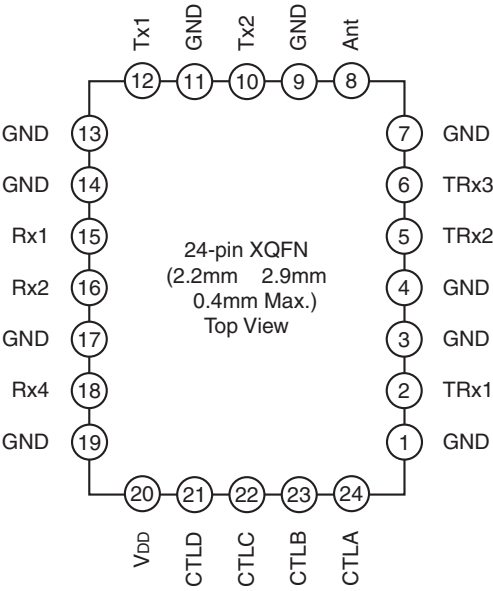


Block Diagram

SP8T Antenna Switch



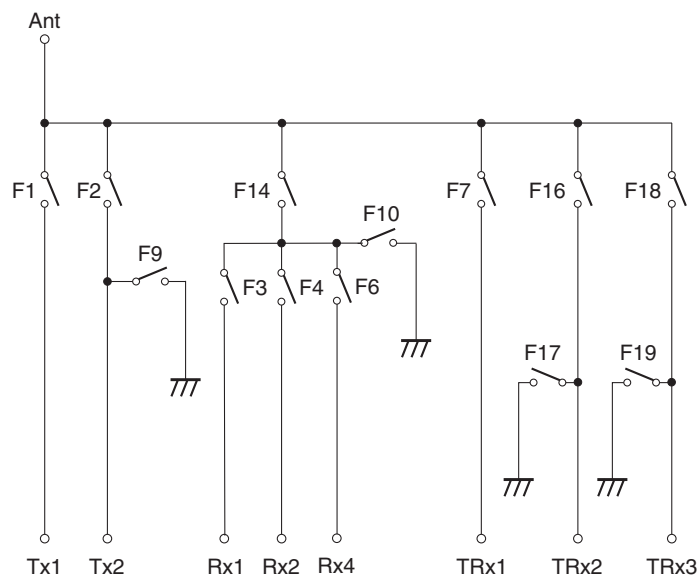
Pin Configuration



**Pin Description**

Pin No.	Name	Pin No.	Name
1	GND	13	GND
2	TRx1	14	GND
3	GND	15	Rx1
4	GND	16	Rx2
5	TRx2	17	GND
6	TRx3	18	Rx4
7	GND	19	GND
8	Ant	20	V _{DD}
9	GND	21	CTLD
10	Tx2 (DCS/PCS)	22	CTLG
11	GND	23	CTLB
12	Tx1 (GSM850/900M)	24	CTLA

RF Switch



Truth Table

State	Active Path	Vctl State				Switch State												
		A	B	C	D	F1	F2	F3	F4	F6	F7	F9	F10	F14	F16	F17	F18	F19
1	Tx1	H	H	L	H	H	L	L	L	L	L	H	H	L	L	H	L	H
2	Tx2	H	L	L	H	L	H	L	L	L	L	L	H	L	L	H	L	H
3	Rx1	L	L	L	H	L	L	H	L	L	L	H	L	H	L	H	L	H
4	Rx2	L	L	H	H	L	L	L	H	L	L	H	L	H	L	H	L	H
5	Rx4	L	H	H	H	L	L	L	L	H	L	H	L	H	L	H	L	H
6	TRx1	L	H	L	H	L	L	L	L	L	H	H	H	L	L	H	L	H
7	TRx2	H	L	H	H	L	L	L	L	L	L	H	H	L	H	L	L	H
8	TRx3	H	H	H	H	L	L	L	L	L	L	H	H	L	L	H	H	L
9	Sleep	L	L	L	L	—	—	—	—	—	—	—	—	—	—	—	—	—



Electrical Characteristics

Supply Voltage Value

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Bias voltage (V _{DD})	+2.5	+2.65	+3.3	V

Logic Value

(Ta = 25°C)

Item	State	Min.	Typ.	Max.	Unit
Control voltage (CTL-A/B/C/D)	High	+1.5	+1.8	+3.3	V
	Low	0	—	+0.3	

Specification 1(Ta = 25°C, V_{DD} = 2.5V, V_{ctl} = 1.5V)

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Insertion loss	IL	Ant-Tx1	*1	—	0.30	0.45	dB
		Ant-Tx2	*2	—	0.45	0.60	
		Ant-Rx1	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-Rx2	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-Rx4	*3	—	0.75	0.90	
			*4	—	1.00	1.15	
		Ant-TRx1	*5	—	0.55	0.70	
			*6	—	0.60	0.75	
		Ant-TRx2	*5	—	0.58	0.73	
			*6	—	0.63	0.78	
			*7	—	0.45	0.60	
			*8	—	0.45	0.60	
			*9	—	0.57	0.72	
			*10	—	0.60	0.75	
		Ant-TRx3	*5	—	0.60	0.75	
			*6	—	0.63	0.78	
			*7	—	0.45	0.60	
			*8	—	0.45	0.60	
			*9	—	0.60	0.75	
			*10	—	0.62	0.77	
VSWR	VSWR	All ports in Active Paths	824 to 2170MHz	—	1.20	1.50	—
Harmonics	2fo	Tx1-Ant	*1	—	−52	−36	dBm
	3fo			—	−40	−35	
	2fo	Tx2-Ant	*2	—	−52	−36	
	3fo			—	−38	−33	
	2fo	TRx1-Ant	*5	—	−53	−39	
	3fo			—	−54	−39	
	2fo	TRx2-Ant	*7, *9	—	−56	−39	
	3fo			—	−55	−39	
	2fo	TRx3-Ant	*7, *9	—	−56	−39	
	3fo			—	−53	−39	

Item	Symbol	Port	Condition	Min.	Typ.	Max.	Unit
Intermodulation distortion level in Rx band	IMD2	TRx1-Ant	*11, *19	—	−106	−97	dBm
		TRx2-Ant	*12, *19	—	−108	−97	
			*13, *19	—	−106	−97	
			*14, *19	—	−117	−97	
		TRx3-Ant	*12, *19	—	−106	−97	
			*13, *19	—	−105	−97	
			*14, *19	—	−116	−97	
	IMD3	TRx1-Ant	*15, *19	—	−105	−97	
		TRx2-Ant	*16, *19	—	−105	−97	
			*17, *19	—	−108	−97	
			*18, *19	—	−109	−97	
		TRx3-Ant	*16, *19	—	−104	−97	
			*17, *19	—	−107	−97	
			*18, *19	—	−108	−97	
Switching time	Ts		50%Ctl to 90%RF	—	3	5	μs
Control current	Ictl		Vctl = 1.80V	—	1	5	μA
Supply current	Idd		VDD = 2.65V	—	0.18	0.40	mA
Sleep current	Isleep		Sleep Mode *State9 VDD = 2.65V	—	1	10	μA

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

- *1 Pin on Tx1: 34dBm, 824 to 915MHz, Tx1 enabled
- *2 Pin on Tx2: 32dBm, 1710 to 1910MHz, Tx2 enabled
- *3 Pin on Ant: 10dBm, 869 to 960MHz, Rx1, Rx2 or Rx4 enabled
- *4 Pin on Ant: 10dBm, 1805 to 1990MHz, Rx1, Rx2 or Rx4 enabled
- *5 Pin on TRx1, TRx2 or TRx3: 26dBm, 1920 to 1980MHz, TRx1, TRx2 or TRx3 enabled
- *6 Pin on Ant: 10dBm, 2110 to 2170MHz, TRx1, TRx2 or TRx3 enabled
- *7 Pin on TRx2 or TRx3: 26dBm, 824 to 849MHz, TRx2 or TRx3 enabled
- *8 Pin on Ant: 10dBm, 869 to 894MHz, TRx2 or TRx3 enabled
- *9 Pin on TRx2 or TRx3: 26dBm, 1710 to 1910MHz, TRx2 or TRx3 enabled
- *10 Pin on Ant: 10dBm, 1805 to 1990MHz, TRx2 or TRx3 enabled
- *11 Pin on TRx1: 20dBm, 1950MHz, Pin on Ant: −15dBm, 190MHz, TRx1 enabled
- *12 Pin on TRx2 or TRx3: 20dBm, 1745MHz, Pin on Ant: −15dBm, 95MHz, TRx2 or TRx3 enabled
- *13 Pin on TRx2 or TRx3: 20dBm, 1880MHz, Pin on Ant: −15dBm, 80MHz, TRx2 or TRx3 enabled
- *14 Pin on TRx2 or TRx3: 20dBm, 835MHz, Pin on Ant: −15dBm, 45MHz, TRx2 or TRx3 enabled
- *15 Pin on TRx1: 20dBm, 1950MHz, Pin on Ant: −15dBm, 1760MHz, TRx1 enabled
- *16 Pin on TRx2 or TRx3: 20dBm, 1745MHz, Pin on Ant: −15dBm, 1650MHz, TRx2 or TRx3 enabled
- *17 Pin on TRx2 or TRx3: 20dBm, 1880MHz, Pin on Ant: −15dBm, 1800MHz, TRx2 or TRx3 enabled
- *18 Pin on TRx2 or TRx3: 20dBm, 835MHz, Pin on Ant: −15dBm, 790MHz, TRx2 or TRx3 enabled
- *19 Measured with the recommended circuit

Specification 1-Isolation(Ta = 25°C, V_{DD} = 2.5V, V_{ctl} = 1.5V)

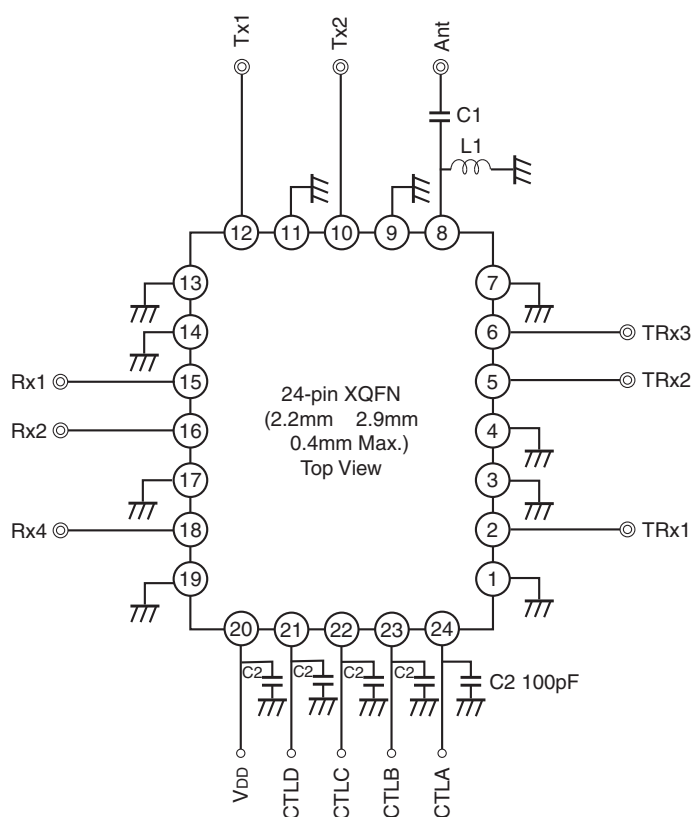
Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	Tx1	Tx1-Rx1	824 to 915MHz	35	46	—	dB
			Tx1-Rx2		35	55	—	
			Tx1-Rx4		35	57	—	
			Tx1-TRx1		25	29	—	
			Tx1-TRx2		25	48	—	
			Tx1-TRx3		25	38	—	
			Tx1-Tx2		25	28	—	
			Tx1-Tx2	1648 to 1830MHz	18	22	—	
		Tx2	Tx2-Rx1	1710 to 1910MHz	35	51	—	
			Tx2-Rx2		35	55	—	
			Tx2-Rx4		35	55	—	
			Tx2-TRx1		20	23	—	
			Tx2-TRx2		20	38	—	
			Tx2-TRx3		20	31	—	
			Tx2-Tx1		16	19	—	
		TRx1	TRx1-Rx1	1920 to 1980MHz	30	52	—	
			TRx1-Rx2		30	57	—	
			TRx1-Rx4		30	54	—	
			TRx1-TRx2		27	34	—	
			TRx1-TRx3		23	26	—	
			TRx1-Tx1		17	19.5	—	
			TRx1-Tx2		20	28	—	
		TRx2	TRx2-Rx1	824 to 849MHz	30	59	—	
			TRx2-Rx2		30	60	—	
			TRx2-Rx4		30	60	—	
			TRx2-TRx1		20	28	—	
			TRx2-TRx3		20	28	—	
			TRx2-Tx1		20	26	—	
			TRx2-Tx2		20	43	—	
			TRx2-Rx1	1710 to 1910MHz	30	52	—	
			TRx2-Rx2		30	57	—	
			TRx2-Rx4		30	56	—	
			TRx2-TRx1		18	21	—	
			TRx2-TRx3		18	20.5	—	
			TRx2-Tx1		17	19.5	—	
			TRx2-Tx2		20	33	—	

Item	Symbol	Path		Condition	Min.	Typ.	Max.	Unit
		Active	Isolation					
Isolation	ISO	TRx3	TRx3-Rx1	824 to 849MHz	30	59	—	dB
			TRx3-Rx2		30	60	—	
			TRx3-Rx4		30	59	—	
			TRx3-TRx1		20	29	—	
			TRx3-TRx2		20	30	—	
			TRx3-Tx1		20	26	—	
			TRx3-Tx2		20	43	—	
			TRx3-Rx1	1710 to 1910MHz	30	52	—	
			TRx3-Rx2		30	57	—	
			TRx3-Rx4		30	55	—	
			TRx3-TRx1		18	22	—	
			TRx3-TRx2		18	22	—	
			TRx3-Tx1		17	19.5	—	
			TRx3-Tx2		20	36	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.



Recommended Circuit



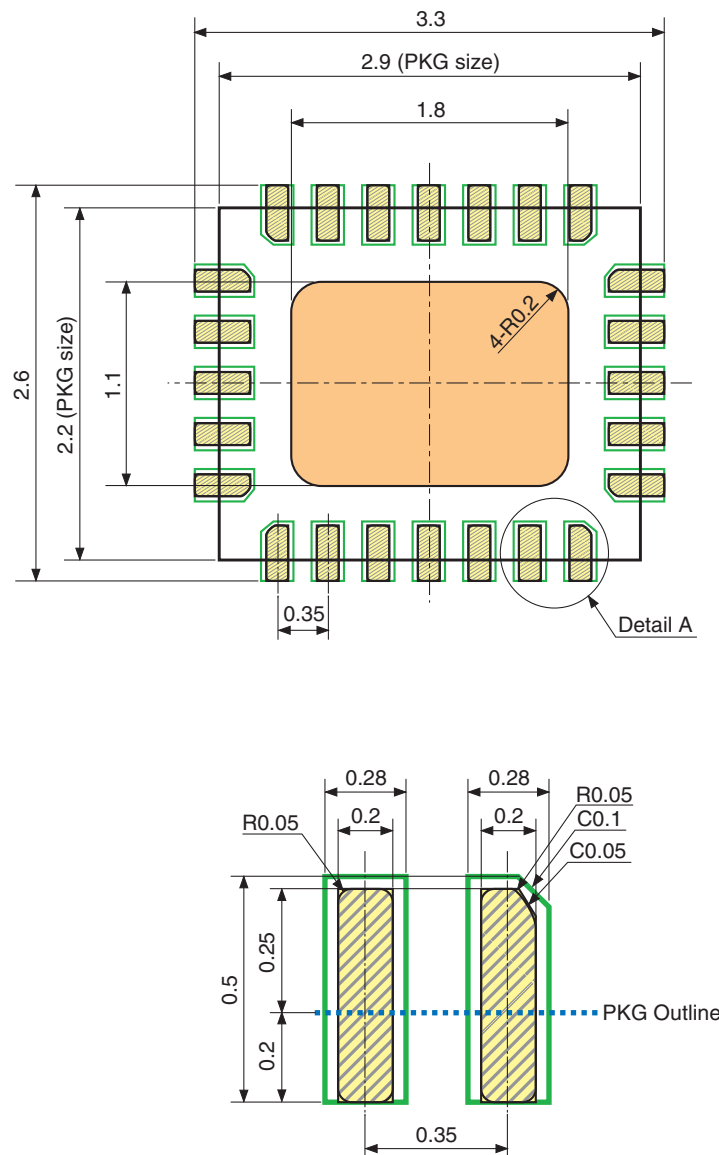
- Note)
1. No DC blocking Capacitors are required on all RF ports.
 2. DC levels of all RF ports are GND.
 3. L1 Inductor(22nH) and C1 Capacitor(22pF) are recommended on Ant port for ESD protection.
 4. C2 Capacitor (100pF) is recommended.

PCB Layout Template

XQFN-24P Macro for MMIC (Reference)

Specification

- PKG size: 2.9mm 2.2mm t0.35mm
- Terminal pitch: 0.35mm
- Terminal length: 0.25mm
- Mask thickness: 0.11mm

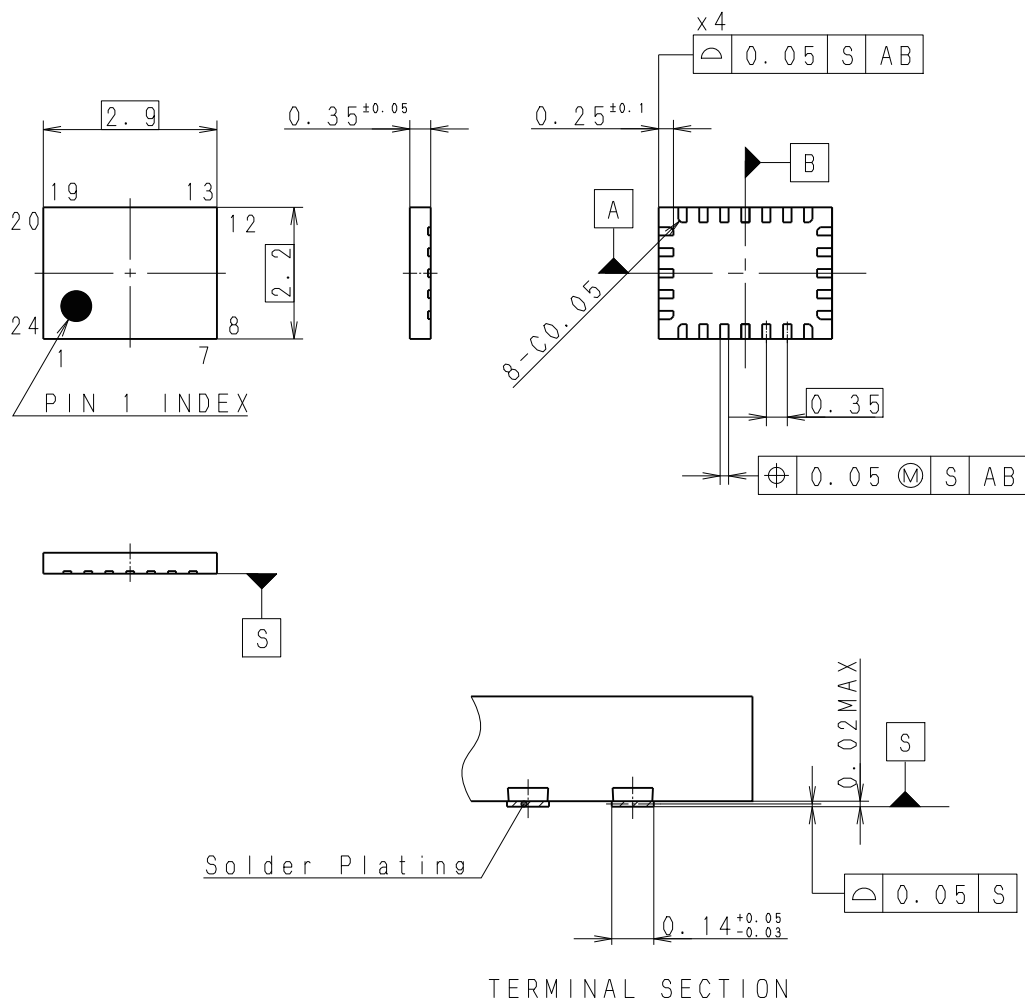


Detail A

- | | |
|--|---|
|  : Land area |  : Mask open area (Solder printing area) |
|  : Board resist open area |  : Metal area in board (GND plane is recommended.) |
|  : PKG Outline | |

Product Code: 875340827

24PIN XQFN (PLASTIC)



Note: Terminal burr height 0.05mmMAX.

PACKAGE STRUCTURE

SONY CODE	XQFN-24P-051
JEITA CODE	_____
JEDEC CODE	_____

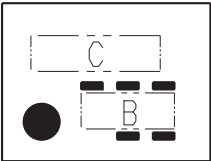
PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.006g

PART No. AP-2000-24XND2		Rev. 0
ISSUED 11. 12. 01	REVISED	
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.	
REMARKS PKG CODE : XR-24-AD		



Marking

Product Code: 875340827



MARKING C: 3539

注1) B部はロット番号 (Max 3文字で通し記号) を配置する。
(規定文字数未満につき省略は省略規定に従う。)

製造年は下記2進法ビット方式により表示する。)

a 部年コード (2進法ビット方式の1ビット目を表示) を配置する。

b 部年コード (2進法ビット方式の2ビット目を表示) を配置する。

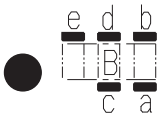
c 部年コード (2進法ビット方式の3ビット目を表示) を配置する。

d 部年コード (2進法ビット方式の4ビット目を表示) を配置する。

注2) C部は製品名 (Max 4文字) を配置する。

(4文字を超える場合は製品名省略標示規定に従う。)

注3) e部は組立場所表記を配置する。



DETAIL B

< INSTRUCTIONS >

1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.

(FOLLOW RULES FOR ABBREVIATIONS.

MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)

A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.

A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.

A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.

A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.

2) TYPE NO. (MAX 4 CHARACTERS) IN SECTION C.

(FOR MORE THAN 4 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

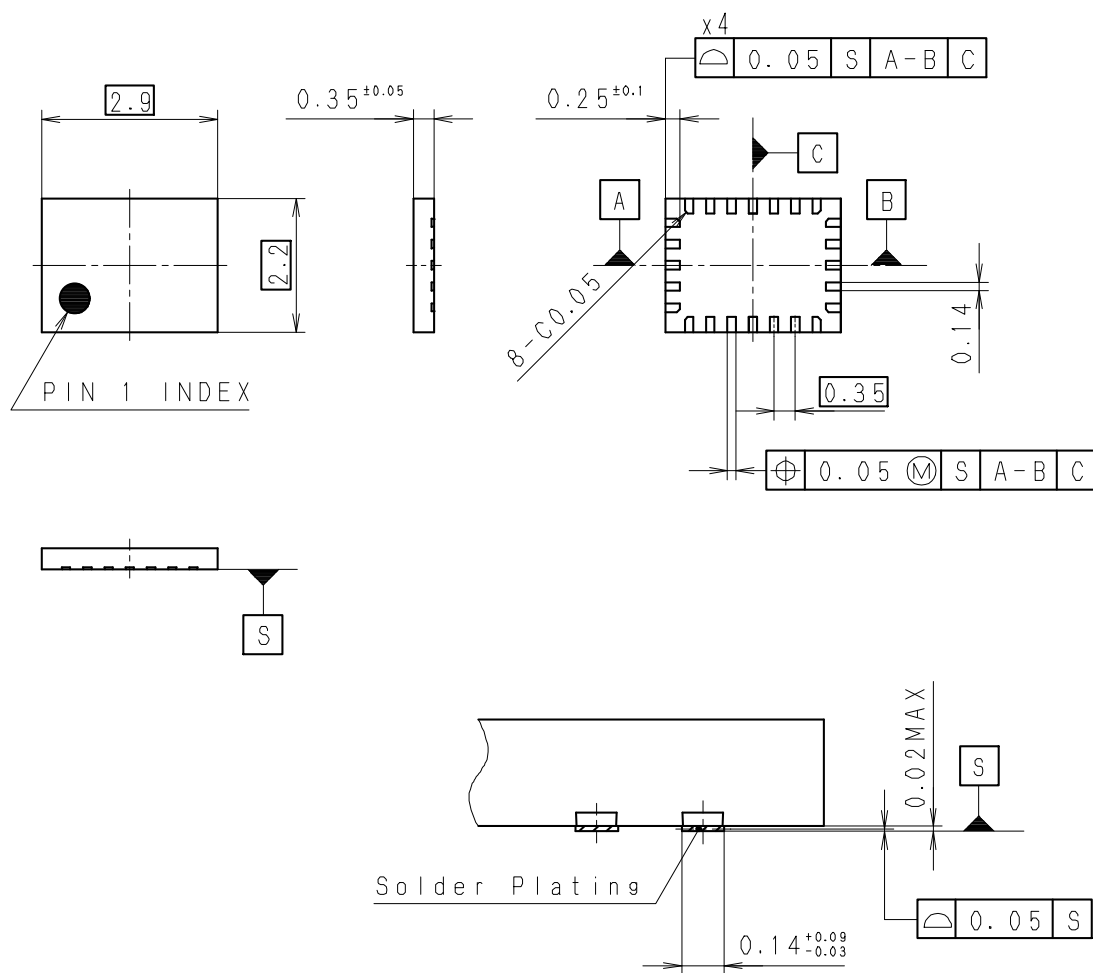
3) ASSEMBLY PLACE IN SECTION e.

Package Outline

(Unit: mm)

Product Code: 875332659

24PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-24P-02
JEITA CODE	_____
JEDEC CODE	_____

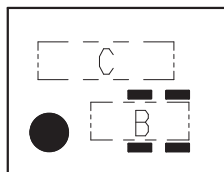
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
TERMINAL TREATMENT	SOLDER PLATING
TERMINAL MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

AP-4000-24046S Rev. 0

Marking

Product Code: 875332659



MARKING C: 3539

注1) B部はロット番号 (Max 3文字で通し記号) を配置する。

(規定文字数未滿につき省略は省略規定に従う。)

製造年は下記2進法ビット方式により表示する。)

a 部年コード (2進法ビット方式の1ビット目を表示) を配置する。

b 部年コード (2進法ビット方式の2ビット目を表示) を配置する。

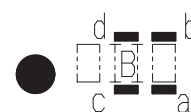
c 部年コード (2進法ビット方式の3ビット目を表示) を配置する。

d 部年コード (2進法ビット方式の4ビット目を表示) を配置する。

注2) C部は製品名 (Max 4文字) を配置する。

(4文字を超える場合は製品名省略標示規定に従う。)

注3) マーク深さは, Max 0.05 mmの事。



DETAIL B

< INSTRUCTIONS >

1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.

(FOLLOW RULES FOR ABBREVIATIONS.

MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)

A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION a.

A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION b.

A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION c.

A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT) IN SECTION d.

2) TYPE NO. (MAX 4 CHARACTERS) IN SECTION C.

(FOR MORE THAN 4 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

3) MARK DEPTH MAX 0.05 mm.