SONY

SP4T Antenna Switch for CDMA/UMTS

CXM3531XR

Description

The CXM3531XR is a high power SP4T antenna switch for CDMA/UMTS applications.
The antenna port can be routed to either of the 4TRx ports.
The low insertion loss on transmit means increased talk time as the Tx power amplifier can be operated at a lower output level.
Built-in decoder reduces component count and simplifies PCB layout by allowing direct connection of the switch to digital base band control lines with the 1.8V CMOS logic levels.
The Sony GaAs JPHEMT MMIC Process is used for low insertion loss and high linearity.
(Applications: CDMA/UMTS handsets)

Features

- ◆ Low insertion Loss (Tx): 0.28dB (Typ.) @27dBm (450MHz)
  0.30dB (Typ.) @27dBm (Cellular)
  0.36dB (Typ.) @27dBm (PCS)
  0.38dB (Typ.) @27dBm (IMT2000)
  0.45dB (Typ.) @27dBm (2.6GHz)
- ◆ High linearity: IIP3 = 70dBm
- ◆ No DC Blocking Capacitors required on RF ports.
- ◆ Lead-Free and RoHS Compliant

Package

Small package: 20pin XQFN (2.7mm × 2.7mm × 0.37mm Max.)

Structure

GaAs JPHEMT MMIC

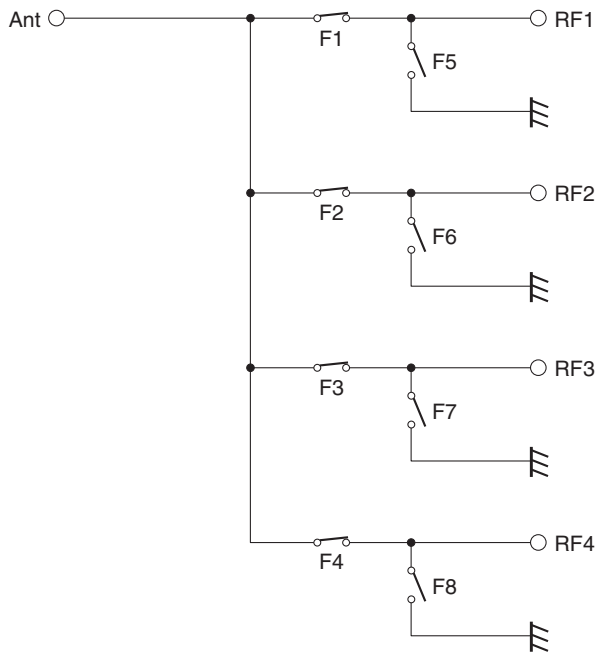
This IC is ESD sensitive device. Special handling precautions are required.

Absolute Maximum Ratings

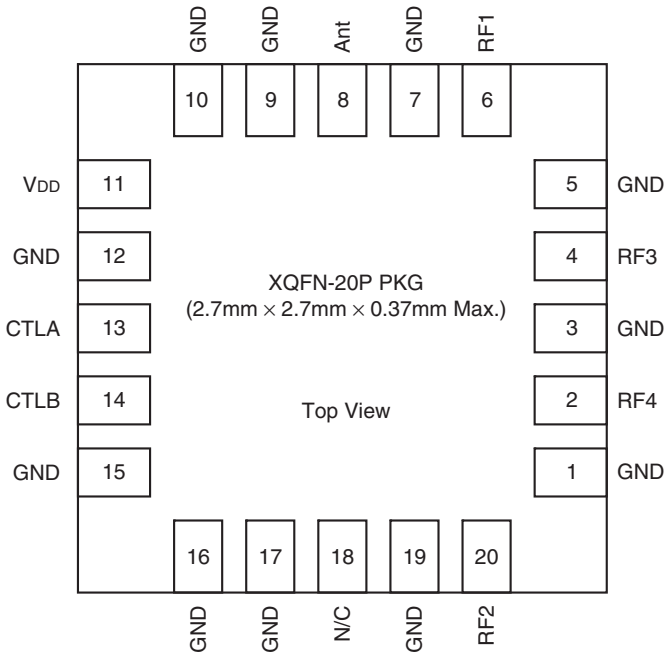
◆ Bias voltage	V_{DD}	4V (Ta = 25℃)
◆ Control voltage	Vctl	4V (Ta = 25℃)
◆ Input power Max. [Ant, RF1, RF2, RF3, RF4]		32dBm (410 to 2690MHz, Ta = 25℃)
◆ Operating temperature		–35 to +85℃
◆ Storage temperature		–65 to +150℃
◆ Maximum power dissipation	P_D	500mW *1

*1 25mm × 25mm × t:0.8mm Mounted on standard board (FR-4)

Block Diagram



Pin Configuration



Truth Table

ON Path	CTLA	CTLB	F1	F2	F3	F4	F5	F6	F7	F8
ANT – RF1	L	L	ON	OFF	OFF	OFF	OFF	ON	ON	ON
ANT – RF2	H	L	OFF	ON	OFF	OFF	ON	OFF	ON	ON
ANT – RF3	L	H	OFF	OFF	ON	OFF	ON	ON	OFF	ON
ANT – RF4	H	H	OFF	OFF	OFF	ON	ON	ON	ON	OFF

DC Bias Condition

(Ta = 25°C)

Item	Min.	Typ.	Max.	Unit
Vctl (H)	1.3	1.8	3.2	V
Vctl (L)	0	—	0.3	
V_{DD}	2.5	2.8	3.2	

Electrical Characteristics

Electrical Characteristics 1

(Ta = +25℃, V_{DD} = 2.8V, Vctl = 0/1.8V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	ANT-RF1	*1	—	0.28	0.43	dB
			*2	—	0.30	0.45	
			*3	—	0.36	0.51	
			*4	—	0.38	0.53	
			*5	—	0.45	0.60	
		ANT-RF2	*1	—	0.28	0.43	
			*2	—	0.30	0.45	
			*3	—	0.36	0.51	
			*4	—	0.38	0.53	
			*5	—	0.46	0.61	
		ANT-RF3	*1	—	0.25	0.40	
			*2	—	0.27	0.42	
			*3	—	0.33	0.48	
			*4	—	0.35	0.50	
			*5	—	0.42	0.57	
		ANT-RF4	*1	—	0.25	0.40	
			*2	—	0.27	0.42	
			*3	—	0.33	0.48	
			*4	—	0.35	0.50	
			*5	—	0.42	0.57	
Isolation	ISO.	ANT-RF1, 2, 3, 4	*1	30	41	—	dB
			*2	25	36	—	
			*3	22	27	—	
			*4	21	26	—	
			*5	18	23	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

*1 freq = 410 to 495MHz
*2 freq = 698 to 960MHz
*3 freq = 1710 to 1990MHz
*4 freq = 2110 to 2170MHz
*5 freq = 2500 to 2690MHz

Electrical Characteristics 2

(Ta = +25°C, V_{DD} = 2.8V, Vctl = 0/1.8V)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
VSWR	VSWR		410 to 2170MHz	—	1.1	1.4	—
			2500 to 2690MHz	—	1.3	1.7	
Harmonics	2fo	ANT-RF1, 2, 3, 4	*1	—	–68	–40	dBm
	3fo			—	–68	–40	
	2fo		*2	—	–66	–40	
	3fo			—	–66	–40	
	2fo		*3	—	–66	–40	
	3fo			—	–63	–40	
	2fo		*4	—	–66	–40	
	3fo			—	–63	–40	
	2fo		*5	—	–62	–40	
	3fo			—	–59	–40	
$P_{0.2dB}$ compression input power	$P_{0.2dB}$	ANT-RF1, 2, 3, 4	*1, *2, *3, *4, *5	31	—	—	dBm
Inter modulation product power in Rx band	IMD2	ANT-RF1, 2, 3, 4	*6-*9, *17	—	–110	–105	dBm
	IMD3		*10-*13, *17	—	–110	–105	
Input IP3	IIP3	ANT-RF1, 2, 3, 4	*14, *17	65	70	—	dBm
			*15, *17	65	70	—	
			*16, *17	65	70	—	
Control current	Ictl		Vctl = 1.8V	—	0.005	10	μA
Supply current	I_{DD}		V_{DD} = 2.8V	—	0.2	0.4	mA
Switching speed	Swt	RF1, 2, 3, 4	50% Ctl to 90% RF	—	2	5	μs

Electrical Characteristics are measured with all RF ports terminated in 50Ω.

*1 Pin = 27dBm, freq = 410 to 484MHz
*2 Pin = 27dBm, freq = 698 to 915MHz
*3 Pin = 27dBm, freq = 1710 to 1910MHz
*4 Pin = 27dBm, freq = 1920 to 1980MHz
*5 Pin = 27dBm, freq = 2500 to 2570MHz
*6 Pin on RF: 20dBm, 1950MHz, Pin on ANT: –15dBm, 190MHz
*7 Pin on RF: 20dBm, 1745MHz, Pin on ANT: –15dBm, 95MHz
*8 Pin on RF: 20dBm, 1880MHz, Pin on ANT: –15dBm, 80MHz
*9 Pin on RF: 20dBm, 835MHz, Pin on ANT: –15dBm, 45MHz
*10 Pin on RF: 20dBm, 1950MHz, Pin on ANT: –15dBm, 1760MHz
*11 Pin on RF: 20dBm, 1745MHz, Pin on ANT: –15dBm, 1650MHz
*12 Pin on RF: 20dBm, 1880MHz, Pin on ANT: –15dBm, 1800MHz
*13 Pin on RF: 20dBm, 835MHz, Pin on ANT: –15dBm, 790MHz
*14 Pin = 27 + 27dBm, 450 + 451MHz, IIP3 = (3 × Pout – IM3) / 2 + Loss
*15 Pin = 27 + 27dBm, 835 + 836MHz, IIP3 = (3 × Pout – IM3) / 2 + Loss
*16 Pin = 27 + 27dBm, 1950 + 1951MHz, IIP3 = (3 × Pout – IM3) / 2 + Loss
*17 Measured with the recommended circuit

Electrical Characteristics 3

(Ta = +25°C, V_{DD} = 2.8V, Vctl = 0/1.8V)

Item	Symbol	Path	Condition					Min.	Typ.	Max.	Unit
			P_{Tx} at RF*			Jammer at Ant –30dBm [MHz]	Triple beat product at RF* [MHz]				
			Pin [dBm]	PTx1 [MHz]	PTx2 [MHz]						
Triple beat ratio	TBR	ANT-RF1, RF2, RF3, RF4	21.5	835.5	836.5	881.5	881.5 ± 1	81	—	—	dBc
			21.5	1880	1881	1960	1960 ± 1	81	—	—	
			13.5	1732	1733	2132	2132 ± 1	81	—	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.
Measured with the recommended circuit

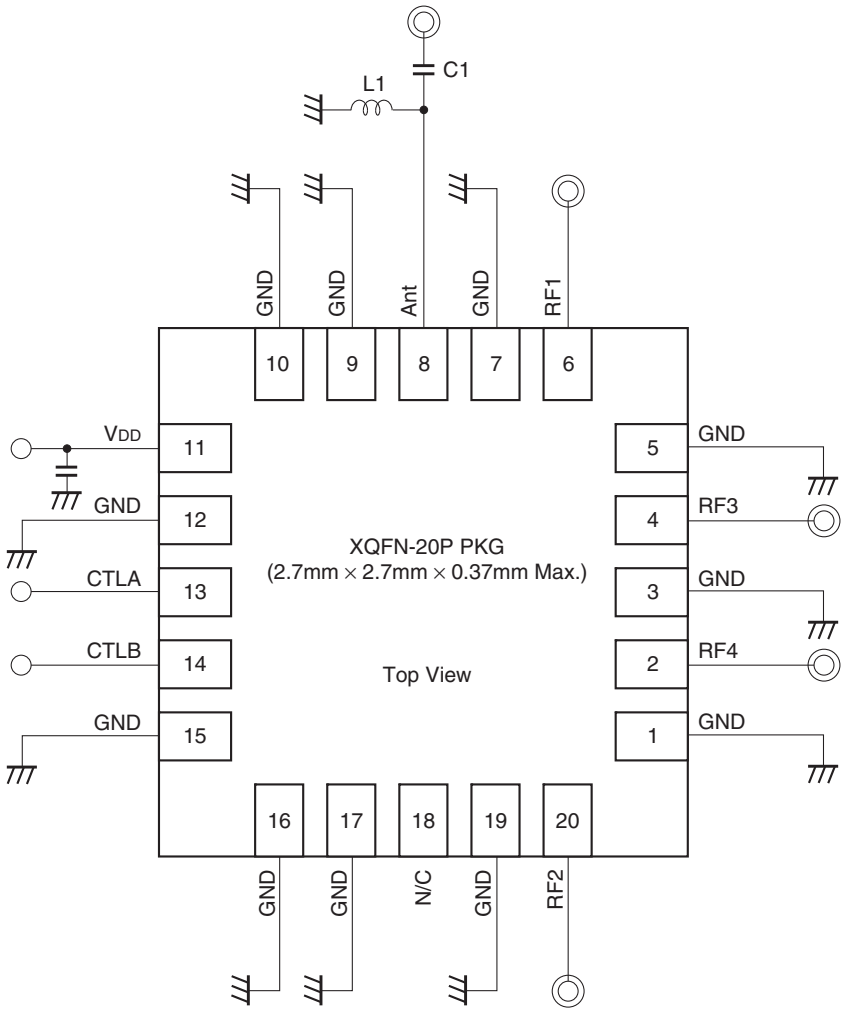
Electrical Characteristics 4

(Ta = +25°C, V_{DD} = 2.8V, Vctl = 0/1.8V)

Item	Symbol	Path	Condition			Min.	Typ.	Max.	Unit
			P_{Tx} at RF* 24dBm [MHz]	Jammer at ANT –20dBm [MHz]	IM2 product at RF* [MHz]				
Input IP2	IIP2	Ant-RF1, RF2, RF3, RF4	836.61	1718.61	881.61	113.5	—	—	dBm
			836.61	45	881.61	95.5	—	—	
			1885	3850	1965	95.5	—	—	
			1885	80	1965	95.5	—	—	
			1732.5	3865	2132.5	95.5	—	—	
			1732.5	400	2132.5	95.5	—	—	

Electrical Characteristics are measured with all RF ports terminated in 50Ω.
Measured with the recommended circuit

Recommended Circuit



Note) 1. No DC blocking capacitors are required on all RF ports.
2. DC levels of all RF ports are GND.
3. L1 (27nH) and C1 (12pF) are recommended on Ant port for ESD protection.

PCB Layout Template

XQFN-20P Macro (Reference)

- ◆ PKG size: □2.7mm × t0.35mm
- ◆ Terminal pitch: 0.4mm
- ◆ Terminal length: 0.4mm
- ◆ Mask thickness: 0.11mm

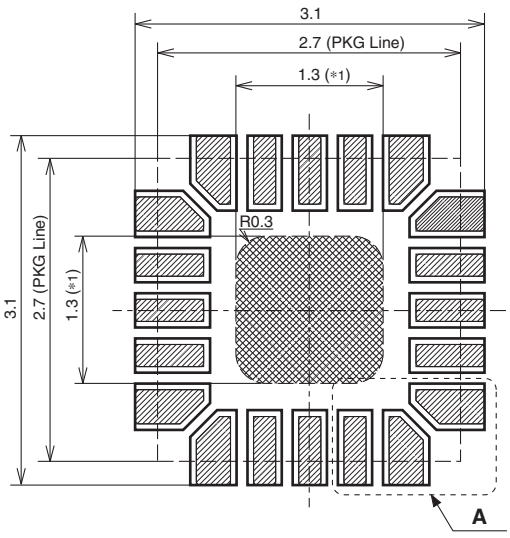
□ : Land area

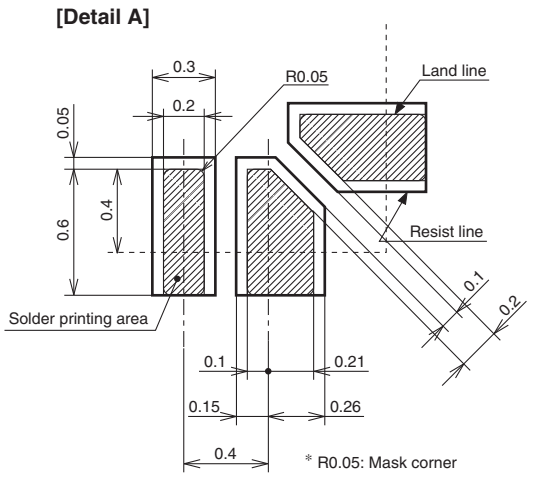
▨ : Mask open area (Solder printing area)

□ : Board resist open area

▩ : Metal area in board (*1)

*1 This metal is for heat loss reduction in package and recommend to connect to GND.



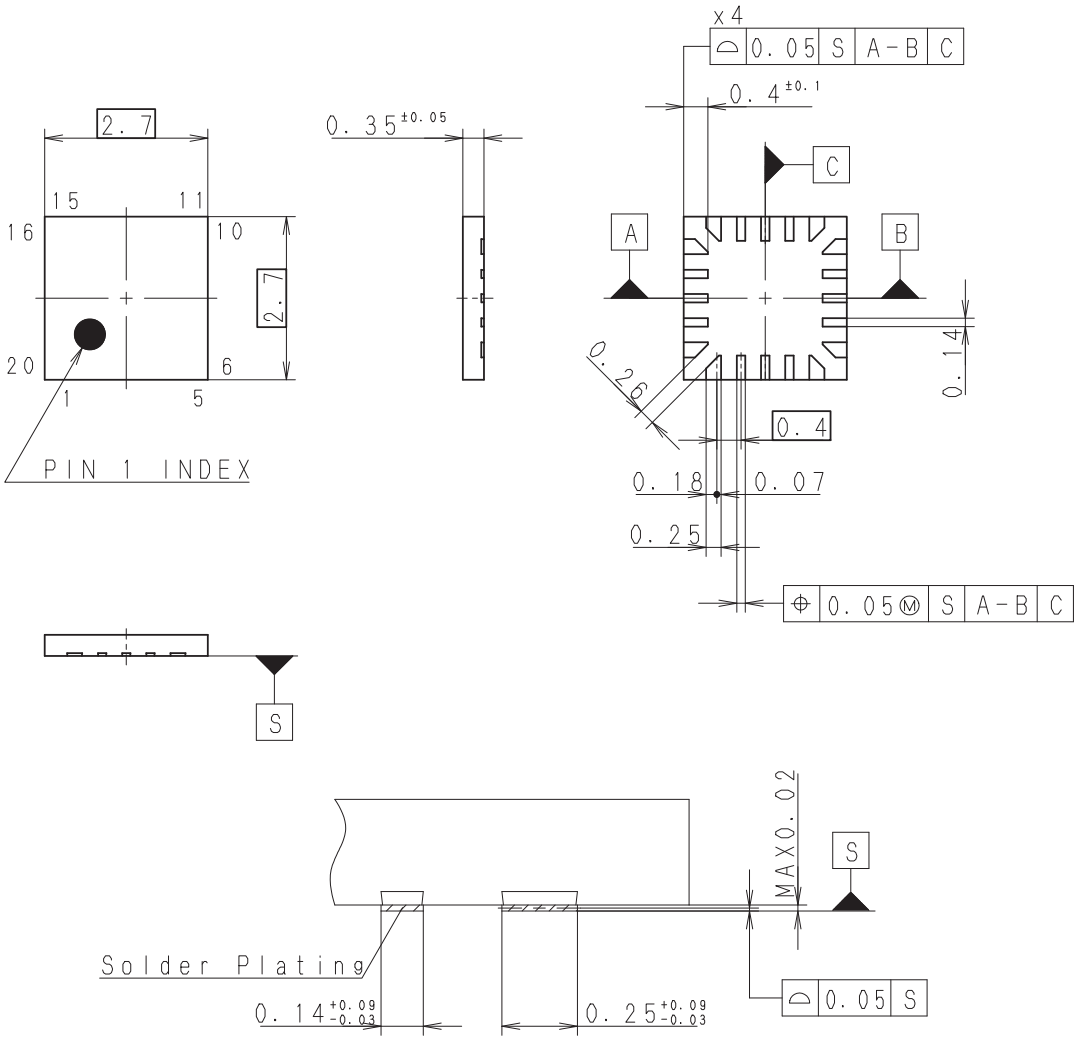


Package Outline

(Unit: mm)

Product Code: 875331306/875340928

20PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Cutting burr of lead are 0.05mm MAX.

SONY CODE	XQFN-20P-01
JEITA CODE	————
JEDEC CODE	————

PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

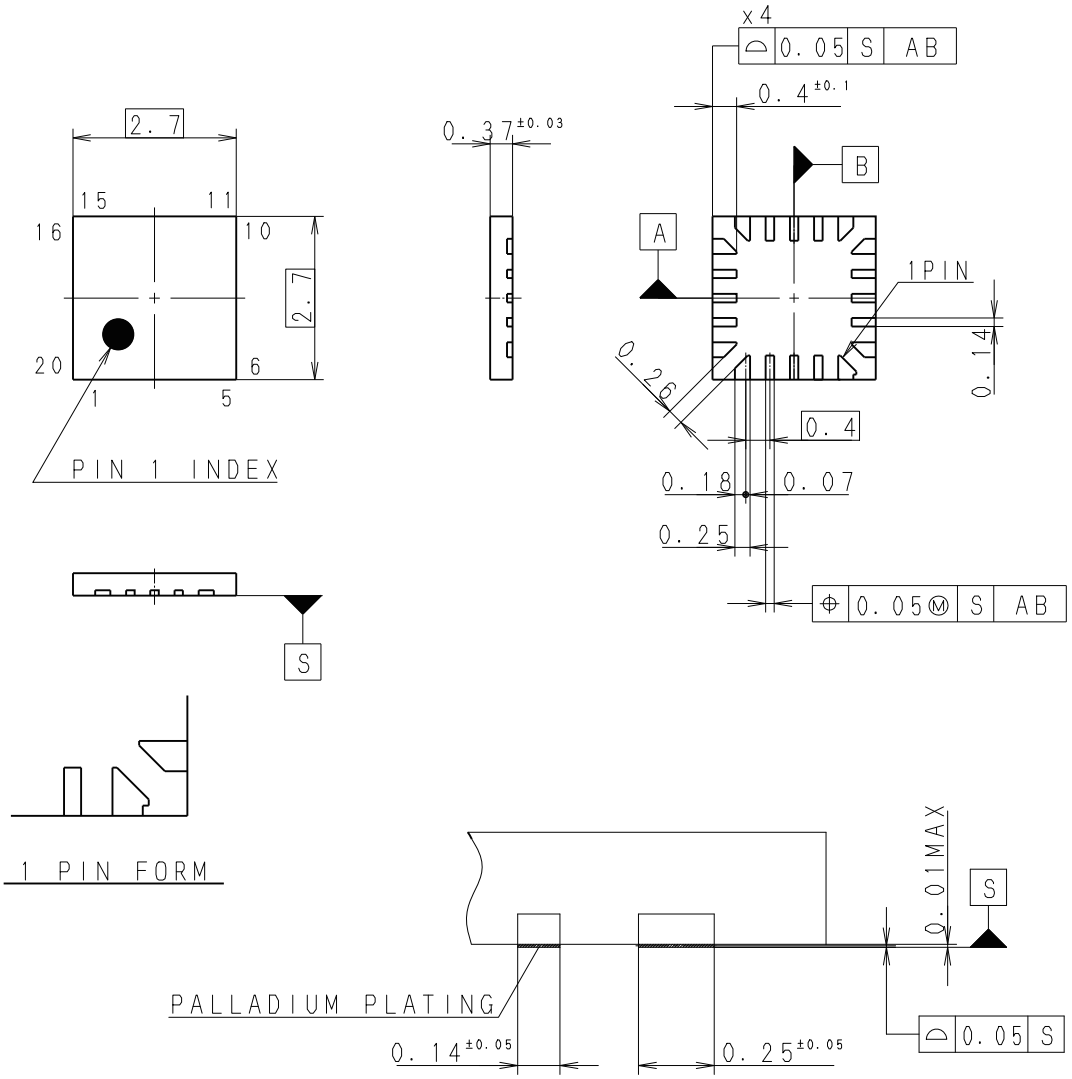
LEAD PLATING SPECIFICATIONS

ITEM	SPEC.
LEAD MATERIAL	COPPER ALLOY
SOLDER COMPOSITION	Sn-Bi Bi:1-4wt%
PLATING THICKNESS	5-18μm

(Unit: mm)

Product Code: 875340929

20PIN XQFN (PLASTIC)



TERMINAL SECTION

Note:Terminal burr height 0.05mm MAX.

SONY CODE	XQFN-20P-541
JEITA CODE	————
JEDEC CODE	————

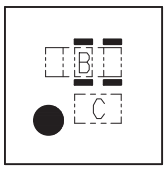
PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.01g

PART No. AP-2000-20XNBE1	Rev. 0
ISSUED 11.11.24	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKE CODE:XR-20-EBE	

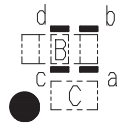
Marking

Product Code: 875331306
875340928



MARKING C: G4

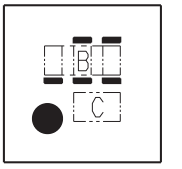
注1） B部はロット番号（Max3文字で通し記号）を配置する。
（規定文字数未満につき省略は省略規定に従う。
製造年は下記2進法ビット方式により表示する。）
a部年コード（2進法ビット方式の1ビット目を表示）を配置する。
b部年コード（2進法ビット方式の2ビット目を表示）を配置する。
c部年コード（2進法ビット方式の3ビット目を表示）を配置する。
d部年コード（2進法ビット方式の4ビット目を表示）を配置する。
注2） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
注3） マーク深さは，Max0．05mmの事。



DETAIL B

< INSTRUCTIONS >
1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
(FOLLOW RULES FOR ABBREVIATIONS.
MANUFACTURING YEAR IS DISPLAYED BY FOLLOWING BYNARY BIT SYSTEM.)
A YEAR CODE(THE 1ST BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION a.
A YEAR CODE(THE 2ND BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION b.
A YEAR CODE(THE 3RD BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION c.
A YEAR CODE(THE 4TH BIT OF A BINARY SYSTEM BIT SYSTEM IS DISPLAYED IN 1 DOT)IN SECTION d.
2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) MARK DEPTH MAX 0.05 mm.

Product Code: 875340929



MARKING C: G4

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（規定文字数未満につき省略は省略規定に従う。
製造年は下記2進法ビット方式により表示する。）
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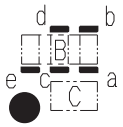
c部年コード（2進法ビット方式の3ビット目を表示）を配置する。
d部年コード（2進法ビット方式の4ビット目を表示）を配置する。
注2） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
注3） e部は組立場所表記を配置する。



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1) LOT NO. (MAX 3 CHARACTERS : SERIAL CODE) IN SECTION B.
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2) TYPE NO.(MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
3) ASSEMBLY PLACE IN SECTION e.