SONY

SPDT High Power SOI Antenna Switch

CXA4011GC

Description

The CXA4011GC is a SPDT antenna switch for GSM/3G/LTE switching applications.
The CXA4011GC has a 1.8V CMOS compatible decoder.
The Sony Silicon On Insulator (SOI) technology is used for low insertion loss.

Features

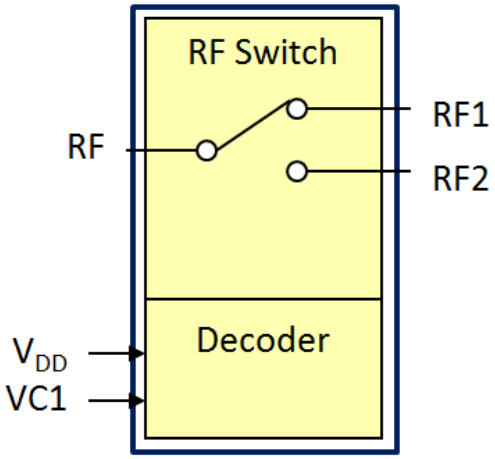
◆Low Insertion loss : 0.22 dB(typ.) at 800 MHz
0.23 dB(typ.) at 2 GHz
0.25 dB(typ.) at 2.7 GHz
◆No DC Blocking Capacitors (except sourcing DC bias)
◆Solder Bump Bare Die(SBBD) : Bump Pitch = 0.4 mm
◆Small Flip-Chip Size : 1.1 mm × 1.1 mm × 0.35 mm Typ.
◆Lead-Free and RoHS compliant
◆Applications: Diversity Switch, GSM/3G/LTE Tx Switch

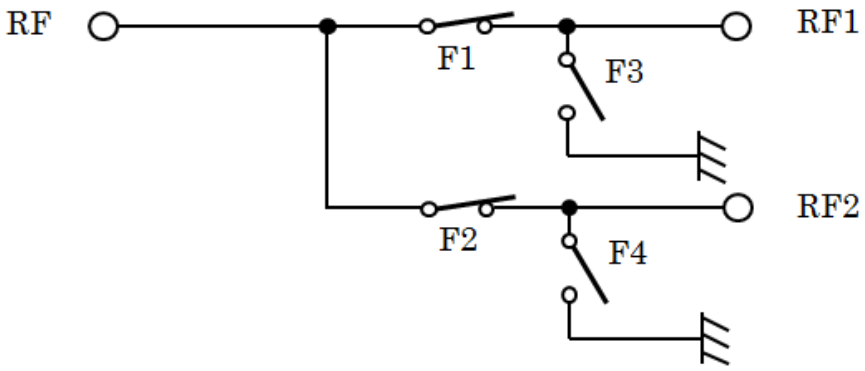
Structure

SOI CMOS MMIC

This IC is ESD sensitive device. Special handling precautions are required

Block Diagram



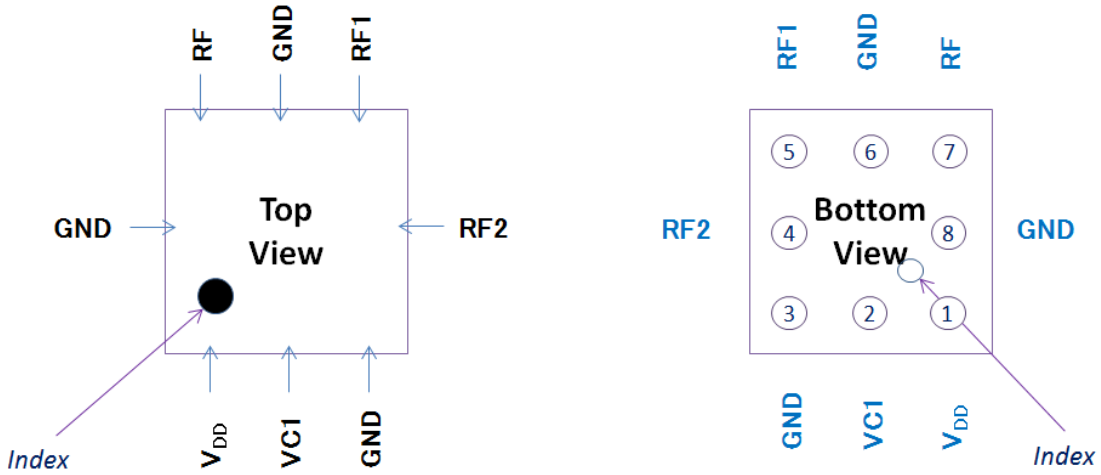


Truth Table

ON Path	VC1	F1	F2	F3	F4
RF – RF1	L	ON	OFF	OFF	ON
RF – RF2	H	OFF	ON	ON	OFF

Pin Configuration

Chip Size: 1.1 × 1.1 mm (0.4 mm Pitch)



Absolute Maximum Ratings

◆Supply voltage	V_{DD}	4	V	(Ta = 25 ℃)
◆Control voltage	VC	4	V	(Ta = 25 ℃)
◆Maximum input		37	dBm	(Ta = 25 ℃, V_{DD}=2.45 to 3.3V)
◆Operating temperature	Topr	–35 to +90	℃	
◆Storage temperature	Tstg	–65 to +150	℃	

DC Bias Condition

(Ta=25℃)

Parameter	Min.	Typ.	Max.	Unit
V_{DD}	2.45	2.65	3.3	V
VC(H)	1.35	1.8	3.3	V
VC(L)	0	-	0.45	V

Electrical Characteristics

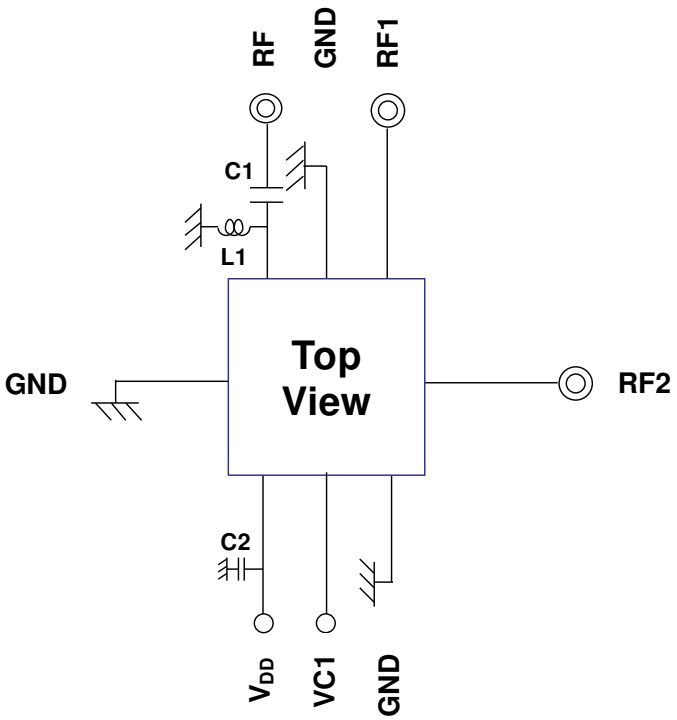
(V_{DD}=2.65V, Ta=25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	RF - RF1	*1	—	0.22	0.32	dB
			*2	—	0.26	0.41	
			*3	—	0.27	0.42	
			*4	—	0.30	0.45	
		RF - RF2	*1	—	0.22	0.32	
			*2	—	0.23	0.38	
			*3	—	0.23	0.38	
			*4	—	0.25	0.40	
Isolation	ISO	RF - RF1,2	*1	42	47	—	dB
			*2	31	36	—	
			*3	30	35	—	
			*4	26	31	—	
		RF1 - RF2	*1	34	39	—	
			*2	28	31	—	
			*3	27	30	—	
			*4	25	28	—	
VSWR	VSWR		704 to 2170 MHz	—	1.1	1.3	—
			2500 to 2690 MHz	—	1.15	1.4	
Harmonics	2fo	RF-RF1,2	*5	—	—	-45	dBm
	3fo			—	—	-45	
	2fo		*6	—	—	-45	
	3fo			—	—	-45	
	2fo		*7	—	—	-55	
	3fo			—	—	-55	
	2fo		*8	—	—	-55	
	3fo			—	—	-55	
Inter Modulation Product Power in Rx Band	IMD2	RF- RF1, 2	*9, *17	—	—	-110	dBm
			*10-12, *17	—	—	-110	
	IMD3		*13, *17	—	—	-110	
			*14-16, *17	—	—	-110	
Control Current	Ictl		VC = 1.8 V per line	—	0.05	1	μA
Supply Current	Idd		V_{DD} = 2.5 V	—	13	30	μA
Switching Speed	Ts		50 % VC to 90 % RF	—	3	5	μS
Wake up time	Tw		Wakeup time from V_{DD} on to Active mode	—	10	30	μS

Electrical Characteristics are measured with all RF ports terminated in 50 Ω.

* 1 freq = 704 to 960 MHz
* 2 freq = 1710 to 1990 MHz
* 3 freq = 2110 to 2170 MHz
* 4 freq = 2500 to 2690 MHz
* 5 Pin = 34dBm, freq = 824 to 915 MHz
* 6 Pin = 31dBm, freq = 1710 to 1910 MHz
* 7 Pin = 24dBm, freq = 1920 to 1980 MHz
* 8 Pin = 23dBm, freq = 2500 to 2570 MHz
* 9 Pin on RF: 20dBm, 835MHz, Pin on ANT: -15dBm, 45MHz
* 10 Pin on RF: 20dBm, 1745MHz, Pin on ANT: -15dBm, 95MHz
* 11 Pin on RF: 20dBm, 1880MHz, Pin on ANT: -15dBm, 80MHz
* 12 Pin on RF: 20dBm, 1950MHz, Pin on ANT: -15dBm, 190MHz
* 13 Pin on RF: 20dBm, 835MHz, Pin on ANT: -15dBm, 790MHz
* 14 Pin on RF: 20dBm, 1745MHz, Pin on ANT: -15dBm, 1650MHz
* 15 Pin on RF: 20dBm, 1880MHz, Pin on ANT: -15dBm, 1800MHz
* 16 Pin on RF: 20dBm, 1950MHz, Pin on ANT: -15dBm, 1760MHz
* 17 Measured with the recommended circuit

Recommended Circuit



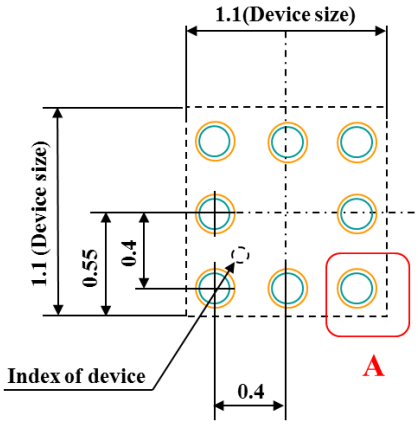
*1: No DC blocking capacitors are required on all RF ports.
*2: DC levels of all RF ports are GND.
*3: L1 (27 nH) and C1 (12 pF) are recommended on Ant port for ESD protection.
*4: C2(100 pF) is recommended on V_{DD} pin for Decoupling Capacitor.

Solder Bump Foot Print (Macro) Reference

Device specification

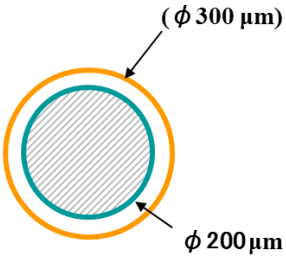
- Device size : 1.1 mm × 1.1 mm × t 0.35 mm
- Pin counts : 8 Pin
- Solder Bump height : 0.15 mm
- Solder Bump ball size : ϕ 0.2 mm
- Solder Bump pitch : 0.4 mm

Unit : mm



Detail - A

- Land size (Resist Open area) : ϕ 200 µm
- Cu pattern size : (ϕ 300 µm)

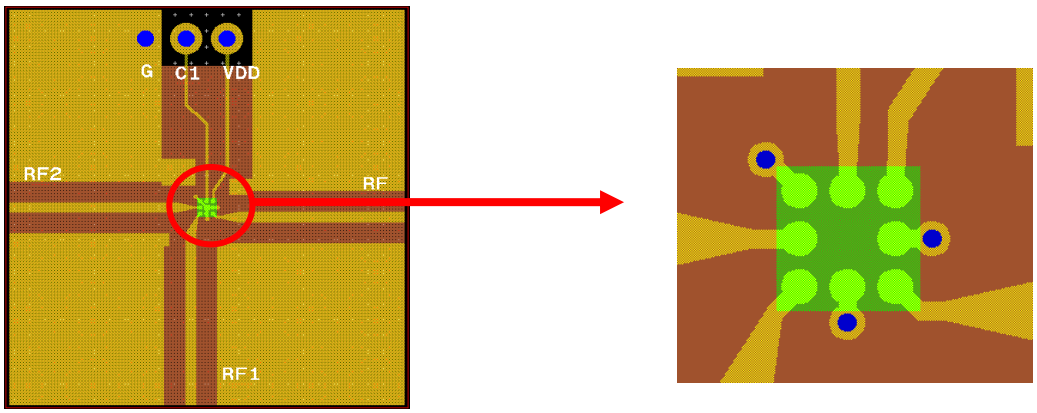


: Cu pattern

: Resist open

: Solder print area (Metal mask thickness : 110 µm)

Recommended PCB Layout



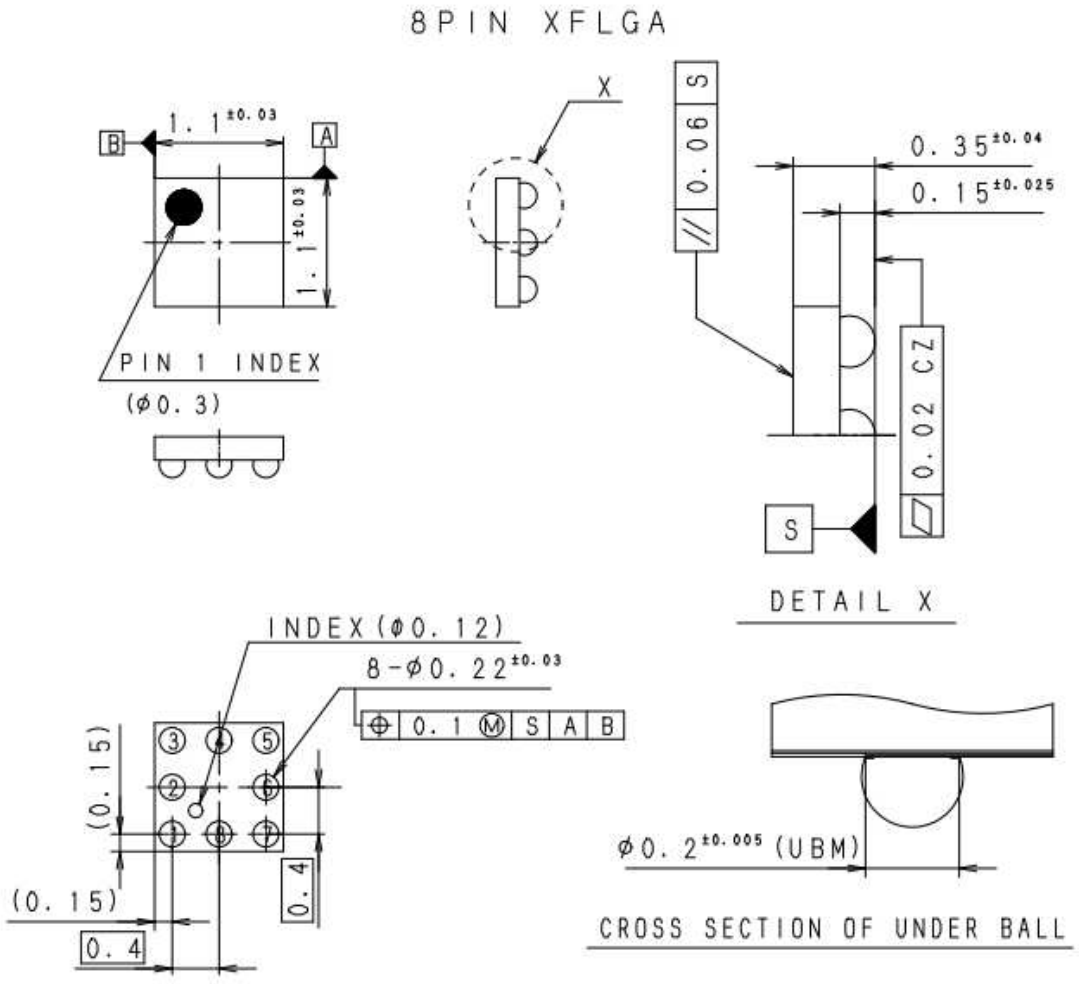
Device Area

Via

Metal Pattern

Package Outline

Unit : mm



PACKAGE STRUCTURE

SONY CODE	XFLGA-8S-433
JEITA CODE	S-XFLGA-1.1x1.1-0.4
JEDEC CODE	————

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	0.0008g

PART No. AP-2000-8LGAS3	Rev. 0
ISSUED 13.02.05	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CORD:GX-8-BAS	

Tape and Reel Size

CXA4011GC-T9

Unit : mm

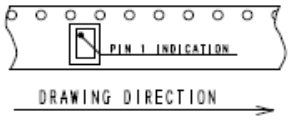
8mm WIDTH EMBOSSED TAPING
(FOR Sony Mobile Communications, Inc.)

PACKAGE CODE	EMBOSSED TAPING CODE
XFLGA-8S-433	R008XL11-08-N-1

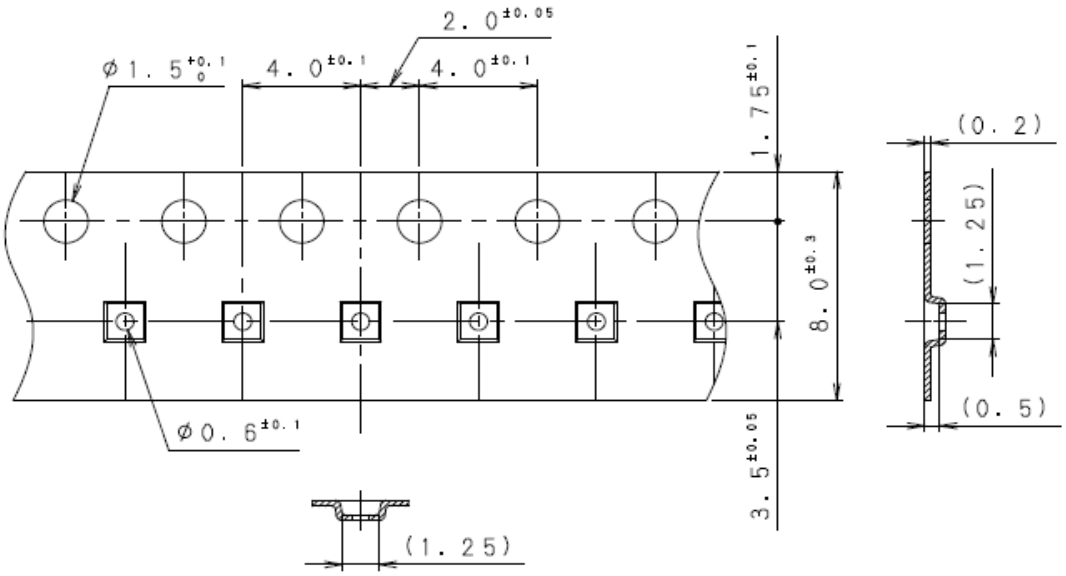
1. SCOPE

THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD(SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION(JEITA). JIS C0806-3. AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION



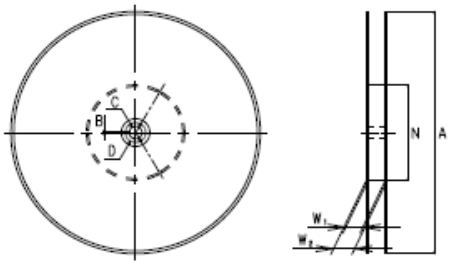
3. TAPING SPECIFICATIONS



NOTE)1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX. GENERAL TOLERANCE: ±0.2
2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT±0.2mm/ 10PITCH. UNIT:mm

4. REEL DIMENSIONS

φ180mm PLASTIC REEL

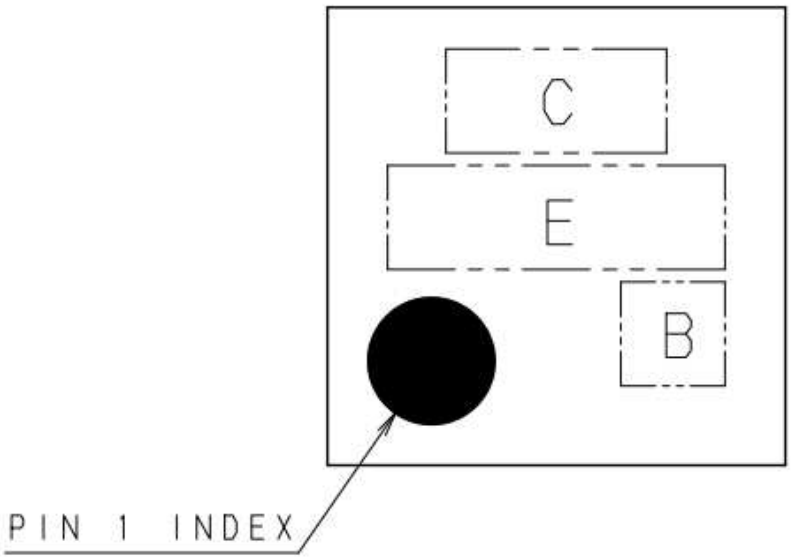


UNIT:mm

SYMBOL	A	N	C	D
DIMENSION	φ180±2	φ54 +0.5 0	φ13 +0.5 -0.2	φ20.2 min
SYMBOL	B	W_1	W_2	
DIMENSION	1.5 min	8.4 +1.0 -0.6	12.4±2	

MATERIAL:POLYSTYRENE CONTAINING CARBON(ANTISTATIC)

Marking



MARKING C: AR

注1） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
2） B部は製造年（1文字）を配置する。
3） E部は通し記号（MAX3文字）を配置する。

< INSTRUCTIONS >
1) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) MANUFACTURING YEAR (1 CHARACTER) IN SECTION B.
3) SERIAL CODE (MAX 3 CHARACTERS) IN SECTION E.

Moisture Sensitivity

Moisture Sensitivity Level for this part is MSL = 1

Note: The MSL of this product contains the following storage conditions (Taping).

Storage period

(With or without opening moisture-proof packing)

⇒The storage time limit shall be 1 year or less under storage environment conditions of temperature 30℃ or less and humidity 85%RH or less.

*This device is unnecessary management of moisture sensitivity.

However, we will assume 1 year for the convenience of seal strength of the taping product.

Avoid storage in locations exposed to direct sunlight, locations where corrosive gases are generated, or dusty locations.

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits