SONY

SP4T SOI Antenna Diversity Switch, and 3G/LTE Tx Switch

CXA2984GC

Description

The CXA2984 is the SP4T antenna diversity switch for WCDMA, and Tx switch for 3G/LTE applications..

The CXA2984 has a 1.8 V CMOS compatible decoder.
The SONY Silicon On Insulator (SOI) technology is used for low insertion loss.

Features

◆Low Insertion loss : 0.37 dB(typ.) @800 MHz
0.45 dB(typ.) @2 GHz
0.50 dB(typ.) @2.7 GHz
◆No DC Blocking Capacitors (except sourcing DC bias)
◆Solder Bump Bare Die(SBBD): Bump Pitch=0.4 mm
◆Small Flip-Chip Size : 1.1 mm x 1.5 mm x 0.35 mm Typ.
◆Lead-Free and RoHS compliant
◆Applications: Diversity Switch, 3G/LTE Tx Switch

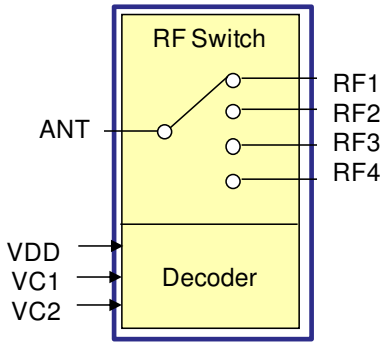
Structure

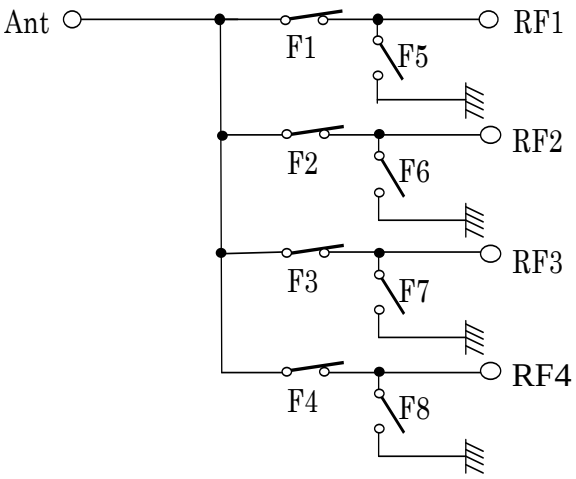
SOI CMOS MMIC

This IC is ESD sensitive device. Special handling precautions are required

Version 1.21 Date Jul. 17, 2013
E13616

Block Diagram

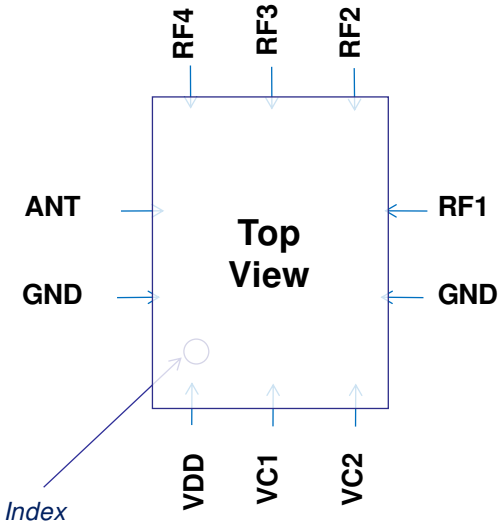


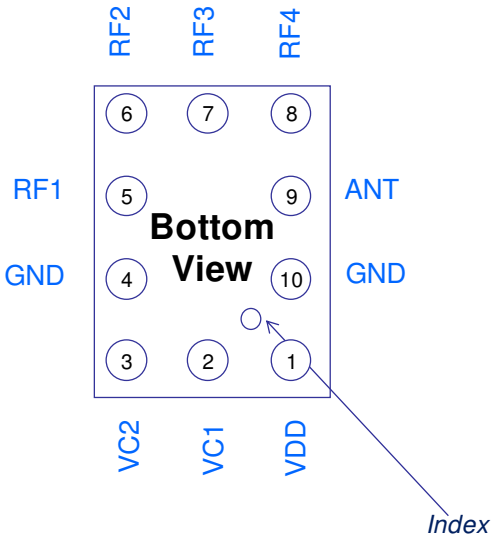


Truth Table

State	Active Path	VC State		Switch State							
		1	2	F1	F2	F3	F4	F5	F6	F7	F8
1	ANT – RF1	L	L	ON	OFF	OFF	OFF	OFF	ON	ON	ON
2	ANT – RF2	L	H	OFF	ON	OFF	OFF	ON	OFF	ON	ON
3	ANT – RF3	H	L	OFF	OFF	ON	OFF	ON	ON	OFF	ON
4	ANT – RF4	H	H	OFF	OFF	OFF	ON	ON	ON	ON	OFF

Pin Configuration





Absolute Maximum Ratings

◆Supply voltage	V_{DD}	4	V	(Ta = 25 ℃)
◆Control voltage	VC	4	V	(Ta = 25 ℃)
◆Maximum input		31	dBm	(Ta = 25 ℃, VDD=2.5 to 3.3 V)
◆Operating temperature	Topr	–35 to +90	℃	
◆Storage temperature	Tstg	–65 to +150	℃	

DC Bias Condition

(Ta=25℃)

Parameter	Min.	Typ.	Max.	Unit
VDD	2.5	2.8	3.3	V
VC(H)	1.3	1.8	3.3	V
VC(L)	0	-	0.45	V

Electrical Characteristics

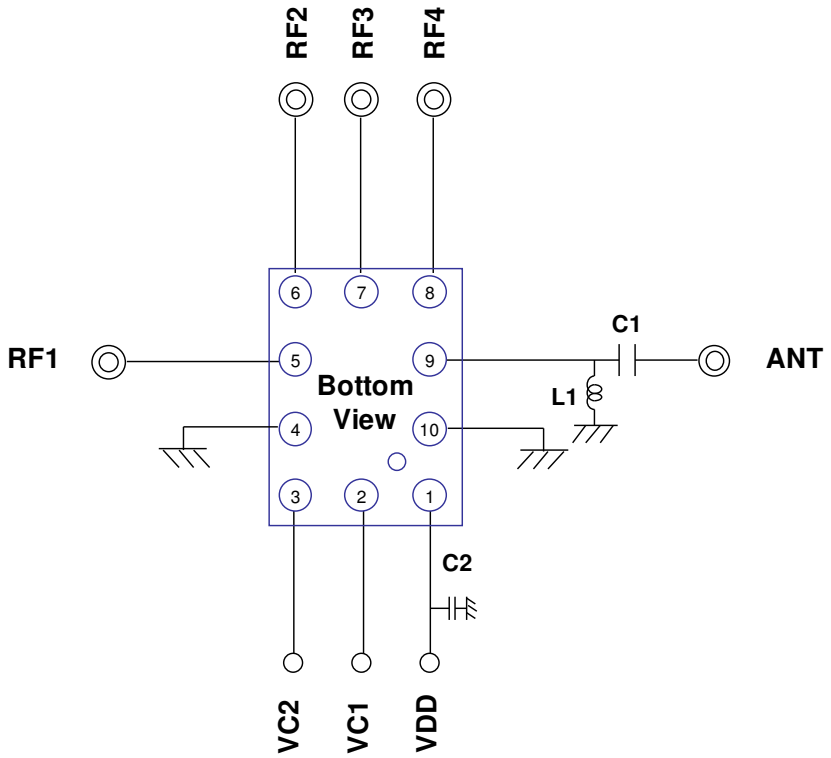
(V_{DD}=2.5V, Ta=25°C)

Item	Symbol	Path	Condition	Min.	Typ.	Max.	Unit
Insertion Loss	IL	ANT – RF1	*1	-	0.37	0.47	dB
			*2, *3	-	0.45	0.60	
			*4	-	0.50	0.65	
		ANT – RF2	*1	-	0.40	0.50	
			*2, *3	-	0.52	0.67	
			*4	-	0.65	0.80	
		ANT – RF3	*1	-	0.40	0.50	
			*2, *3	-	0.62	0.77	
			*4	-	0.80	0.95	
		ANT – RF4	*1	-	0.42	0.52	
			*2, *3	-	0.58	0.73	
			*4	-	0.75	0.90	
Isolation	ISO.	ANT – RF1	*1	25	40	-	dB
			*2, *3	17	30	-	
			*4	15	26	-	
		ANT – RF2	*1	27	38	-	dB
			*2, *3	16	25	-	
			*4	15	20	-	
		ANT – RF3	*1	29	36	-	dB
			*2, *3	16	25	-	
			*4	15	22	-	
		ANT – RF4	*1	30	38	-	dB
			*2, *3	18	25	-	
			*4	17	22	-	
VSWR	VSWR		824 to 2170 MHz		1.1	1.5	-
			2500 to 2690 MHz		1.4	1.7	
Harmonics***	2fo	ANT – RF1-4	*1		-64	-45	dBm
	3fo				-67	-45	
	2fo		*2, *3		-64	-45	
	3fo				-64	-45	
	2fo		*4		-62	-45	
	3fo				-62	-45	
Inter Modulation Product Power in Rx Band	IMD2	ANT – RF1-4	*5, *13		-	-100	dBm
			*6-8, *13		-	-100	
	IMD3		*9, *13		-	-100	
			*10-12, *13		-	-100	
Control Current	Ictl		Vctl = 1.8V		0.05	2	µA
Supply Current	Idd		Vdd = 2.5V		12	30	µA
Switching Speed	Swt	RF1-4	Vdd = 2.5V		3	5	µS

Electrical Characteristics are measured with all RF ports terminated in 50 Ohms.

* 1 Pin = 26 dBm, freq = 704 to 915 MHz
* 2 Pin = 26 dBm, freq = 1710 to 1910 MHz
* 3 Pin = 26 dBm, freq = 1920 to 1980 MHz
* 4 Pin = 26 dBm, freq = 2500 to 2570 MHz
* 5 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 45 MHz
* 6 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 95 MHz
* 7 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 80 MHz
* 8 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 190 MHz
* 9 Pin on RF: 20 dBm, 835 MHz, Pin on ANT: -15 dBm, 790 MH
* 10 Pin on RF: 20 dBm, 1745 MHz, Pin on ANT: -15 dBm, 1650 MHz
* 11 Pin on RF: 20 dBm, 1880 MHz, Pin on ANT: -15 dBm, 1800 MHz
* 12 Pin on RF: 20 dBm, 1950 MHz, Pin on ANT: -15 dBm, 1760 MHz
* 13 Measured with the recommended circuit

Recommended Circuit



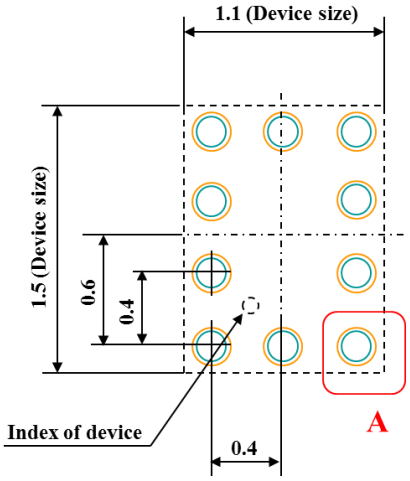
*1: No DC blocking capacitors are required on all RF ports.
*2: DC levels of all RF ports are GND.
*3: L1 (27 nH) and C1 (6.8 pF) are recommended on Ant port for ESD protection.
*4: C2(100 pF) is recommended on VDD pin for Decoupling Capacitor.

Solder Bump Foot Print (Macro) *Reference

Device specification

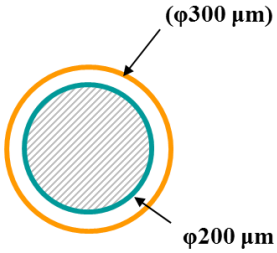
- Device size : 1.1 mm × 1.5 mm × t 0.35 mm
- Pin counts : 10Pin
- Solder Bump height : 0.15 mm
- Solder Bump ball size : φ0.2 mm
- Solder Bump pitch : 0.4 mm

Unit:mm



Detail - A

- Land size (Resist Open area) : φ200 µm
- Cu pattern size : (φ300 µm)

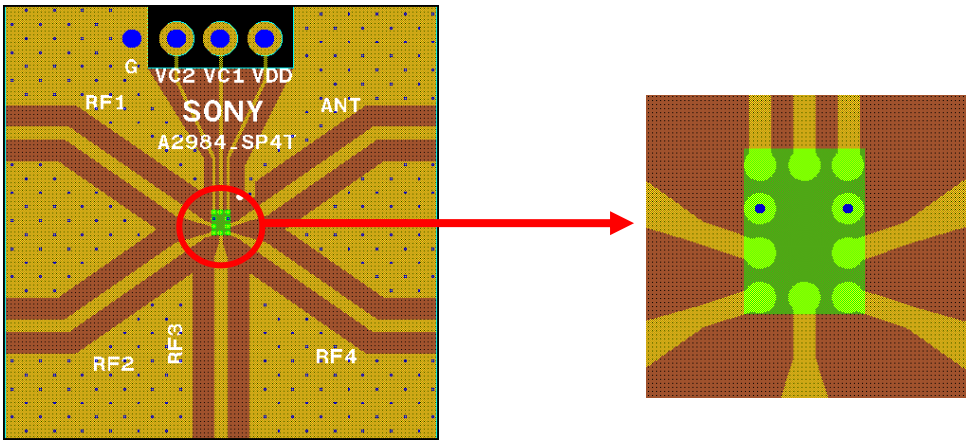


: Cu pattern

: Resist open

: Solder print area (Metal mask thickness : 110 µm)

Recommended PCB Layout



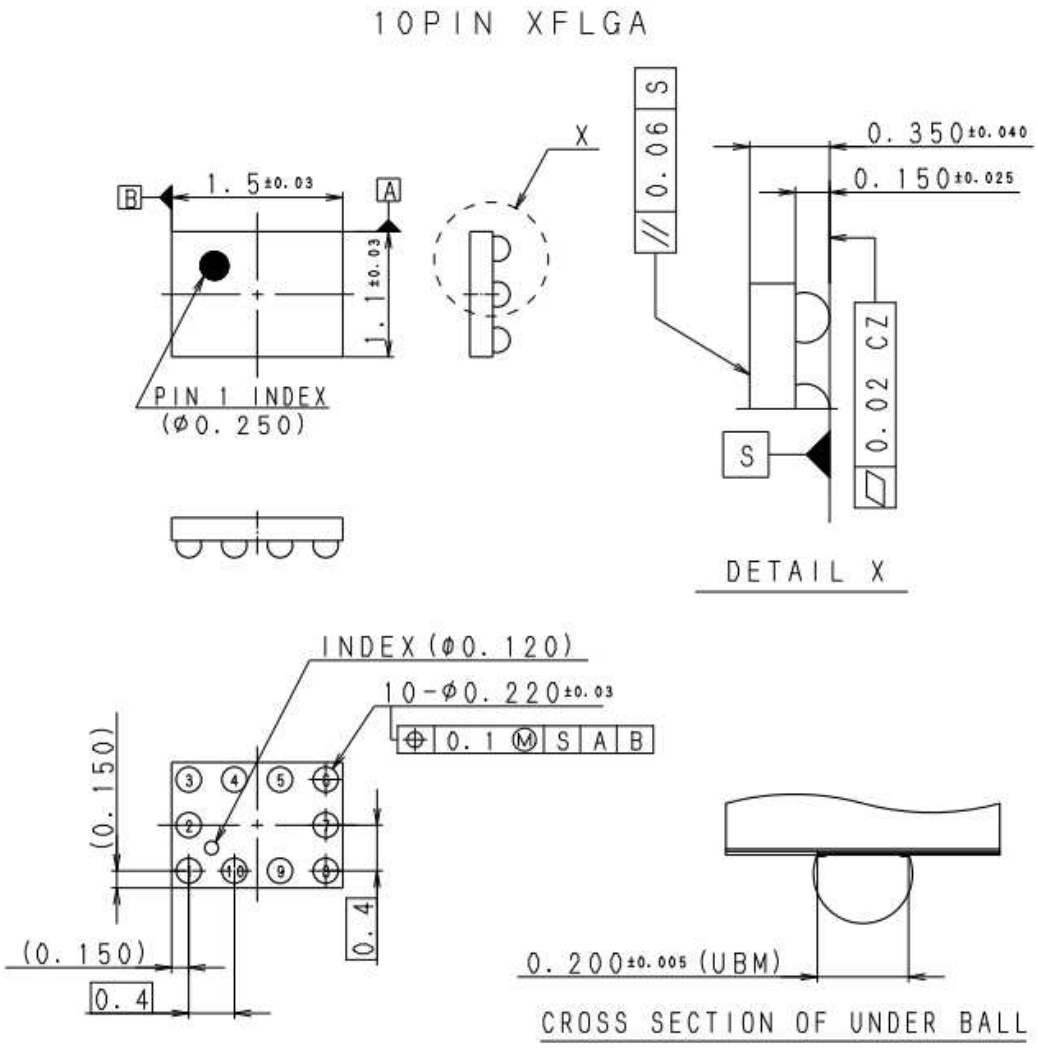
Device Area

Via

Metal Pattern

Package Outline

Unit : mm



PACKAGE STRUCTURE

SONY CODE	XFLGA-10S-432
JEITA CODE	S-XFLGA10-1.5x1.1-0.4
JEDEC CODE	————

PACKAGE MATERIAL	Si SUBSTRATE
TERMINAL MATERIAL	Sn-3.0Ag-0.5Cu
PACKAGE MASS	0.001g

PART No. AP-2000-10LGAS2	Rev. 0
ISSUED 12.06.20	REVISED
PRODUCTION LINE	COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS PKG CODE:GX-10-AAS For CXA2984GC	

Tape and Reel Size

CXA2984GC-T9

Unit : mm

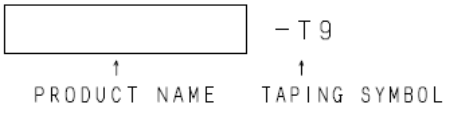
8mm WIDTH EMBOSSED TAPING

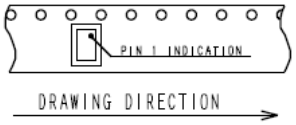
PACKAGE CODE	EMBOSSED TAPING CODE
XFLGA-10S-433	R010XLN3-08-N-1

1. SCOPE

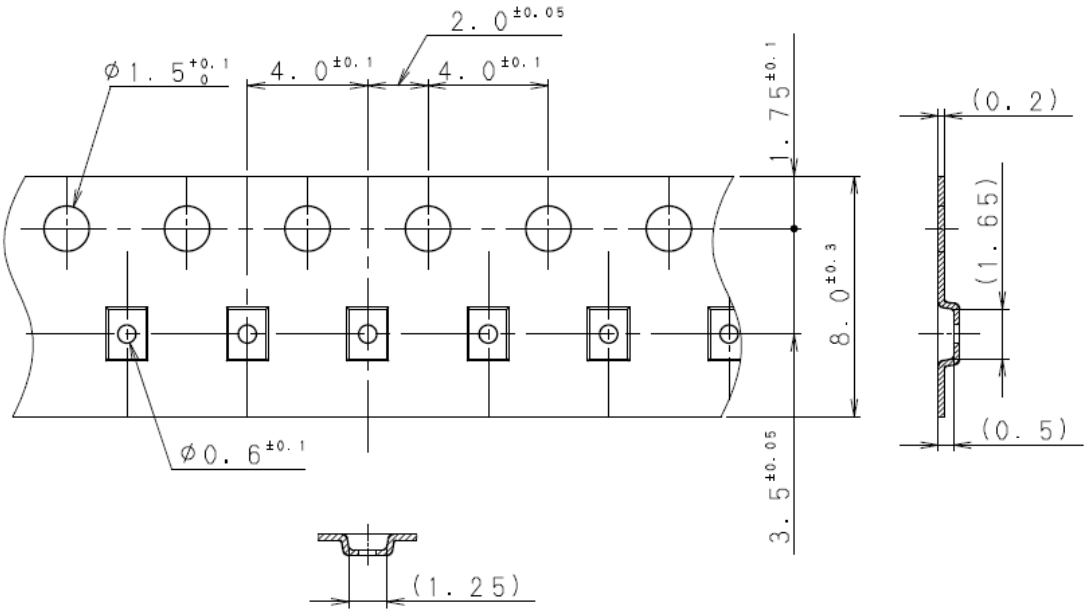
THIS SPECIFICATION DESCRIBES THE EMBOSSED TAPING FOR SMD (SURFACE MOUNTED DEVICE) IC'S. FOR SHIPMENT. THIS SPECIFICATION IS BASED ON THE STIPULATIONS OF JAPAN ELECTRONICS AND INFORMATION TECHNOLOGY INDUSTRIES ASSOCIATION (JEITA), JIS C0806-3, AND ELECTRONIC INDUSTRIES ASSOCIATION EIA-481.

2. PRODUCT INDICATION





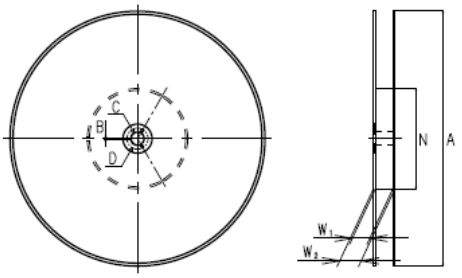
3. TAPING SPECIFICATIONS



NOTE) 1. THE R MEASUREMENT WITHOUT INDICATION IS ASSUMED TO BE 0.3mm MAX. GENERAL TOLERANCE: ±0.2
2. THE FEED HOLE CUMULATIVE PITCH ERROR IS ASSUMED AT ±0.2mm/ 10 PITCH. UNIT: mm

4. REEL DIMENSIONS

φ180mm PLASTIC REEL

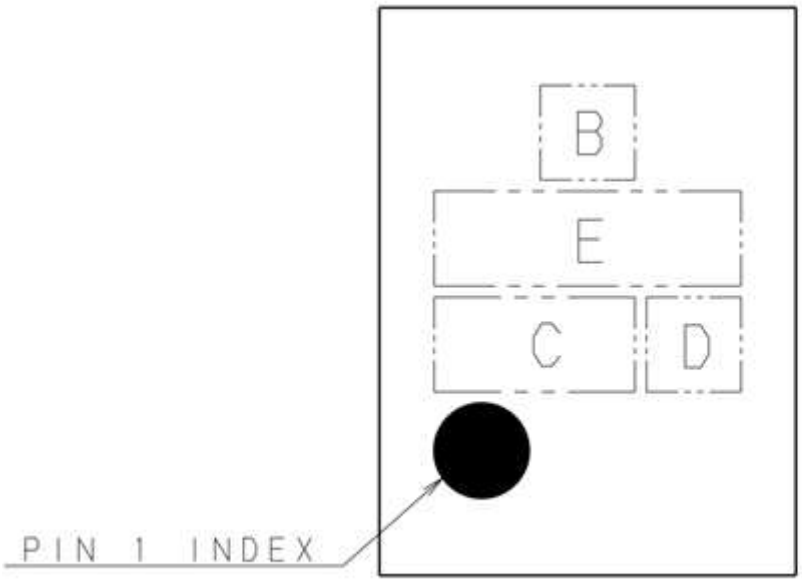


UNIT: mm

SYMBOL	A	N	C	D
DIMENSION	φ180±2	φ54 +3 0	φ13 +0.5 -0.2	φ20.2min
SYMBOL	B	W_1	W_2	
DIMENSION	1.5min	8.4 +1.5 -0.0	12.4±2	

MATERIAL: POLYSTYRENE CONTAINING CARBON (ANTISTATIC)

Marking



MARKING C:

注1） C部は製品名（Max2文字）を配置する。
（2文字を超える場合は製品名省略標示規定に従う。）
2） B部は製造年（1文字）を配置する。
3） D部は組立場所記号（1文字）を配置する。
4） E部は通し記号（MAX3文字）を配置する。

< INSTRUCTIONS >
1) TYPE NO. (MAX 2 CHARACTERS) IN SECTION C.
(FOR MORE THAN 2 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)
2) MANUFACTURING YEAR (1 CHARACTER) IN SECTION B.
3) ASSEMBLY LOCATION CODE (1 CHARACTER) IN SECTION D.
4) SERIAL CODE (MAX 3 CHARACTERS) IN SECTION E.

Moisture Sensitivity

Moisture Sensitivity Level for this part is MSL = 2

Note

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Application circuits shown, if any, are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits