

6-channel CCD Vertical Clock Driver

Description

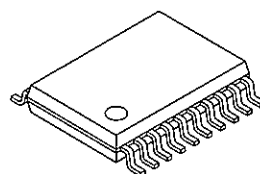
The CXD3400N is a vertical clock driver for CCD image sensor. This IC is composed of 6 channels which supports high frame rate readout mode.

Features

- Composition

Vertical transfer output	3 levels driver × 4
	2 levels driver × 2
Electronic shutter output	2 levels driver × 1
- Suitable drive capability for high-pixel CCD (40% improved compared to current device)
- Small package (20-pin SSOP)
- 2.7 to 5.5V supported input interface

20 pin SSOP (Plastic)



Applications

Digital still camera

Structure

CMOS

Absolute Maximum Ratings

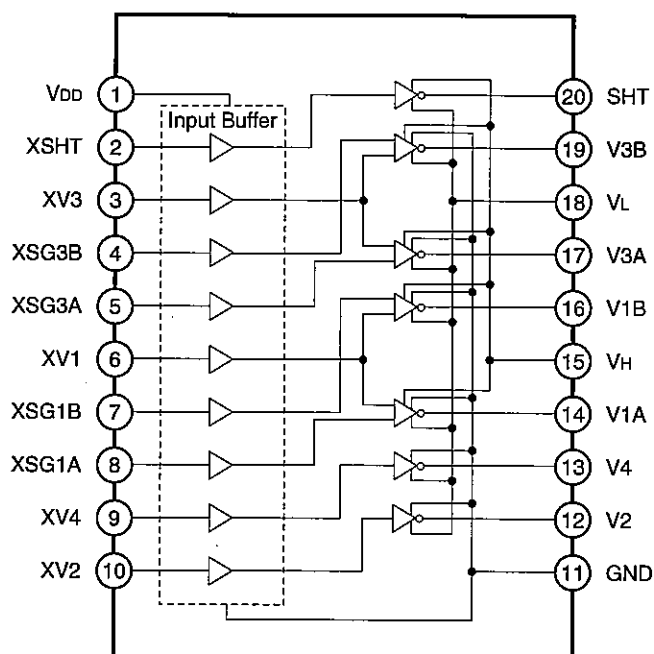
- | | | | |
|-------------------------|------------------|-------------------------------------|----|
| • Supply voltage | V _{DD} | GND – 0.3 to +7.0 | V |
| • Supply voltage | V _L | GND to –10 | V |
| • Supply voltage | V _H | V _L + 26 | V |
| • Input voltage | V _{IN} | GND – 0.3V to V _{DD} + 0.3 | V |
| • Operating temperature | T _{opr} | –20 to +75 | °C |
| • Storage temperature | T _{stg} | –55 to +150 | °C |

Recommended Operating Conditions

- | | | | |
|-------------------------|------------------|--------------|----|
| • Supply voltage | V _{DD} | 2.7 to 5.5 | V |
| • Supply voltage | V _L | −5.0 to −9.0 | V |
| • Supply voltage | V _H | 11.5 to 15.5 | V |
| • Operating temperature | T _{opr} | −20 to +75 | °C |

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Block Diagram



Pin Description

Pin No.	Symbol	I/O	Functions
1	VDD	—	Input power supply (3.3V system)
2	XSHT	I	SHT pulse input
3	XV3	I	V3A and V3B transfer pulse input
4	XSG3B	I	V3B readout pulse input
5	XSG3A	I	V3A readout pulse input
6	XV1	I	V1A and V1B readout pulse input
7	XSG1B	I	V1B readout pulse input
8	XSG1A	I	V1A readout pulse input
9	XV4	I	V4 transfer pulse input
10	XV2	I	V2 transfer pulse input
11	GND	—	GND (= VM)
12	V2	O	High voltage output (2 levels: VM, VL)
13	V4	O	High voltage output (2 levels: VM, VL)
14	V1A	O	High voltage output (3 levels: VH, VM, VL)
15	VH	—	Positive power supply for high voltage output (15V system)
16	V1B	O	High voltage output (3 levels: VH, VM, VL)
17	V3A	O	High voltage output (3 levels: VH, VM, VL)
18	VL	—	Negative power supply for high voltage output (−7.5V system)
19	V3B	O	High voltage output (3 levels: VH, VM, VL)
20	SHT	O	High voltage output (2 levels: VH, VL)

Truth Table

Input				Output		
XV1, 3	XSG1A, 1B, 3A, 3B	XV2, 4	XSHT	V1A, 1B, 3A, 3B	V2, 4	SHT
L	L	X	X	V _H	X	X
L	H	X	X	V _M	X	X
H	L	X	X	Z	X	X
H	H	X	X	V _L	X	X
X	X	L	X	X	V _M	X
X	X	H	X	X	V _L	X
X	X	X	L	X	X	V _H
X	X	X	H	X	X	V _L

Z: High impedance X: Don't care

Electrical Characteristics

DC Characteristics

(V_{DD} = 3.3V, V_H = 15V, V_M = GND, V_L = -8.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
"H" level input voltage	V _{IH}		0.7V _{DD}	—	—	V
"L" level input voltage	V _{IL}		—	—	0.3V _{DD}	V
Input current	I _{IN}	V _{IN} = GND to 5V	-10	0.0	10	μA
Operating supply current	I _H	*1	—	0.10	0.20	mA
Operating supply current	I _{DD}	*1	—	0.25	0.50	mA
Operating supply current	I _L	*1	-8.5	-5.5	—	mA
Output current	I _{OL}	V1A, 1B, 3A, 3B, V2, 4 = -8.25V	10	—	—	mA
Output current	I _{OM1}	V1A, 1B, 3A, 3B, V2, 4 = -0.25V	—	—	-5.0	mA
Output current	I _{OM2}	V1A, 1B, 3A, 3B = 0.25V	5.0	—	—	mA
Output current	I _{OH}	V1A, 1B, 3A, 3B = 14.75V	—	—	-7.2	mA
Output current	I _{OSL}	SHT = -8.25V	5.4	—	—	mA
Output current	I _{OSH}	SHT = 14.75V	—	—	-4.0	mA

*1 See Measurement Circuit. Shutter speed 1/10000

Note) Current direction +: inflow to IC; -: outflow from IC

Switching Characteristics

(V_{DD} = 3.3V, V_H = 15V, V_M = GND, V_L = -7.5V)

Item	Symbol	Conditions	Min.	Typ.	Max.	Unit
Propagation delay time	T _{PLM}	*1	50	70	100	ns
Propagation delay time	T _{PMH}	*1	50	70	100	ns
Propagation delay time	T _{PLH}	*1	50	70	100	ns
Propagation delay time	T _{PML}	*1	10	30	50	ns
Propagation delay time	T _{PHM}	*1	10	30	50	ns
Propagation delay time	T _{PHL}	*1	10	30	50	ns
Rise time	T _{TLM}	V _L → V _M *1	200	350	500	ns
Rise time	T _{TMH}	V _M → V _H *1	200	350	500	ns
Rise time	T _{TLH}	V _L → V _H *1	30	60	90	ns
Fall time	T _{TML}	V _M → V _L *1	200	350	500	ns
Fall time	T _{THM}	V _H → V _M *1	200	350	500	ns
Fall time	T _{THL}	V _H → V _L *1	30	60	90	ns
Output noise voltage	V _{CLH}	*2	—	—	1.0	V
Output noise voltage	V _{CLL}	*2	—	—	1.0	V
Output noise voltage	V _{CMH}	*2	—	—	1.0	V
Output noise voltage	V _{CML}	*2	—	—	1.0	V

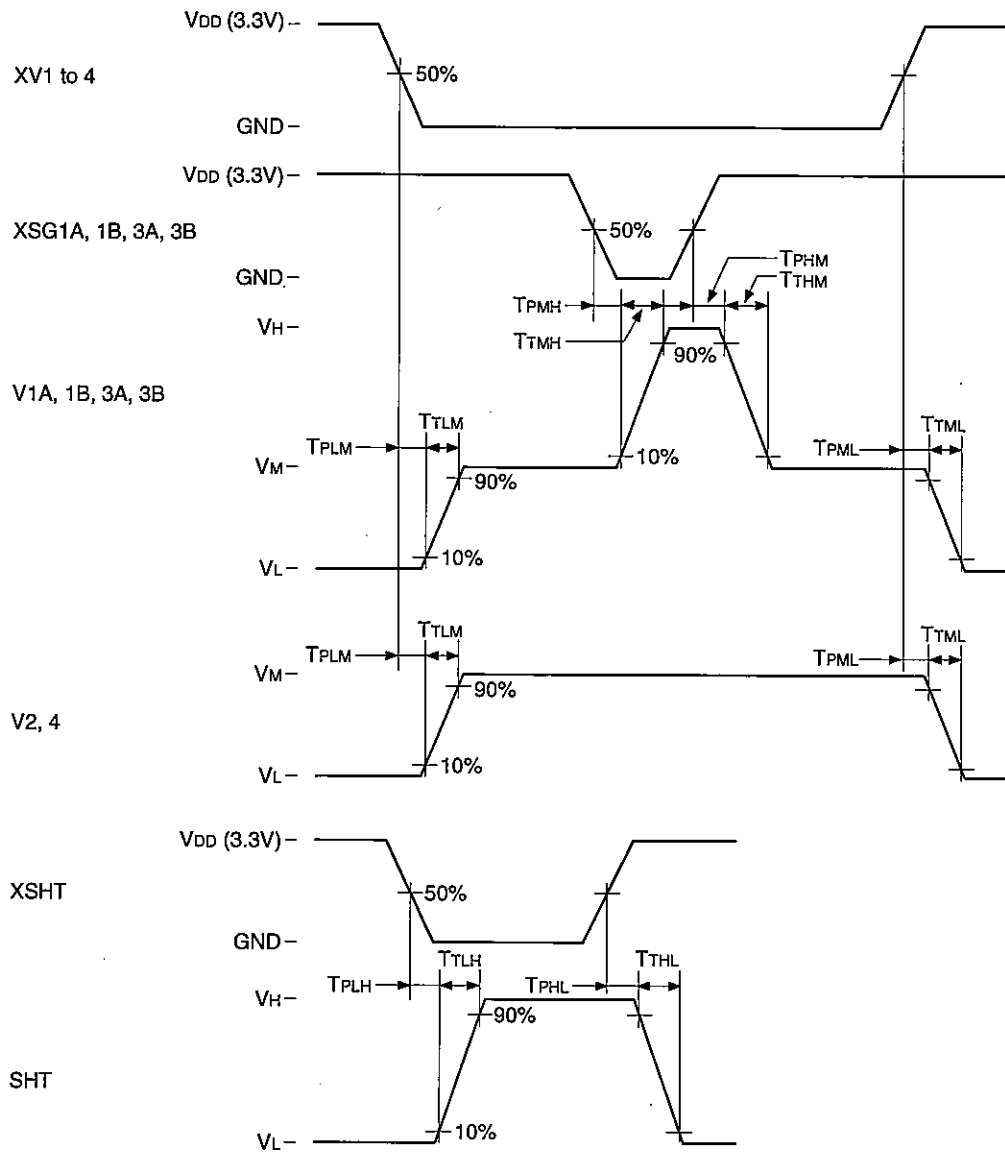
*1 See Switching Waveform.

*2 See Noise on a Waveform.

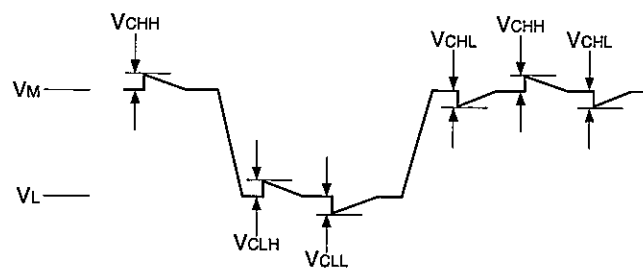
Note) Each item is evaluated by Measurement Circuit.**Notes on Operation** (See Application Circuit.)

1. Be sure to protect against static electricity because this IC is MOS structure.
2. A bypass capacitor (0.1μF or more) is connected between GND and near each power supply (V_H, V_{DD}, V_L).
3. In order to protect CCD image sensor, input SHT pin output to SUB pin of CCD image sensor after that has been clamped at V_H.

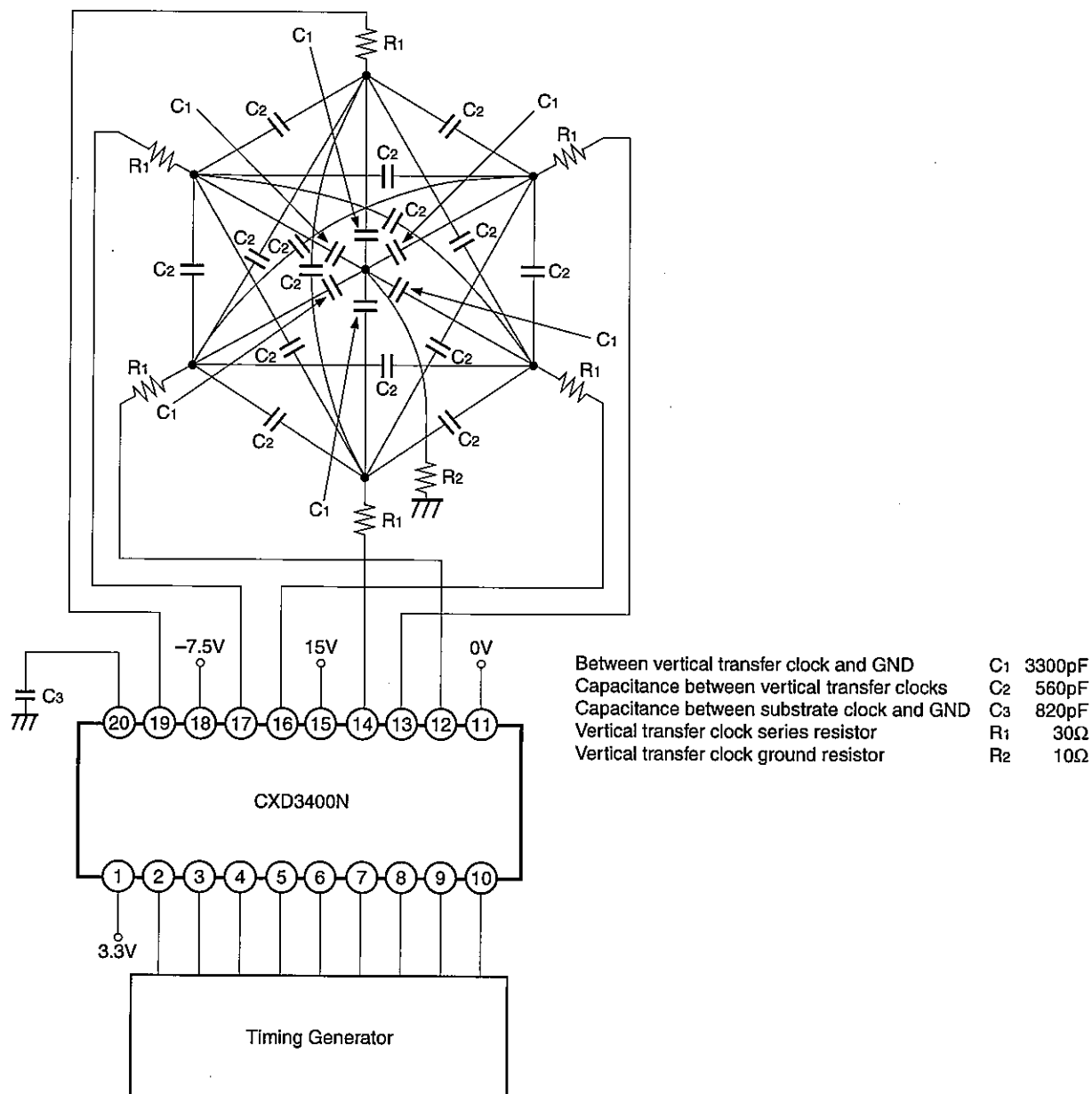
Switching Waveform



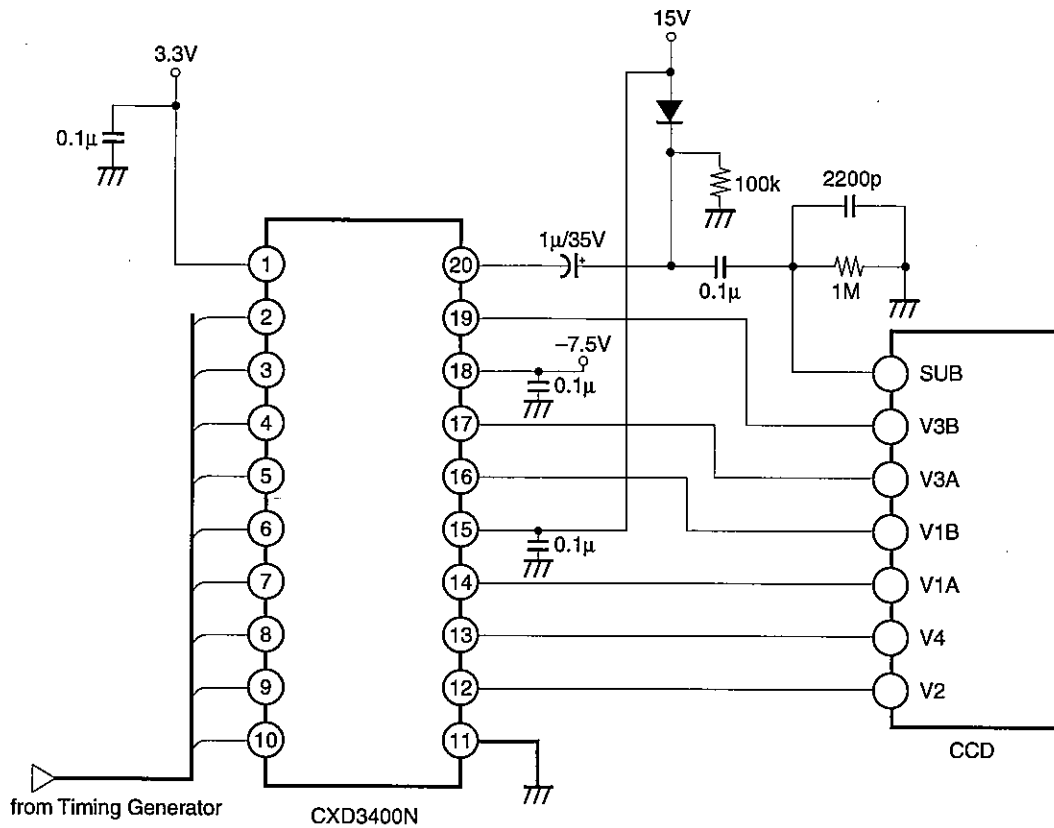
Noise on a Waveform



Measurement Circuit



Application Circuit



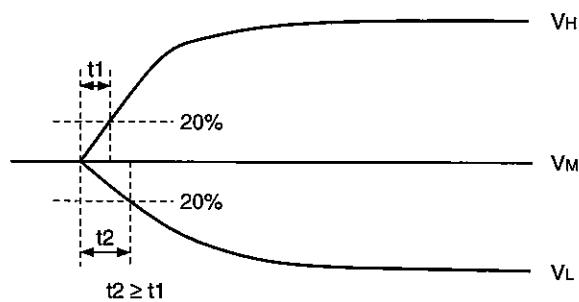
* See with drive circuit of CCD image sensor.

Application circuits shown are typical examples illustrating the operation of the devices. Sony cannot assume responsibility for any problems arising out of the use of these circuits or for any infringement of third party patent and other right due to same.

Note with Power-on Sequence

To protect CCD image sensor, rise two power supplies, V_L and V_H as follows.

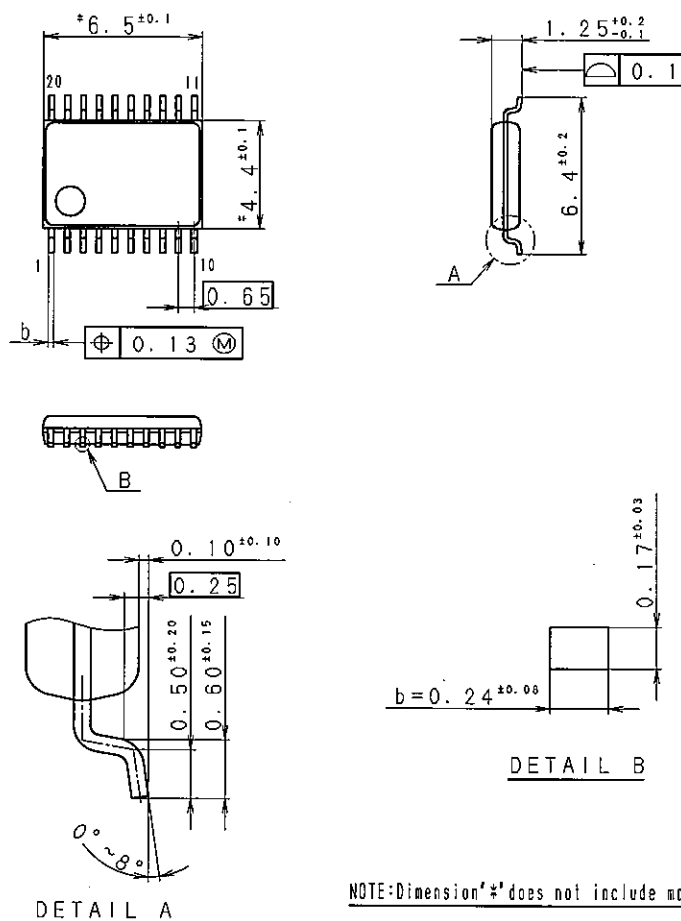
Note that rise V_{DD} first.



Package Outline Unit: mm

Ass'y: Fujitsu IMTKyusyu

20PIN SSOP (PLASTIC)



NOTE: Dimension '*' does not include mold protrusion.

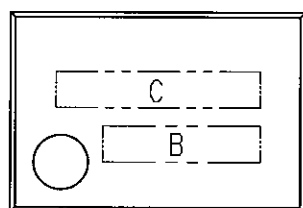
PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L021
JEITA CODE	P-SSOP20-4.4X6.5-0.65
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.09g

PART No.	AP-2000-20MA4	Rev. 0
ISSUED	11.11.18	REVISED
PRODUCTION LINE		COMPILING DIV. SONY SEMICONDUCTOR.
REMARKS	PKG CODE N-20-AA	

Marking



MARKING C: D3400N

注1) C部は製品名 (Max 7文字) を配置する。

(7文字を超える場合は製品名省略指示規定に従う。)

注2) B部はロット番号 (Max 5文字) を配置する。

(規定文字数未満につき省略は省略規定に従う。)

< INSTRUCTIONS >

1) TYPE NO. (MAX 7 CHARACTERS) IN SECTION C.

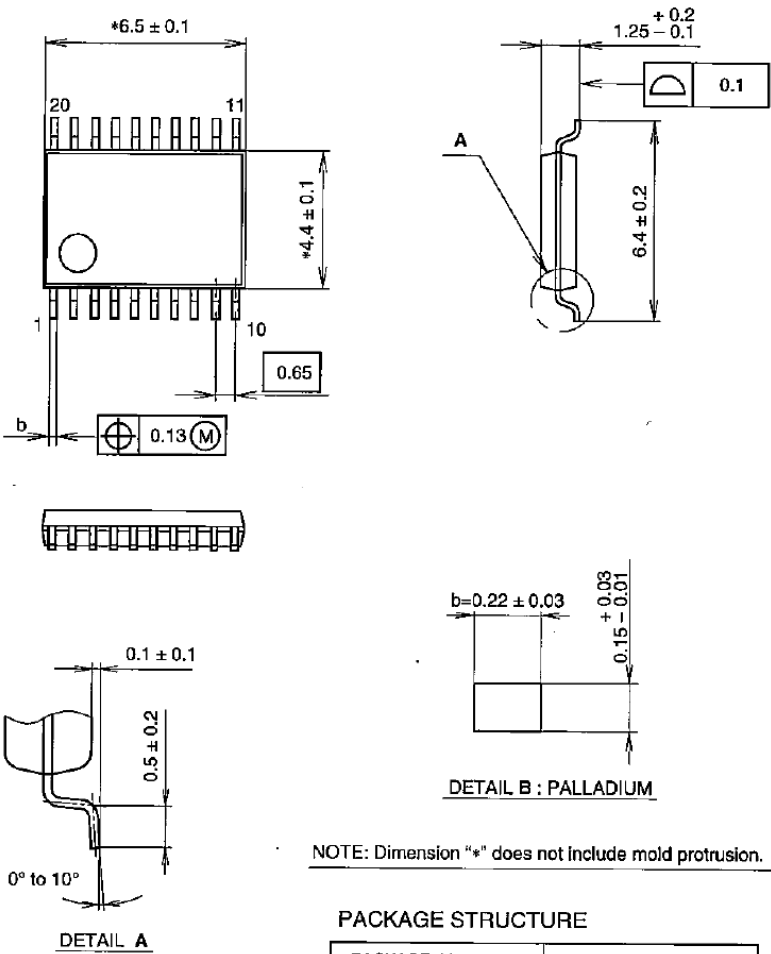
(FOR MORE THAN 7 CHARACTERS FOLLOW RULES FOR ABBREVIATIONS.)

2) LOT NO. (MAX 5 CHARACTERS) IN SECTION B.

(FOLLOW RULES FOR ABBREVIATIONS.)

Package Outline Unit : mm
Ass'y : SCK Kagoshima/SDT/PROSPERITY ELECTRONICS CO., LTD.

20PIN SSOP (PLASTIC)



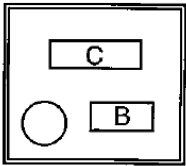
NOTE: Dimension "*" does not include mold protrusion.

PACKAGE STRUCTURE

SONY CODE	SSOP-20P-L01
EIAJ CODE	SSOP020-P-0044
JEDEC CODE	

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	PALLADIUM PLATING
LEAD MATERIAL	COPPER ALLOY
PACKAGE MASS	0.1g

Marking



C:D3400N
B: Lot No. (Max. 5)

管理記号 (Control No.)
製造週 (Week manufactured)
製造年 (西暦下 1 桁)
(Year manufactured)