SONY

Diagonal 4.5mm (Type 1/4) Progressive Scan CCD Image Sensor
with Square Pixel for Color Cameras

ICX618AKA

Description

The ICX618AKA is a diagonal 4.5mm (Type 1/4) interline CCD solid-state image sensor with a square pixel array which supports VGA format. Progressive scan enables all pixel signals to be output separately within approximately 1/60 second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still images without a mechanical shutter. The sensitivity and near infrared sensitivity are improved drastically through the adoption of advanced EXview HAD CCD technology. This chip is suitable for applications such as security cameras and network cameras.
The ICX618AKA has different spectral characteristics from the current CCD.

Features

- ◆ High sensitivity (+3.5dB compared with the ICX614AKA)
- ◆ High saturation signal (+2.0dB compared with the ICX614AKA)
- ◆ Low smear (– 8.0dB compared with the ICX614AKA)
- ◆ Progressive scan enables individual readout of the image signals from all pixels.
- ◆ Square pixel
- ◆ Supports VGA format
- ◆ Horizontal drive frequency: Supports 24.54MHz
- ◆ No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- ◆ Ye, Cy, Mg and G complementary color mosaic filters on chip
- ◆ High sensitivity, low dark current
- ◆ Continuous variable-speed shutter
- ◆ Excellent anti-blooming characteristics
- ◆ Horizontal register: 3.3V drive
- ◆ 14-pin high accuracy plastic package (dual-surface reference available)

EXview HAD CCD™

* EXview HAD CCD is a trademark of Sony Corporation. The EXview HAD CCD is a CCD that drastically improves light efficiency by including near infrared light region as a basic structure of HAD (Hole-Accumulation Diode) sensor.

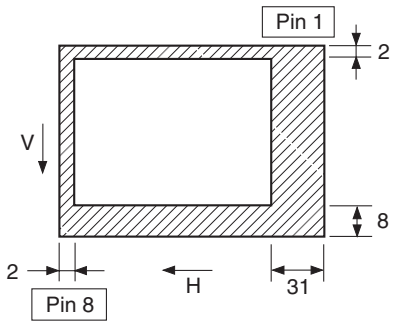
E05953

Element Structure

- ◆ Interline CCD image sensor
- ◆ Image size
  Diagonal 4.5mm (Type 1/4)
- ◆ Number of effective pixels
  659 (H) × 494 (V) approx. 330K pixels
- ◆ Total number of pixels
  692 (H) × 504 (V) approx. 350K pixels
- ◆ Chip size
  4.46mm (H) × 3.80mm (V)
- ◆ Unit cell size
  5.6μm (H) × 5.6μm (V)
- ◆ Optical black
  Horizontal (H) direction: Front 2 pixels, rear 31 pixels
  Vertical (V) direction: Front 8 pixels, rear 2 pixels
- ◆ Number of dummy bits
  Horizontal: 16
  Vertical: 4
- ◆ Substrate material
  Silicon

Optical Black Position

(Top View)



USE RESTRICTION NOTICE (December 1, 2003 ver.)

This USE RESTRICTION NOTICE (“Notice”) is for customers who are considering or currently using the CCD products (“Products”) set forth in this specifications book. Sony Corporation (“Sony”) may, at any time, modify this Notice which will be available to you in the latest specifications book for the Products. You should abide by the latest version of this Notice. If a Sony subsidiary or distributor has its own use restriction notice on the Products, such a use restriction notice will additionally apply between you and the subsidiary or distributor. You should consult a sales representative of the subsidiary or distributor of Sony on such a use restriction notice when you consider using the Products.

Use Restrictions

- The Products are intended for incorporation into such general electronic equipment as office products, communication products, measurement products, and home electronics products in accordance with the terms and conditions set forth in this specifications book and otherwise notified by Sony from time to time.
- You should not use the Products for critical applications which may pose a life- or injury- threatening risk or are highly likely to cause significant property damage in the event of failure of the Products. You should consult your Sony sales representative beforehand when you consider using the Products for such critical applications. In addition, you should not use the Products in weapon or military equipment.
- Sony disclaims and does not assume any liability and damages arising out of misuse, improper use, modification, use of the Products for the above-mentioned critical applications, weapon and military equipment, or any deviation from the requirements set forth in this specifications book.

Design for Safety

- Sony is making continuous efforts to further improve the quality and reliability of the Products; however, failure of a certain percentage of the Products is inevitable. Therefore, you should take sufficient care to ensure the safe design of your products such as component redundancy, anti-conflagration features, and features to prevent mis-operation in order to avoid accidents resulting in injury or death, fire or other social damage as a result of such failure.

Export Control

- If the Products are controlled items under the export control laws or regulations of various countries, approval may be required for the export of the Products under the said laws or regulations. You should be responsible for compliance with the said laws or regulations.

No License Implied

- The technical information shown in this specifications book is for your reference purposes only. The availability of this specifications book shall not be construed as giving any indication that Sony and its licensors will license any intellectual property rights in such information by any implication or otherwise. Sony will not assume responsibility for any problems in connection with your use of such information or for any infringement of third-party rights due to the same. It is therefore your sole legal and financial responsibility to resolve any such problems and infringement.

Governing Law

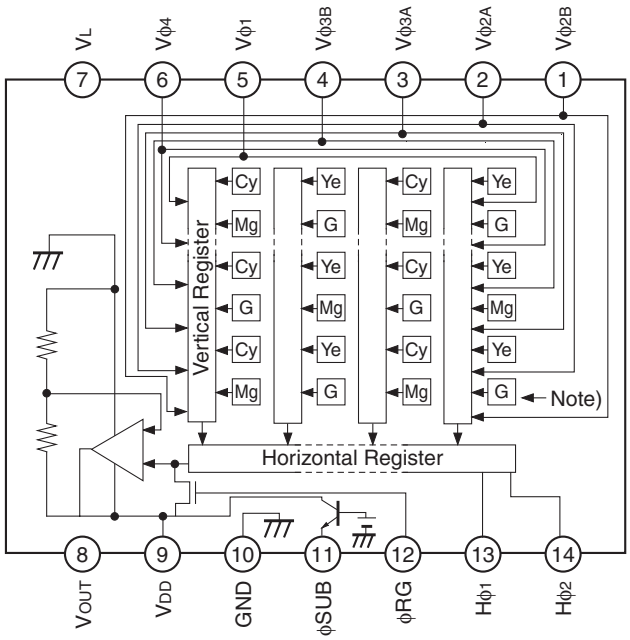
- This Notice shall be governed by and construed in accordance with the laws of Japan, without reference to principles of conflict of laws or choice of laws. All controversies and disputes arising out of or relating to this Notice shall be submitted to the exclusive jurisdiction of the Tokyo District Court in Japan as the court of first instance.

Other Applicable Terms and Conditions

- The terms and conditions in the Sony additional specifications, which will be made available to you when you order the Products, shall also be applicable to your use of the Products as well as to this specifications book. You should review those terms and conditions when you consider purchasing and/or using the Products.

Block Diagram and Pin Configuration

(Top View)



Note) □ : Photo sensor

Pin Description

Pin No.	Symbol	Description
1	Vφ2B	Vertical register transfer clock
2	Vφ2A	Vertical register transfer clock
3	Vφ3A	Vertical register transfer clock
4	Vφ3B	Vertical register transfer clock
5	Vφ1	Vertical register transfer clock
6	Vφ4	Vertical register transfer clock
7	VL	Protective transistor bias
8	VOUT	Signal output
9	VDD	Supply voltage
10	GND	GND
11	φSUB	Substrate clock
12	φRG	Reset gate clock
13	Hφ1	Horizontal register transfer clock
14	Hφ2	Horizontal register transfer clock

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against ϕSUB	V_{DD}, V_{OUT}, ϕRG – ϕSUB	–40 to +13	V	
	$V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$ – ϕSUB	–50 to +15	V	
	$V\phi_1$, $V\phi_4$ – ϕSUB	–50 to +0.3	V	
	$H\phi_1$, $H\phi_2$, GND – ϕSUB	–40 to +0.3	V	
Against GND	V_{DD}, V_{OUT}, ϕRG – GND	–0.3 to +18	V	
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$, $V\phi_4$ – GND	–10 to +18	V	
	$H\phi_1$, $H\phi_2$ – GND	–10 to +5	V	
Against V_L	$V\phi_{2A}$, $V\phi_{2B}$, $V\phi_{3A}$, $V\phi_{3B}$ – V_L	–0.3 to +28	V	
	$V\phi_1$, $V\phi_4$, $H\phi_1$, $H\phi_2$ – V_L	–0.3 to +15	V	
Between input clock pins	Potential difference between vertical clock input pins	to +15	V	*1
	$H\phi_1$ – $H\phi_2$	–5 to +5	V	
	$H\phi_1$, $H\phi_2$ – $V\phi_3$	–13 to +13	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

*1 +24V (Max.) is guaranteed when clock width < 10μs, clock duty factor < 0.1%.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	ϕSUB	*2				
Reset gate clock	ϕRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical clock waveform, or the same voltage as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated internally.

DC Characteristics

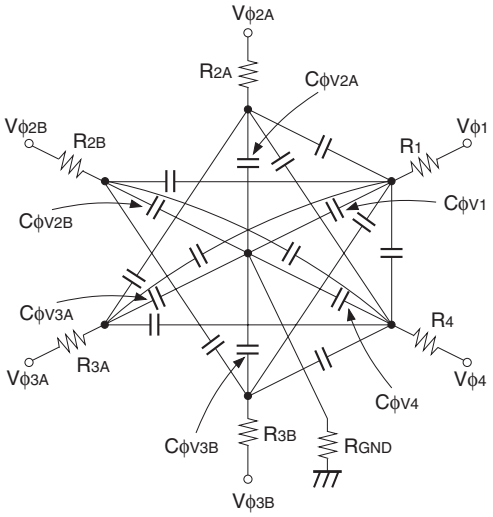
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current	I_{DD}		6.0		mA	

Clock Voltage Conditions

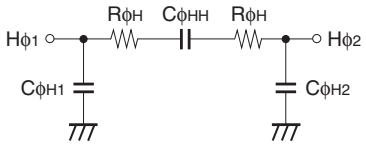
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02A}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02A}$
	V_{VH1}, $V_{VH2\,(A, B)}$, $V_{VH3\,(A, B)}$, V_{VH4}	–0.2	0	0.05	V	2	
	V_{VL1}, $V_{VL2\,(A, B)}$, $V_{VL3\,(A, B)}$, V_{VL4}	–5.8	–5.5	–5.2	V	2	$V_{VL} = (V_{VL1} + V_{VL3\,(A, B)})/2$
	$V\phi1$, $V\phi2\,(A, B)$, $V\phi3\,(A, B)$, $V\phi4$	5.0	5.5	5.85	V	2	
	$\lvert V_{VL3\,(A, B)}, V_{VL4} - V_{VL} \rvert$			0.1	V	2	
	V_{VHH}			0.3	V	2	High-level coupling
	V_{VHL}			1.0	V	2	High-level coupling
	V_{VLH}			0.5	V	2	Low-level coupling
	V_{VLL}			0.5	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi H$	3.0	3.3	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi RG$	3.0	3.3	5.5	V	4	
	$V_{RGLH} - V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} - V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi SUB$	19.75	20.5	21.25	V	5	

Clock Equivalent Circuit Constants

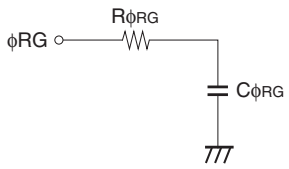
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		1000		pF	
	$C_{\phi V2A}$, $C_{\phi V2B}$		820		pF	
	$C_{\phi V3A}$, $C_{\phi V3B}$		390		pF	
	$C_{\phi V4}$		1500		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12A}$, $C_{\phi V12B}$		56		pF	
	$C_{\phi V13A}$, $C_{\phi V13B}$		2		pF	
	$C_{\phi V14}$		180		pF	
	$C_{\phi V2A3A}$, $C_{\phi V2B3B}$		220		pF	
	$C_{\phi V2A4}$, $C_{\phi V2B4}$		270		pF	
	$C_{\phi V3A4}$, $C_{\phi V3B4}$		180		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$		15		pF	
	$C_{\phi H2}$		15		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		47		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		5		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		270		pF	
Vertical transfer clock series resistor	R_1		47		Ω	
	R_{2A}, R_{2B}		91		Ω	
	R_{3A}, R_{3B}		68		Ω	
	R_4		24		Ω	
Vertical transfer clock ground resistor	R_{GND}		47		Ω	
Horizontal transfer clock series resistor	$R_{\phi H1}$, $R_{\phi H2}$		15		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		56		Ω	



Vertical transfer clock equivalent circuit



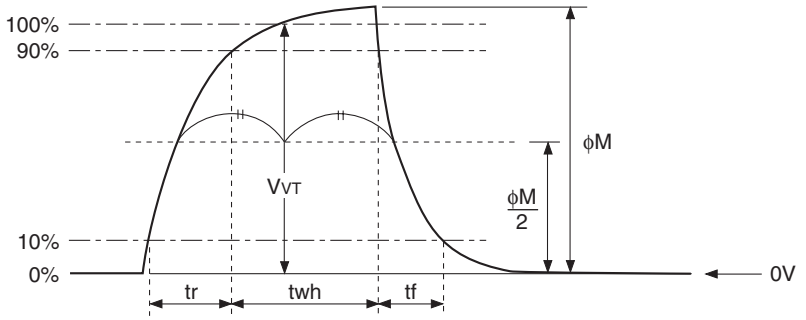
Horizontal transfer clock equivalent circuit



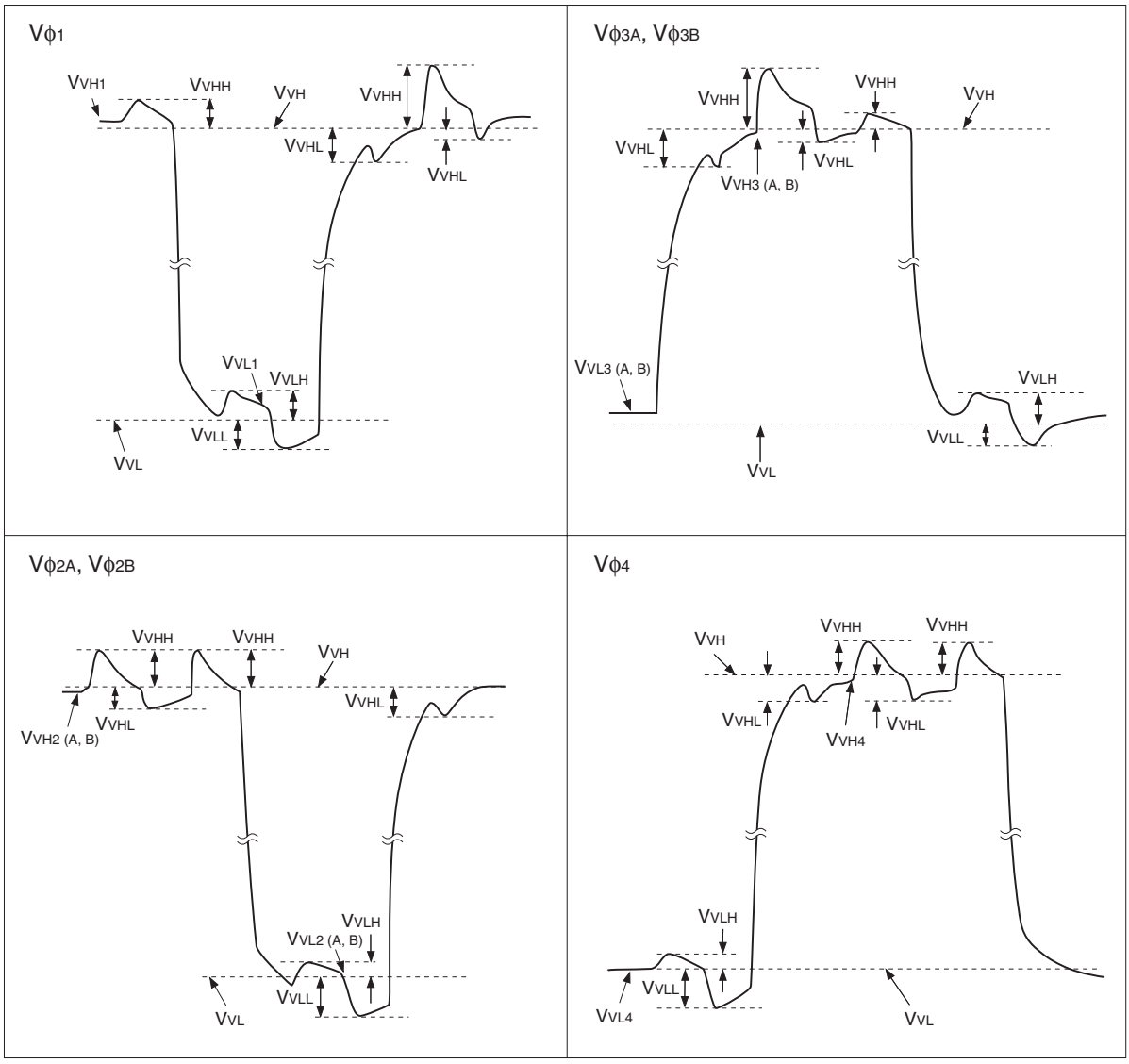
Reset gate clock equivalent circuit

Drive Clock Waveform Conditions

1. Readout clock waveform

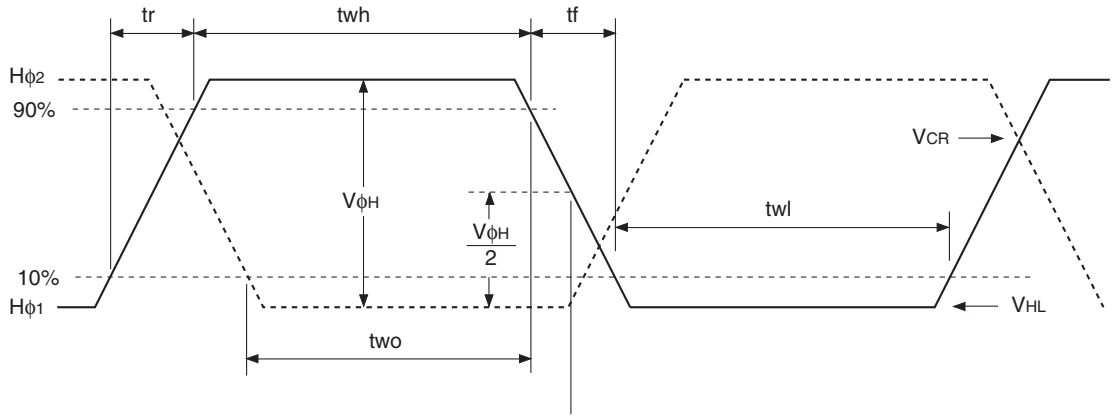


2. Vertical transfer clock waveform



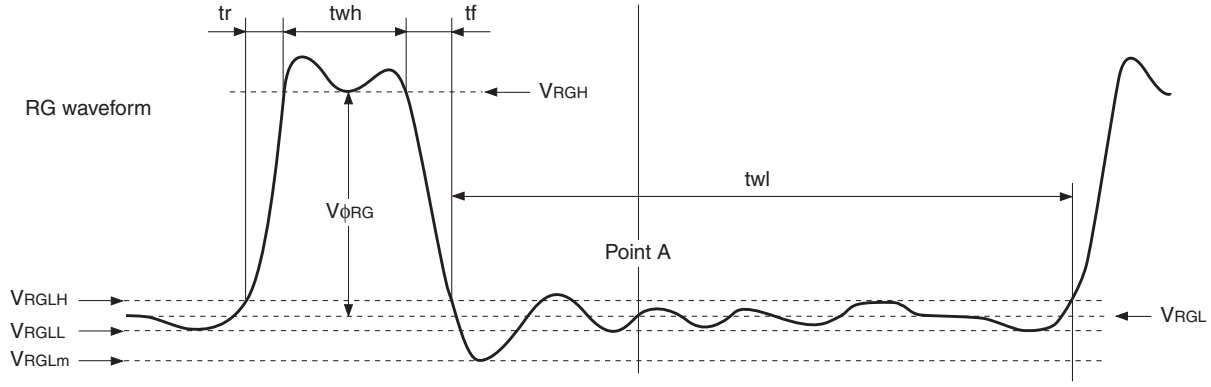
$V_{VH} = (V_{VH1} + V_{VH2\,(A,\,B)})/2$
$V_{VL} = (V_{VL3\,(A,\,B)} + V_{VL4})/2$
$V_{\phi V} = V_{VHn} - V_{VLn}$ (n = 1 to 4)

3. Horizontal transfer clock waveform



Cross-point voltage for the Hϕ1 rising side of the horizontal transfer clocks Hϕ1 and Hϕ2 waveforms is VCR.
The overlap period for twh and twl of horizontal transfer clocks Hϕ1 and Hϕ2 is “two”.

4. Reset gate clock waveform



VRGLH is the maximum value and VRGLL is the minimum value of the coupling waveform during the period from Point A in the above diagram until the rising edge of RG.
In addition, VRGL is the average value of VRGLH and VRGLL.

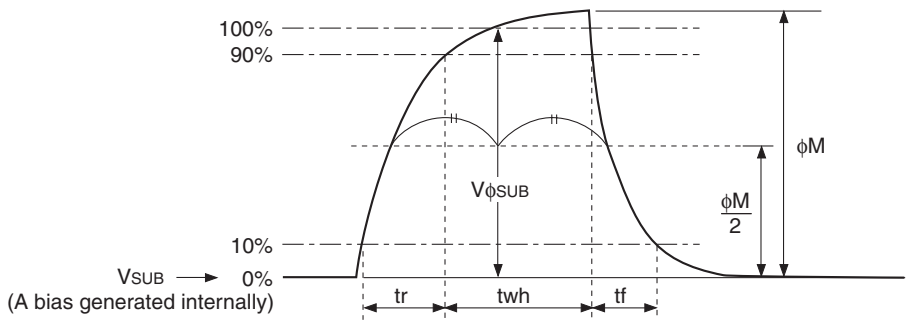
$V_{RGL} = (V_{RGLH} + V_{RGLL})/2$

Assuming VRGH is the minimum value during the interval twh, then:

$V_{\phi RG} = V_{RGH} - V_{RGL}$

Negative overshoot level during the falling edge of RG is VRGLm.

5. Substrate clock waveform



Clock Switching Characteristics

Item		Symbol	twh			twl			tr			tf			Unit	Remarks
			Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.		
Readout clock		V_T	1.8	2.0						0.5			0.5		μs	During readout
Vertical transfer clock		$V\phi1$, $V\phi2_{(A,B)}$, $V\phi3_{(A,B)}$, $V\phi4$										15		250	ns	*1
Horizontal transfer clock	During imaging	$H\phi1$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5	ns	*2
		$H\phi2$	10.5	14.6		10.5	14.6			6.4	10.5		6.4	10.5		
	During parallel-serial conversion	$H\phi1$								0.001					μs	
		$H\phi2$								0.001						
Reset gate clock		ϕRG	6	8			25.8			4			3		ns	
Substrate clock		ϕSUB	0.63	0.73							0.5			0.5	μs	When draining charge

*1 When vertical transfer clock driver CXD1267AN is used.

*2 $tf \geq tr - 2ns$, and the cross-point voltage (V_{CR}) for the $H\phi1$ rising side of the $H\phi1$ and $H\phi2$ waveforms must be at least $V\phi H/2$[V].

Item	Symbol	two			Unit	Remarks
		Min.	Typ.	Max.		
Horizontal transfer clock	$H\phi1$, $H\phi2$	10.5	14.6		ns	

Spectral Sensitivity Characteristics

(excludes lens characteristics and light source characteristics)

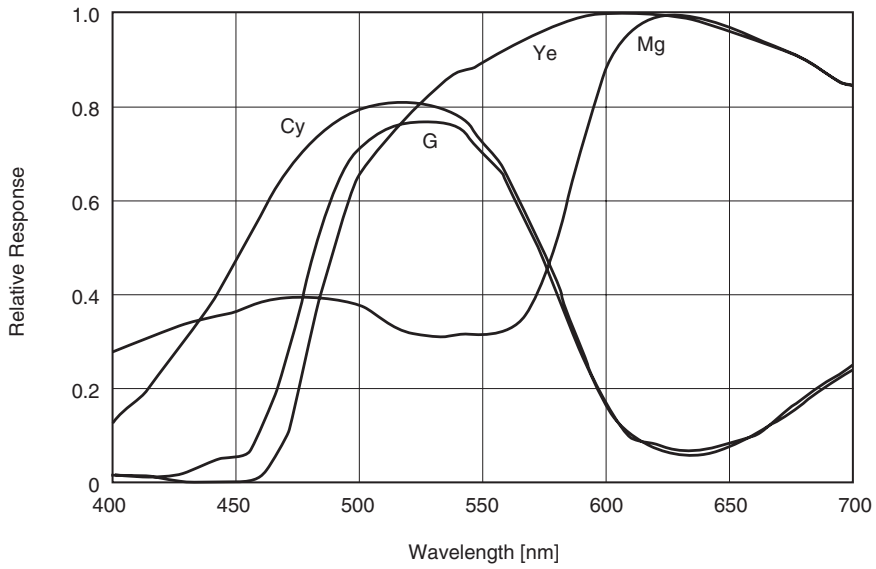
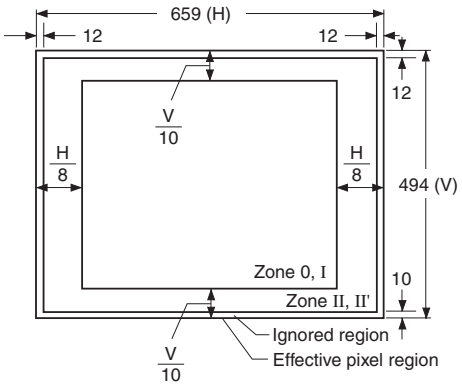


Image Sensor Characteristics

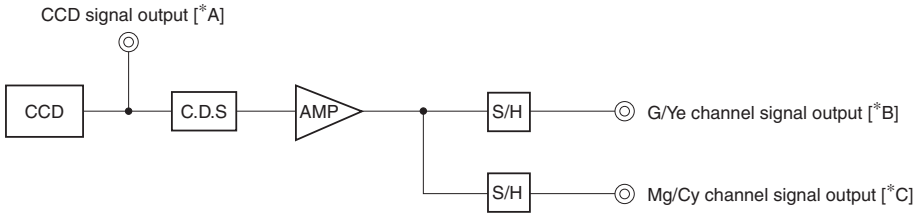
(Ta = 25℃)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement method	Remarks
Sensitivity	S	1120	1400		mV	1	1/30s accumulation
Sensitivity ratio	R_{MgG}	0.93		1.35		1	
	R_{YeCy}	1.19		1.57		1	
Saturation signal	Vsat	800			mV	2	Ta = 60℃
Smear	Sm		– 110	– 100	dB	3	
Video signal shading	SHy			20	%	4	Zone 0 and I
				25	%	4	Zone 0 to II'
Uniformity between video signal channels	ΔSr			10	%	5	
	ΔSb			10	%	5	
Dark signal	Vdt			4	mV	6	Ta = 60℃, 1/30s accumulation
Dark signal shading	ΔVdt			1	mV	7	Ta = 60℃, 1/30s accumulation
Line crawl R	Lcr			3	%	8	
Line crawl G	Lcg			3	%	8	
Line crawl B	Lcb			3	%	8	
Line crawl W	Lcw			3	%	8	
Lag	Lag			0.5	%	9	

Zone Definition of Video Signal Shading



Measurement System



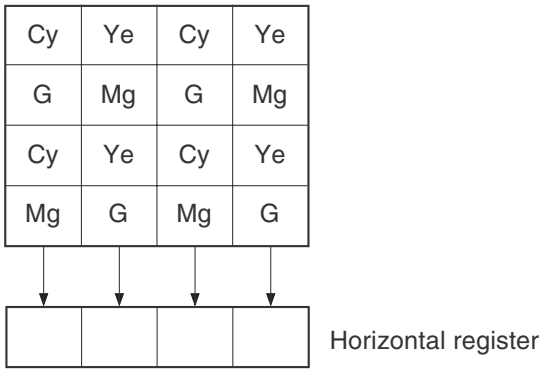
Note) Adjust the amplifier gain so that the gain between [*A] and [*B], and between [*A] to [*C] equals 1.

Image Sensor Characteristics Measurement Method

Measurement conditions

1. In the following measurements, the device drive conditions are at the typical values of the bias and clock voltage conditions.
2. In the following measurements, spot pixels are excluded and, unless otherwise specified, the optical black level (OB) is used as the reference for the signal output, which is taken as the value of the G/Ye channel signal output or the Mg/Cy channel signal output of the measurement system.

Color coding of this image sensor & Composition of luminance (Y) and chroma (color difference) signals



Color Coding Diagram

The complementary color filters of this image sensor are arranged in the layout shown in the figure above.

These signals are processed to form the Y signal and chroma (color difference) signal as follows.
The approximation;

$$V = (G + Mg + Ye + Cy)/4$$
$$= (2B + 3G + 2R)/4$$

is used for the Y signal, and the approximation;

$$R - Y = \{(Mg + Ye) - (G + Cy)\}$$
$$= 2R - G$$
$$B - Y = \{(Mg + Cy) - (G + Ye)\}$$
$$= 2B - G$$

are used for the chroma (color difference) signal.

Definition of standard imaging conditions

◆ Standard imaging condition I:
Use a pattern box (luminance: 706cd/m^2, color temperature of 3200K halogen source) as a subject. (Pattern for evaluation is not applicable.) Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter and image at F5.6. The luminous intensity to the sensor receiving surface at this point is defined as the standard sensitivity testing luminous intensity.

◆ Standard imaging condition II:
Image a light source (color temperature of 3200K) with a uniformity of brightness within 2% at all angles. Use a testing standard lens with CM500S (t = 1.0mm) as an IR cut filter. The luminous intensity is adjusted to the value indicated in each testing item by the lens diaphragm.

1. Sensitivity, sensitivity ratio
Set to the standard imaging condition I. After setting the electronic shutter mode with a shutter speed of 1/100s, measure the signal outputs (V_G, V_{Mg}, V_{Ye} and V_{Cy}) at the center of each G, Mg, Ye and Cy channel screen, and substitute the values into the following formulas.

$V = (V_G + V_{Mg} + V_{Ye} + V_{Cy})/4$
$S = V \times (100/30)$ [mV]
$R_{MgG} = V_{Mg}/V_G$
$R_{YeCy} = V_{Ye}/V_{Cy}$

2. Saturation signal
Set to the standard imaging condition II. After adjusting the luminous intensity to 10 times the intensity with the average value of the Y signal output, 150mV, measure the minimum values of the G, Mg, Ye and Cy signal outputs.

3. Smear
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, first adjust the average value of the Y signal output to 150mV. After the readout clock is stopped and the charge drain is executed by the electronic shutter at the respective H blankings, measure the maximum value (Vsm [mV]) independent of the G, Mg, Ye and Cy signal outputs, and substitute the values into the following formula.

$Sm = 20 \times \log \{(Vsm/150) \times (1/500) \times (1/10)\}$ [dB] (1/10V method conversion value)

4. Video signal shading
Set to the standard imaging condition II. With the lens diaphragm at F5.6 to F8, adjusting the luminous intensity so that the average value of the Y signal output is 150mV. Then measure the maximum value (Vmax [mV]) and minimum value (Vmin [mV]) of the Y signal and substitute the values into the following formula.

$SHy = (Vmax - Vmin)/150 \times 100$ [%]

5. Uniformity between video signal channels
Set to the standard imaging condition II. Adjust the luminous intensity so that the average value of the Y signal output is 150mV, and then measure the maximum (Crmax, Cbmax [mV]) and minimum (Crmin, Cbmin [mV]) values of the R – Y and B – Y channels of the chroma signal and substitute the values into the following formula.

$\Delta Sr = |(Crmax - Crmin)/150| \times 100$ [%]
$\Delta Sb = |(Cbmax - Cbmin)/150| \times 100$ [%]

6. Dark signal
Measure the average value of the Y signal output (Vdt [mV]) with the device ambient temperature of 60°C and the device in the light-obstructed state, using the horizontal idle transfer level as a reference.

7. Dark signal shading
After the measurement item 6, measure the maximum (Vdmax [mV]) and minimum (Vdmin [mV]) values of the dark signal output and substitute the values into the following formula.

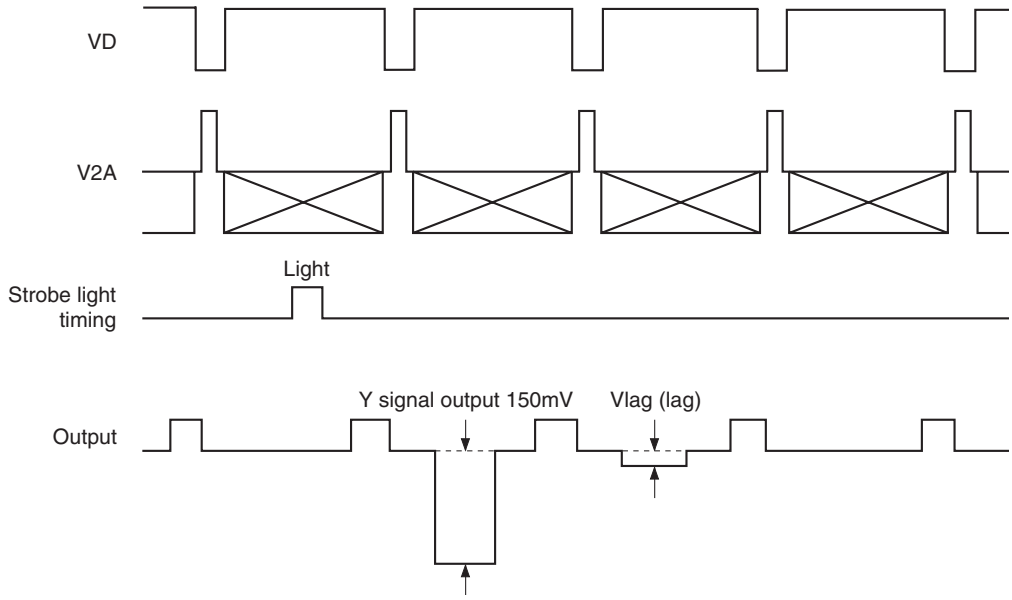
$\Delta Vdt = Vdmax - Vdmin$ [mV]

8. Line crawl
   Set to the standard imaging condition II. Adjusting the luminous intensity so that the average value of the Y signal output is 150mV, and then insert R, G and B filters and measure the difference between Y signal lines (ΔVlw, ΔVlr, ΔVlg, ΔVlb [mV]). Substitute the values into the following formula.

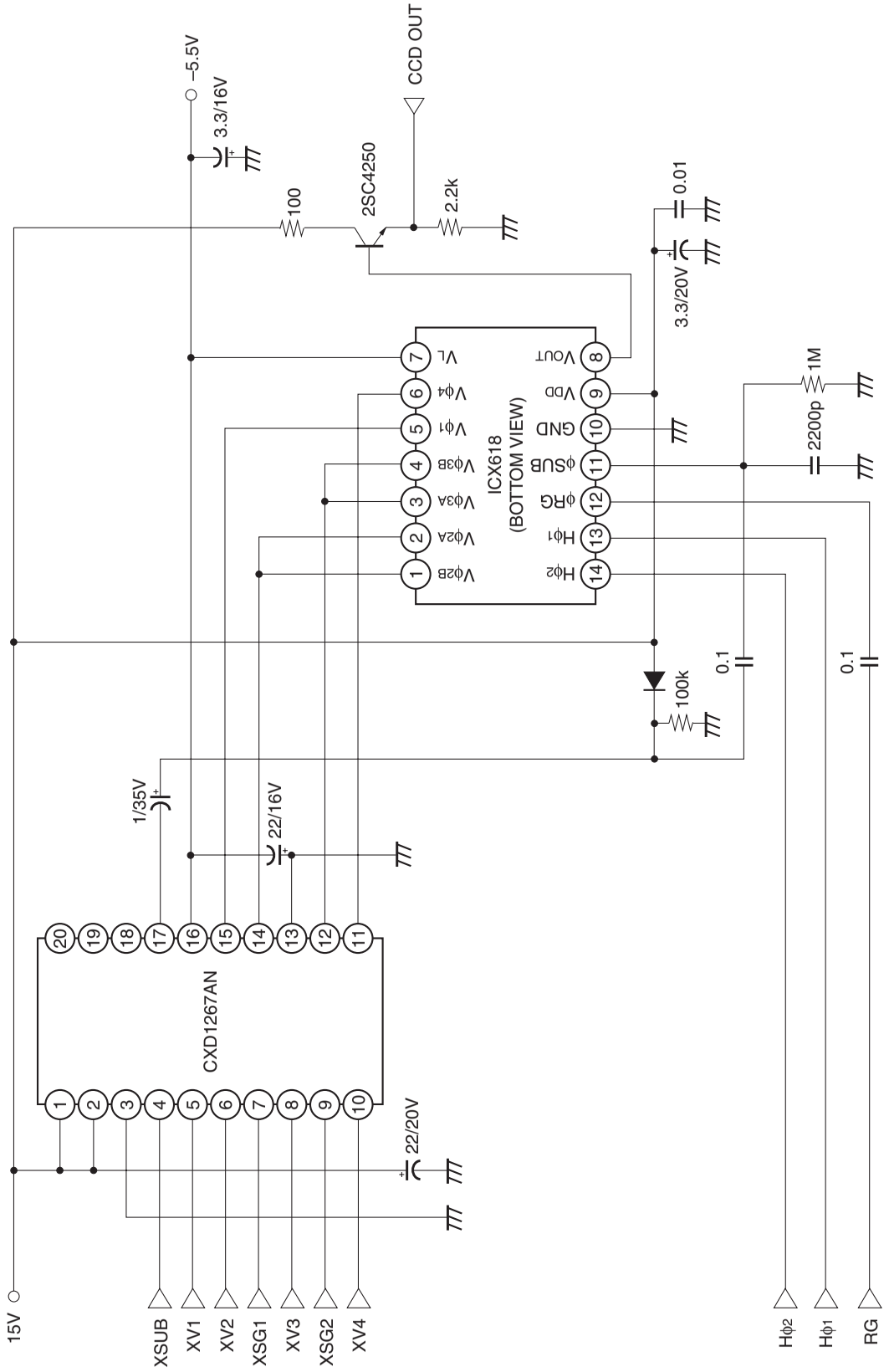
   Lc*i* = (ΔVl*i* /150) × 100 [%] (*i* = w, r, g, b)

9. Lag
   Adjust the Y signal output value generated by strobe light to 150mV. After setting the strobe light so that it strobes with the following timing, measure the residual signal (Vlag). Substitute the value into the following formula.

   Lag = (Vlag/150) × 100 [%]

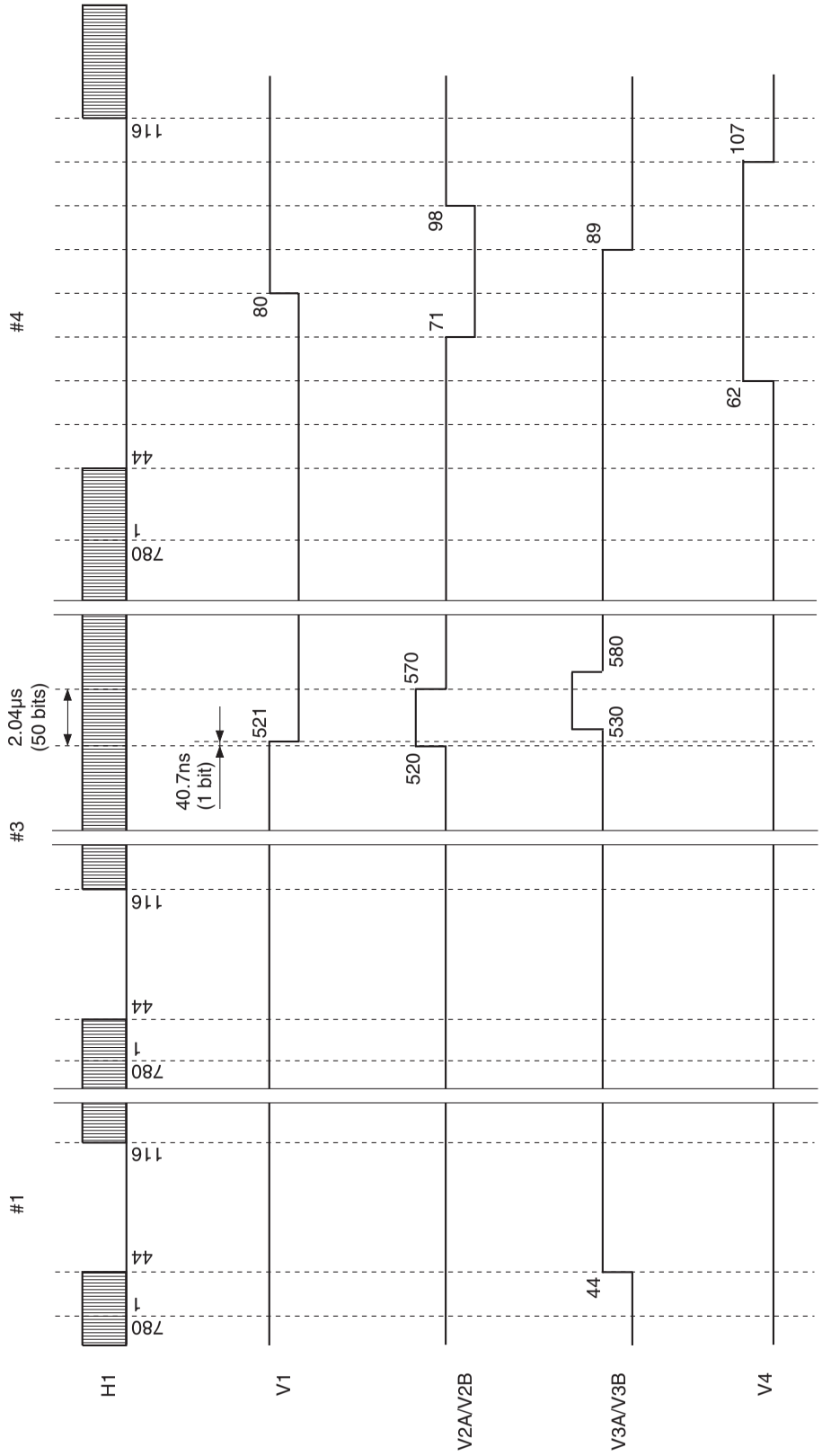


Driving Circuit



Drive Timing Chart

Readout Portion

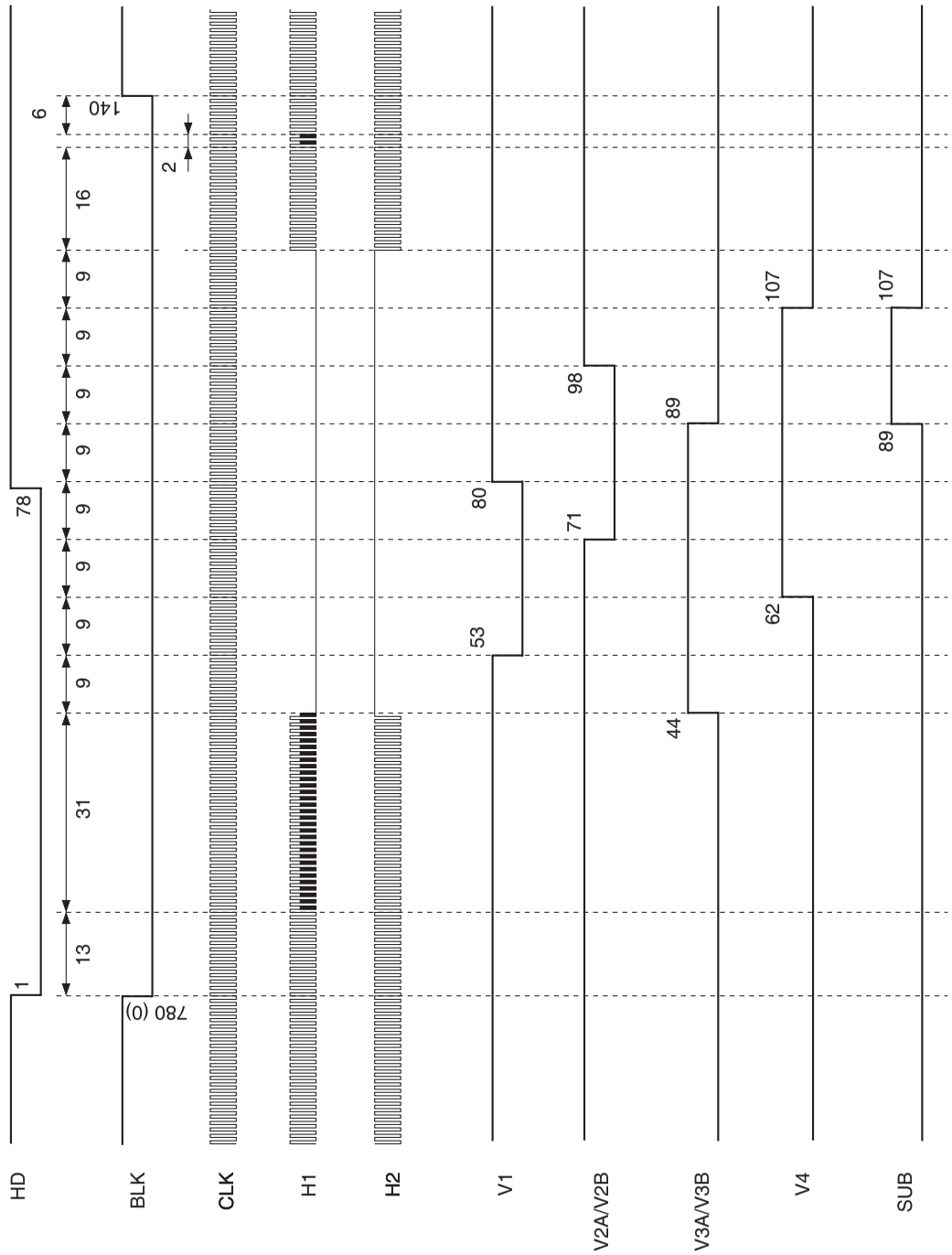


Drive Timing Chart

Vertical Sync

Drive Timing Chart

Horizontal Sync



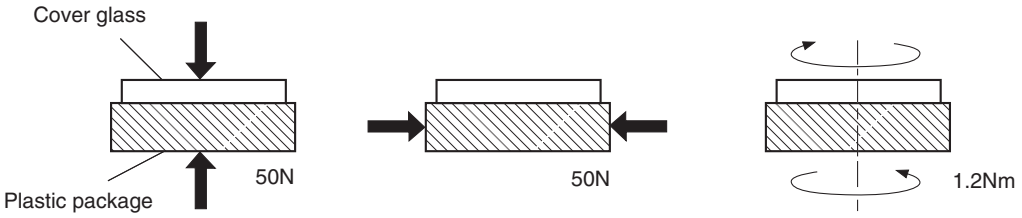
Notes On Handling

1. Static charge prevention
   CCD image sensors are easily damaged by static discharge. Before handling be sure to take the following protective measures.
   (1) Either handle bare handed or use non-chargeable gloves, clothes or material.
   Also use conductive shoes.
   (2) Use a wrist strap when handling directly.
   (3) Install grounded conductive mats on the floor and working table to prevent the generation of static electricity.
   (4) Ionized air is recommended for discharge when handling CCD image sensors.
   (5) For the shipment of mounted boards, use boxes treated for the prevention of static charges.

2. Soldering
   (1) Make sure the package temperature does not exceed 80°C.
   (2) Solder dipping in a mounting furnace causes damage to the glass and other defects. Use a 30W soldering iron with a ground wire and solder each pin in 2 seconds or less. For repairs and remount, cool sufficiently.
   (3) To dismount an image sensor, do not use solder suction equipment. When using an electric desoldering tool, use a thermal controller of the zero-cross On/Off type and connect it to ground.

3. Protection from dust and dirt
   Image sensors are packed and delivered with care taken to protect the element glass surfaces from harmful dust and dirt. Clean glass surfaces with the following operations as required before use.
   (1) Perform all lens assembly and other work in a clean room (class 1000 or less).
   (2) Do not touch the glass surface with hand and make any object contact with it. If dust or other is stuck to a glass surface, blow it off with an air blower. (For dust stuck through static electricity, ionized air is recommended.)
   (3) Clean with a cotton bud and ethyl alcohol if grease stained. Be careful not to scratch the glass.
   (4) Keep in a dedicated case to protect from dust and dirt. To prevent dew condensation, preheat or precool when moving to a room with great temperature differences.
   (5) When a protective tape is applied before shipping, remove the tape applied for electrostatic protection just before use. Do not reuse the tape.

4. Installing (attaching)
   (1) Remain within the following limits when applying a static load to the package. Do not apply any load more than 0.7mm inside the outer perimeter of the glass portion, and do not apply any load or impact to limited portions. (This may cause cracks in the package.)



Compressive strength **Torsional strength**

   (2) If a load is applied to the entire surface by a hard component, bending stress may be generated and the package may fracture, etc., depending on the flatness of the bottom of the package. Therefore, for installation, use either an elastic load, such as a spring plate, or an adhesive.
   (3) The adhesive may cause the marking on the rear surface to disappear, especially in case the regulated voltage value is indicated on the rear surface. Therefore, the adhesive should not be applied to this area, and indicated values should be transferred to the other locations as a precaution.
   (4) The notch of the package is used for directional index, and that can not be used for reference of fixing. In addition, the cover glass and seal resin may overlap with the notch of the package.

(5) If the lead bend repeatedly and the metal, etc., clash or rub against the package, dust may be generated by the fragments of resin.

(6) Acrylate anaerobic adhesives are generally used to attach CCD image sensors. In addition, cyanoacrylate instantaneous adhesives are sometimes used jointly with acrylate anaerobic adhesives. (reference)

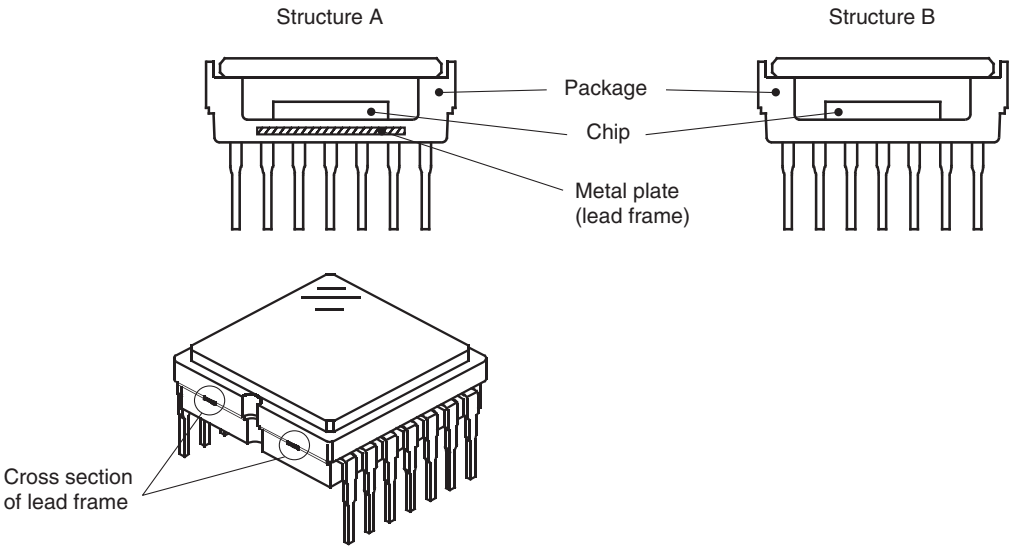
5. Others

(1) Do not expose to strong light (sun rays) for long periods, as color filters will be discolored. When high luminance objects are imaged with the exposure level controlled by electronic-iris, the luminance of the image-plane may become excessive and discoloration of the color filters may be accelerated. In such a case, arrangements such as using an automatic iris with the imaging lens or automatically closing the shutter during power-off are advisable. For continuous use under harsh conditions exceeding the normal conditions of use, consult your Sony representative.

(2) Exposure to high temperature or humidity will affect the characteristics. Accordingly avoid storage or use in such conditions.

(3) Brown stains may be seen on the bottom or side of the package. But this does not affect the CCD characteristics.

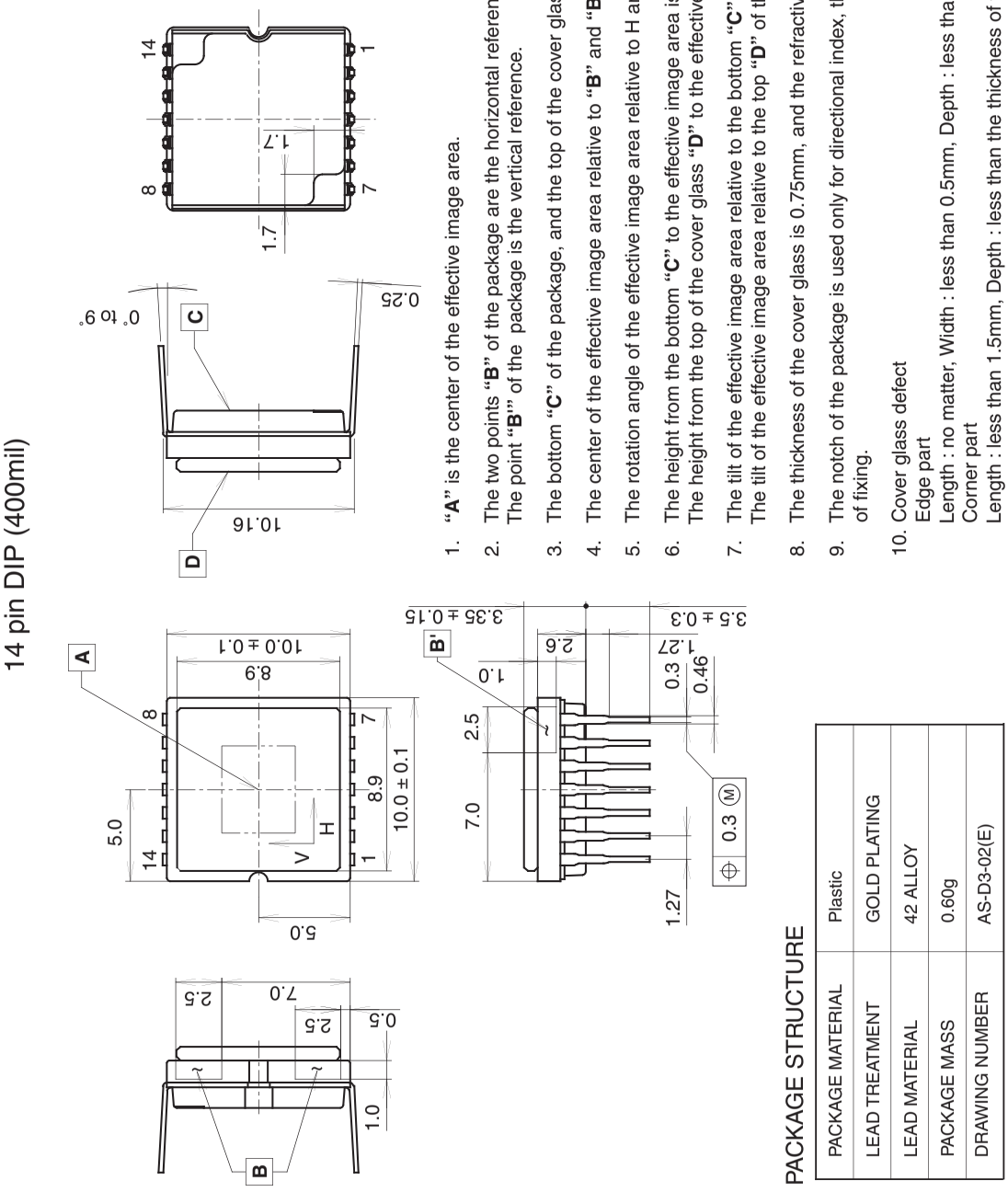
(4) This package has 2 kinds of internal structure. However, their package outline, optical size, and strength are the same.



The cross section of lead frame can be seen on the side of the package for structure A.

Package Outline

(Unit: mm)



1. **"A"** is the center of the effective image area.
2. The two points **"B"** of the package are the horizontal reference.
   The point **"B'"** of the package is the vertical reference.
3. The bottom **"C"** of the package, and the top of the cover glass **"D"** are the height reference.
4. The center of the effective image area relative to **"B"** and **"B'"** is (H, V) = (5.0, 5.0) ± 0.15mm.
5. The rotation angle of the effective image area relative to H and V is ± 1°.
6. The height from the bottom **"C"** to the effective image area is 1.41 ± 0.10mm.
   The height from the top of the cover glass **"D"** to the effective image area is 1.94 ± 0.15mm.
7. The tilt of the effective image area relative to the bottom **"C"** is less than 25µm.
   The tilt of the effective image area relative to the top **"D"** of the cover glass is less than 25µm.
8. The thickness of the cover glass is 0.75mm, and the refractive index is 1.5.
9. The notch of the package is used only for directional index, that must not be used for reference of fixing.
10. Cover glass defect
    Edge part
    Length : no matter, Width : less than 0.5mm, Depth : less than the thickness of the glass.
    Corner part
    Length : less than 1.5mm, Depth : less than the thickness of the glass.

PACKAGE STRUCTURE

PACKAGE MATERIAL	Plastic
LEAD TREATMENT	GOLD PLATING
LEAD MATERIAL	42 ALLOY
PACKAGE MASS	0.60g
DRAWING NUMBER	AS-D3-02(E)