SONY

Diagonal 8mm (Type 1/2) Progressive Scan CCD Image Sensor with Square Pixel for B/W Cameras

ICX267AL

Description

The ICX267AL is a diagonal 8mm (Type 1/2) interline CCD solid-state image sensor with a square pixel array and 1.45M effective pixels. Progressive scan allows all pixels' signals to be output independently. Also, the adoption of high frame rate readout mode supports 30 frames per second. This chip features an electronic shutter with variable charge-storage time which makes it possible to realize full-frame still image without a mechanical shutter. High resolution and high low dark current are achieved through the adoption of HAD (Hole-Accumulation Diode) sensors.
(Applications: Electronic still cameras, PC input cameras, etc.)

Features

- ◆ Progressive scan allows individual readout of the image signals from all pixels.
- ◆ High horizontal and vertical resolution (both approx. 1024TV-lines) still image without a mechanical shutter.
- ◆ Supports high frame rate readout mode (effective 512 lines output, 30 frames/s)
- ◆ Square pixel
- ◆ Horizontal drive frequency: 28.636MHz
- ◆ No voltage adjustments (Reset gate and substrate bias need no adjustment.)
- ◆ High resolution, high color reproductivity, high sensitivity, low dark current
- ◆ Low smear, excellent antiblooming characteristics
- ◆ Continuous variable-speed shutter

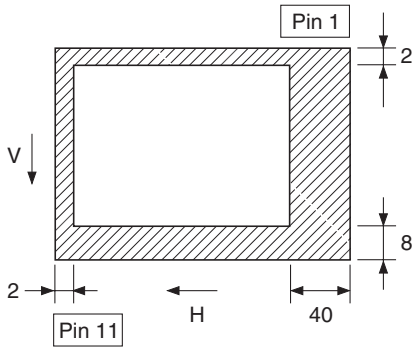
E01Y03C88-CR

Device Structure

- ◆ Interline CCD image sensor
- ◆ Image size : Diagonal 8mm (Type 1/2)
- ◆ Total number of pixels : 1434 (H) × 1050 (V) approx. 1.50M pixels
- ◆ Number of effective pixels : 1392 (H) × 1040 (V) approx. 1.45M pixels
- ◆ Number of active pixels : 1360 (H) × 1024 (V) approx. 1.40M pixels (7.959mm diagonal)
- ◆ Chip size : 7.60mm (H) × 6.20mm (V)
- ◆ Unit cell size : 4.65μm (H) × 4.65μm (V)
- ◆ Optical black : Horizontal (H) direction : Front 2 pixels, rear 40 pixels
  Vertical (V) direction : Front 8 pixels, rear 2 pixels
- ◆ Number of dummy bits : Horizontal 20
  Vertical 3
- ◆ Substrate material : Silicon

Optical Black Position

(Top View)



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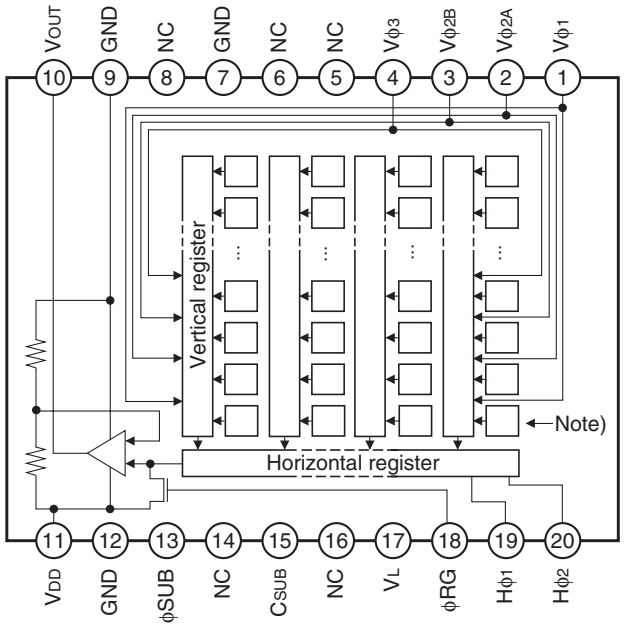
Block Diagram and Pin Configuration

(Top View)



Note) : Photo sensor

Pin Description

Pin No.	Symbol	Description	Pin No.	Symbol	Description
1	Vφ1	Vertical register transfer clock	11	VDD	Supply voltage
2	Vφ2A	Vertical register transfer clock	12	GND	GND
3	Vφ2B	Vertical register transfer clock	13	φSUB	Substrate clock
4	Vφ3	Vertical register transfer clock	14	NC	
5	NC		15	CSUB	Substrate bias*1
6	NC		16	NC	
7	GND	GND	17	VL	Protective transistor bias
8	NC		18	φRG	Reset gate clock
9	GND	GND	19	Hφ1	Horizontal register transfer clock
10	VOUT	Signal output	20	Hφ2	Horizontal register transfer clock

*1 DC bias is generated within the CCD, so that this pin should be grounded externally through a capacitance of 0.1μF.

Absolute Maximum Ratings

Item		Ratings	Unit	Remarks
Against φSUB	V_{DD}, V_{OUT}, φRG – φSUB	–40 to +10	V	
	$V_{\phi 2A}$, $V_{\phi 2B}$ – φSUB	–50 to +15	V	
	$V_{\phi 1}$, $V_{\phi 3}$, V_L – φSUB	–50 to +0.3	V	
	$H_{\phi 1}$, $H_{\phi 2}$, GND – φSUB	–40 to +0.3	V	
	C_{SUB} – φSUB	–25 to	V	
Against GND	V_{DD}, V_{OUT}, φRG, C_{SUB} – GND	–0.3 to +18	V	
	$V_{\phi 1}$, $V_{\phi 2A}$, $V_{\phi 2B}$, $V_{\phi 3}$ – GND	–10 to +18	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – GND	–10 to +15	V	
Against V_L	$V_{\phi 2A}$, $V_{\phi 2B}$ – V_L	–0.3 to +28	V	
	$V_{\phi 1}$, $V_{\phi 3}$, $H_{\phi 1}$, $H_{\phi 2}$, GND – V_L	–0.3 to +15	V	
Between input clock pins	Voltage difference between vertical clock input pins	to +15	V	*1
	$H_{\phi 1}$ – $H_{\phi 2}$	–16 to +16	V	
	$H_{\phi 1}$, $H_{\phi 2}$ – $V_{\phi 3}$	–16 to +16	V	
Storage temperature		–30 to +80	℃	
Operating temperature		–10 to +60	℃	

*1 +24V (Max.) when clock width < 10μs, clock duty factor < 0.1%.
+16V (Max.) is guaranteed for turning on or off power supply.

Bias Conditions

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power Supply voltage	V_{DD}	14.55	15.0	15.45	V	
Protective transistor bias	V_L	*1				
Substrate clock	φSUB	*2				
Reset gate clock	φRG	*2				

*1 V_L setting is the V_{VL} voltage of the vertical transfer clock waveform, or the same power supply as the V_L power supply for the V driver should be used.

*2 Do not apply a DC bias to the substrate clock and reset gate clock pins, because a DC bias is generated within the CCD.

DC Characteristics

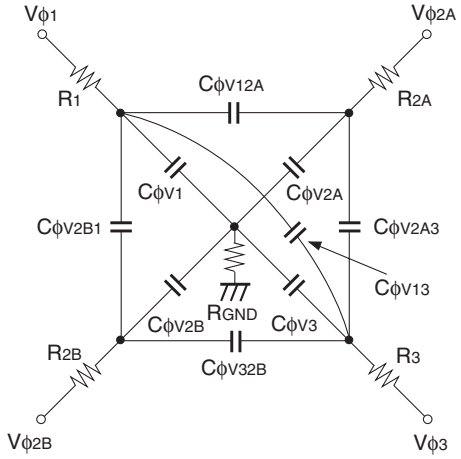
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Power supply current	I_{DD}		7.7		mA	

Clock Voltage Conditions

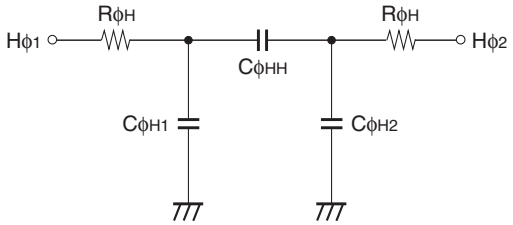
Item	Symbol	Min.	Typ.	Max.	Unit	Waveform diagram	Remarks
Readout clock voltage	V_{VT}	14.55	15.0	15.45	V	1	
Vertical transfer clock voltage	V_{VH02A}	–0.05	0	0.05	V	2	$V_{VH} = V_{VH02A}$
	V_{VH1}, V_{VH2A}, V_{VH2B}, V_{VH3}	–0.2	0	0.05	V	2	
	V_{VL1}, V_{VL2A}, V_{VL2B}, V_{VL3}	–8.4	–8.0	–7.6	V	2	$V_{VL} = (V_{VL1} + V_{VL3})/2$
	$V\phi_1$, $V\phi_{2A}$, $V\phi_{2B}$, $V\phi_3$	7.6	8.0	8.4	V	2	
	$\lvert V_{VL1} – V_{VL3} \rvert$			0.1	V	2	
	V_{VHH}			0.9	V	2	High-level coupling
	V_{VHL}			1.3	V	2	High-level coupling
	V_{VLH}			1.0	V	2	Low-level coupling
	V_{VLL}			0.9	V	2	Low-level coupling
Horizontal transfer clock voltage	$V\phi_H$	4.75	5.0	5.25	V	3	
	V_{HL}	–0.05	0	0.05	V	3	
Reset gate clock voltage	$V\phi_{RG}$	3.0	3.3	5.5	V	4	
	$V_{RGLH} – V_{RGLL}$			0.4	V	4	Low-level coupling
	$V_{RGL} – V_{RGLm}$			0.5	V	4	Low-level coupling
Substrate clock voltage	$V\phi_{SUB}$	22.15	23.0	23.85	V	5	

Clock Equivalent Circuit Constant

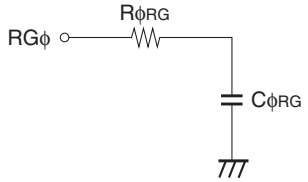
Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Capacitance between vertical transfer clock and GND	$C_{\phi V1}$		2200		pF	
	$C_{\phi V2A}$		3300		pF	
	$C_{\phi V2B}$		3300		pF	
	$C_{\phi V3}$		3300		pF	
Capacitance between vertical transfer clocks	$C_{\phi V12A}$, $C_{\phi V2B1}$		1200		pF	
	$C_{\phi V2A3}$, $C_{\phi V32B}$		1200		pF	
	$C_{\phi V13}$		2200		pF	
Capacitance between horizontal transfer clock and GND	$C_{\phi H1}$, $C_{\phi H2}$		47		pF	
Capacitance between horizontal transfer clocks	$C_{\phi HH}$		100		pF	
Capacitance between reset gate clock and GND	$C_{\phi RG}$		8		pF	
Capacitance between substrate clock and GND	$C_{\phi SUB}$		680		pF	
Vertical transfer clock series resistor	R_1		36		Ω	
	R_{2A}, R_3		56		Ω	
	R_{2B}		56		Ω	
Vertical transfer clock ground resistor	R_{GND}		30		Ω	
Horizontal transfer clock series resistor	$R_{\phi H}$		15		Ω	
Reset gate clock series resistor	$R_{\phi RG}$		20		Ω	



Vertical transfer clock equivalent circuit



Horizontal transfer clock equivalent circuit



Reset gate clock equivalent circuit