

Endicott Research Group, Inc.

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Specifications and Applications Information

05/04/12 Preliminary

The ERG SmartBridge Series is designed to "bridge the gap" in current LCD systems when transistioning from an OEM CCFL backlit LCD to an OEM LED LCD panel with a built-in driver taking into consideration the parameters of the existing power setup. The result is a complete plug-and-play setup transitioning the design towards the new LED backlit LCD.

The ERG SBDCD4213F is specifically designed for applications requiring a step-up conversion from a 5 Volt DC supply to a 12 Volt DC source. The SBDCD4213F passes through both the Enable signal and ground. The SBDCD4213F utilizes the analog Control signal to convert it to a Pulse Width Modulated (PWM) dimming signal to the OEM panel driver. The connection to the panel is completed by an integration harness.

Designed, manufactured and supported within the USA, the SBDCD4213F features:

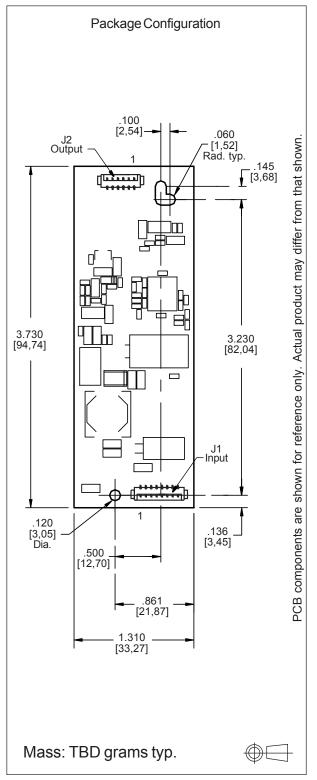
- ✓ Less than 11 mm in height
- ✓ Provides up to 255:1 dimming range
- ✓ One year warranty
- ✓ Soft start
- ✓ Custom footprints are available

Connectors					
Input Connector	Output Connector				
Molex 53261-0871	Molex 53261-0671				
J1-1 Vin(+5 Vdc) J1-2 Vin(+5 Vdc) J1-3 GND J1-4 GND J1-5 Enable J1-6 Control J1-7 N/C J1-8 N/C	J2-1 Vout(+12 Vdc) J2-2 Vout(+12 Vdc) J2-3 GND J2-4 GND J2-5 Enable J2-6 PWM Out				
Recommended input harness: H1308460F - flying lead input harness or H5106305 - DV to ERG input harness					

SBDCD4213F



SmartBridge DC-DC Converter with Integrated PWM Dimming





SBDCD4213F



Absolute Maximum Ratings

Rating	Symbol	Value	Units
Input Voltage Range	V _{in}	-0.3 to +6.0	Vdc
Storage Temperature	T _{stg}	-40 to +85	°C
Control Input Voltage	V _{PWM}	0 to +5.0	Vdc

Operating Characteristics

Unless otherwise noted Vin = 5.00 Volts dc and Ta = 25°C.

Characteristic	Symbol	Min	Тур	Max	Units			
Input Voltage	V _{in}	+4.5	+5.0	+5.5	Vdc			
Component Surface Temperature	T _s	-40	-	+80	°C			
Input Current	I _{in}	0.5	0.6	0.7	Adc			
Peak Inrush Current (Note 1)	I _{peak}	0	2.0	-	Adc			
Control Pin (Notes 2,3)								
Full-on Threshold	V _{thon}	-	1	-	Vdc			
Minimum Pulse Width Threshold	V _{PWmin}	-	4.5	-	Vdc			
Minimum Pulse Width Period	T _{PWmin}	-	16	-	µsec			
Input Impedance to GND	Z _{in}	-	10k	-	Ohms			
Frequency	F _{PWM}	-	245	-	Hz			
PWM Out								
Output ON Voltage	V _{on}	3.8	4.3	4.8	Vdc			
Output OFF Voltage	V _{off}	0	0.3	0.8	Vdc			
Output Current	I _{out}	-15	-	15	mAdc			
Vout (+12 Vdc)								
Output Voltage	V _{out}	11.4	12.0	12.6	Vdc			
Output Current	I _{out}	0	0.20	0.45	Adc			
Output Voltage Ripple (Note 4)	V _{rip}	-	0.07	-	Vrms			
Load Regulation (Note 4)	I _{reg}	-	±0.25	-	%			
Efficiency	η	-	80	-	%			

Specifications subject to change without notice.

Note 1 At full load for 5ms duration.

Note 2 Control pin is internally pulled to ground.

Note 3 Control pin input impedance is $4.3k\Omega$.

Note 4 At full load.



SBDCD4213F



Application Information

The ERG SBDCD4213F has been designed to be configured in multiple ways:

NO DIMMING

- OPERATION: The SBDCD4213F can be configured to operate without dimming by floating the Control (J1-6) pin.
- Pin 1,2 of connector J1 must be connected to +Vin, between 4.5 and 5.5 Vdc. Pins 3 and 4 of connector J1 must be connected to GND.

ONBOARD PWM DIMMING

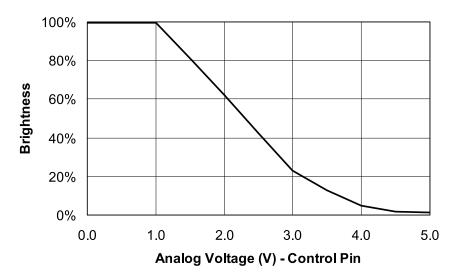
- OPERATION: Onboard PWM configuration as shown in Figure 1 allows the user to control display brightness by controlling the onboard PWM generator. The user is responsible to provide an analog control signal. A dimming ratio up to 255:1 is possible with this configuration.
- DIMMING: Dimming is accomplished by applying an analog voltage to the Control Pin (J1-6). Display brightness is modulated by controlling the Control Pin voltage as shown in Graph 1.
- Pin 1,2 of connector J1 must be connected to +Vin, between 4.5 and 5.5 Vdc. Pins 3 and 4 of connector J1 must be connected to GND.



SBDCD4213F



ONBOARD PWM DIMMING



Graph 1

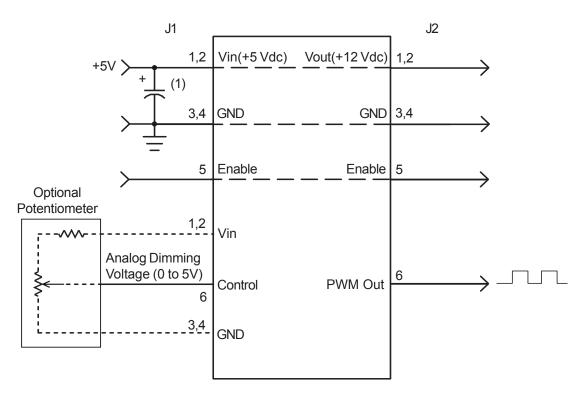


Figure 1

(1) Low ESR type input by-pass capacitor (10 uF - 220 uF) may be required to reduce reflected ripple and to improve power supply response.



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