Product Specifications		
PART NO.:	VL41B2863F-K9S/F8S/E7S-S1	REV: 1.2

General Information

1GB 128Mx72 DDR3 SDRAM ULP ECC UNBUFFERED SO-UDIMM 204-PIN

Description

The VL41B2863F is a 128Mx72 DDR3 SDRAM high density SO-UDIMM. This memory module is single rank, consists of nine CMOS 128Mx8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages and a 2K EEPROM in an 8-pin MLF package. This module is a 204-pin small-outline dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features

- 204-pin, unbuffered small-outline dual in-line memory module (SO-UDIMM)
- Supports ECC error detection and correction
- Fast data transfer rates: PC3-10600, PC3-8500, PC3-6400
- VDD = VDDQ = 1.5V +/-0.075V
- JEDEC standard 1.5V +/-0.075V I/O (SSTL_15 compatible)
- VDDSPD = 3.0V to 3.6V
- Eight internal component banks for concurrent operation
- 8-bit pre-fetch architecture
- Bi-directional differential data-strobe
- Nominal and dynamic on-die termination (ODT)
- ZQ calibration support
- Programmable CAS# latency:
  9 (DDR3-1333), 7 (DDR3-1066), 6 (DDR3-800)
- Programmable burst; length (8)
- Average refresh period 7.8 us
- Asynchronous reset
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 17.78mm (0.700”), double sided component
- Operating temperature (TOPER): -40 to +95°C (module screening using commercial DRAM)

  Note: Double refresh rate is required when 85°C < TOPER <= 95°C.

Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
DM0~DM8	Data Masks
CB0~CB7	Data Check Bits I/O
CK0,CK0#	Clock Input
ODT0	On-die Termination Control
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
RESET#	Register and SDRAM Control
NC	No Connect

Order Information:

VL41B2863F-K9 S X-S1

- S1: Screening temperature
- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  K9: PC3-10600 @ CL9
  F8: PC3-8500 @ CL7
  E7: PC3-6400 @ CL6
- VL: Lead-free/RoHS

Pin Configuration

204-PIN DDR3 SO-UDIMM FRONT

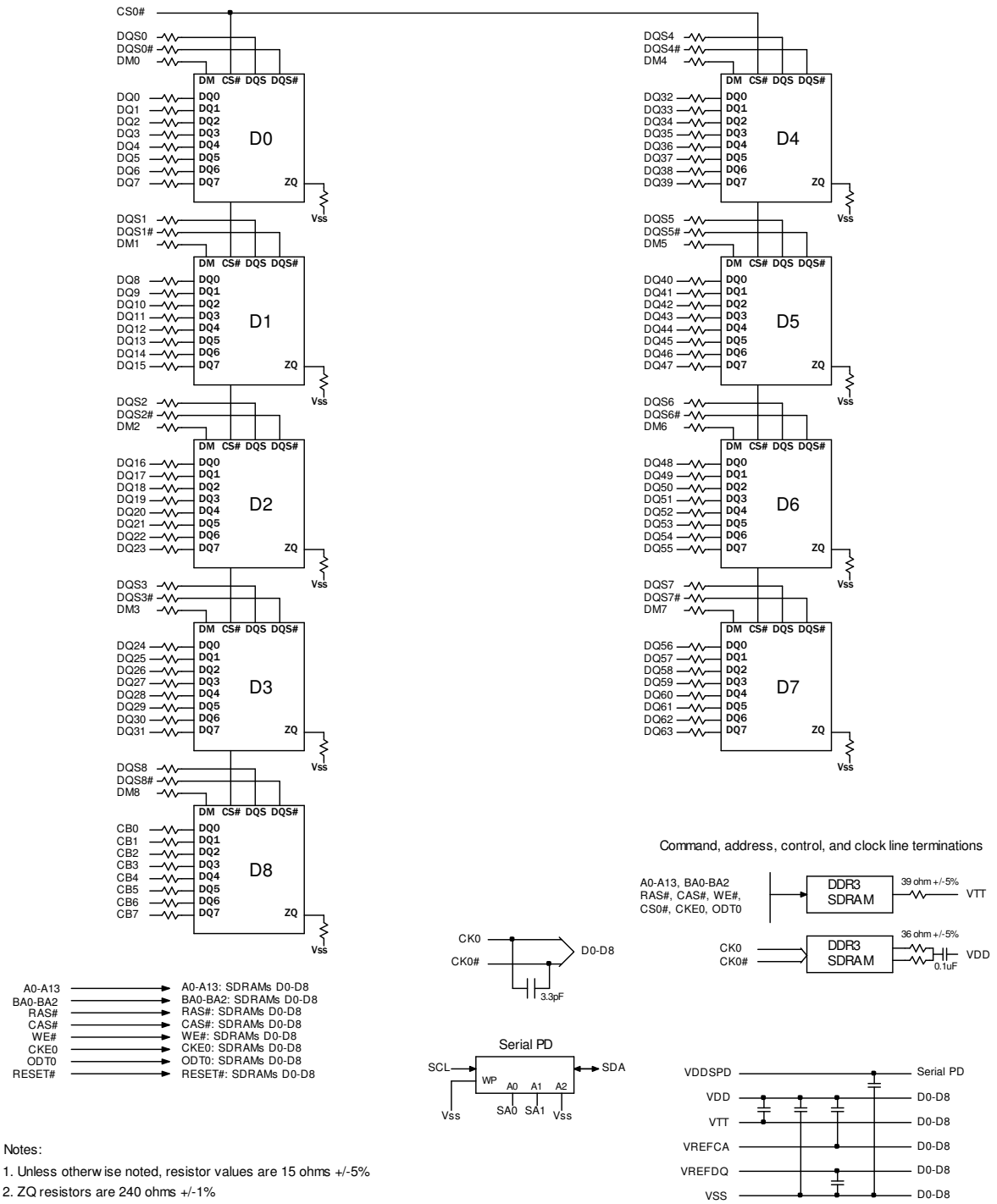
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	53	VSS	105	A1	157	DM5
3	VSS	55	DQ24	107	A0	159	DQ42
5	DQ0	57	DQ25	109	VDD	161	DQ43
7	DQ1	59	DM3	111	CK0	163	VSS
9	VSS	61	VSS	113	CK0#	165	DQ48
11	DM0	63	DQ26	115	VDD	167	DQ49
13	DQ2	65	DQ27	117	A10/AP	169	VSS
15	DQ3	67	VSS	119	BA0	171	DQS6#
17	VSS	69	CB0	121	WE#	173	DQS6
19	DQ8	71	CB1	123	VDD	175	VSS
21	DQ9	73	VSS	125	CAS#	177	DQ50
23	VSS	75	DQS8#	127	CS0#	179	DQ51
25	DQS1#	77	DQS8	129	CS1# *	181	VSS
27	DQS1	79	VSS	131	VDD	183	DQ56
29	VSS	81	CB2	133	DQ32	185	DQ57
31	DQ10	83	CB3	135	DQ33	187	VSS
33	DQ11	85	VDD	137	VSS	189	DM7
35	VSS	87	CKE0	139	DQS4#	191	DQ58
37	DQ16	89	CKE1 *	141	DQS4	193	DQ59
39	DQ17	91	BA2	143	VSS	195	VSS
41	VSS	93	VDD	145	DQ34	197	SA0
43	DQS2#	95	A12/BC#	147	DQ35	199	VDDSPD
45	DQS2	97	A8	149	VSS	201	SA1
47	VSS	99	A5	151	DQ40	203	VTT
49	DQ18	101	VDD	153	DQ41		
51	DQ19	103	A3	155	VSS		

204-PIN DDR3 SO-UDIMM BACK

Pin	Name	Pin	Name	Pin	Name	Pin	Name
2	VSS	54	DQ28	106	A2	158	VSS
4	DQ4	56	DQ29	108	BA1	160	DQ46
6	DQ5	58	VSS	110	VDD	162	DQ47
8	VSS	60	DQS3#	112	CK1 *	164	VSS
10	DQS0#	62	DQS3	114	CK1# *	166	DQ52
12	DQS0	64	VSS	116	VDD	168	DQ53
14	VSS	66	DQ30	118	CS3# *	170	VSS
16	DQ6	68	DQ31	120	CS2# *	172	DM6
18	DQ7	70	VSS	122	RAS#	174	DQ54
20	VSS	72	CB4	124	VDD	176	DQ55
22	DQ12	74	CB5	126	ODT0	178	VSS
24	DQ13	76	DM8	128	ODT1 *	180	DQ60
26	VSS	78	VSS	130	A13	182	DQ61
28	DM1	80	CB6	132	VDD	184	VSS
30	RESET#	82	CB7	134	DQ36	186	DQS7#
32	VSS	84	VREFCA	136	DQ37	188	DQS7
34	DQ14	86	VDD	138	VSS	190	VSS
36	DQ15	88	A15 *	140	DM4	192	DQ62
38	VSS	90	A14 *	142	DQ38	194	DQ63
40	DQ20	92	A9	144	DQ39	196	VSS
42	DQ21	94	VDD	146	VSS	198	EVENT# *
44	DM2	96	A11	148	DQ44	200	SDA
46	VSS	98	A7	150	DQ45	202	SCL
48	DQ22	100	A6	152	VSS	204	VTT
50	DQ23	102	VDD	154	DQS5#		
52	VSS	104	A4	156	DQS5		

*: These pins are not used in this module.

Function Block Diagram



Notes:

1. Unless otherwise noted, resistor values are 15 ohms +/-5%
2. ZQ resistors are 240 ohms +/-1%

Absolute Maximum Ratings

Symbol	Parameter		MIN	MAX	Unit
VDD	Voltage on VDD pin relative to VSS		-0.4	1.975	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.4	1.975	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.4	1.975	V
TSTG	Storage temperature		-55	100	^{0}C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, BA	-18	18	uA
		CS#, CKE, ODT, CK, CK#	-18	18	uA
		DM	-2	2	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-9	9	uA

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply Voltage	1.425	1.5	1.575	V	1,2
VDDQ	I/O Supply Voltage	1.425	1.5	1.575	V	1,2
VREFDQ (DC)	I/O reference voltage DQ bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VREFCA (DC)	Input reference voltage CMD/ADD bus	0.49 x VDD	0.5 x VDD	0.51 x VDD	V	3,4
VTT	Termination Reference Voltage	-0.483 x VDDQ	0.5 x VDDQ	+0.517 x VDDQ	V	5

Note:
1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VDD
4. For reference: approximate VDD/2 +/-15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	-40 to +95	^{o}C	1,2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
Command and Address				
VIHCA(DC)	Input High (Logic 1) Voltage DDR3-800/1066/1333	VREF + 0.100	VDD	V
VILCA(DC)	Input Low (Logic 0) Voltage DDR3-800/1066/1333	VSS	VREF - 0.100	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1) Voltage DDR3-800/1066/1333	VREF + 0.100	VDD	V
VILDQ(DC)	Input Low (Logic 0) Voltage DDR3-800/1066/1333	VSS	VREF - 0.100	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
Command and Address				
VIHCA(AC)	Input High (Logic 1) Voltage DDR3-800/1066/1333	VREF + 0.175	-	V
VILCA(AC)	Input Low (Logic 0) Voltage DDR3-800/1066/1333	-	VREF - 0.175	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1) Voltage DDR3-800/1066	VREF + 0.175	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage DDR3-800/1066	-	VREF - 0.175	V
VIHDQ(AC)	Input High (Logic 1) Voltage DDR3-1333	VREF + 0.150	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage DDR3-1333	-	VREF - 0.150	V

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	10.75	15.7	10.75	17.5	10.75	17.5	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	10.75	15.7	10.75	17.5	10.75	17.5	pF
Input capacitance (CK0, CK0#)	CIN3	11.2	16.6	11.2	18.4	11.2	18.4	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	5.5	6.5	5.5	6.7	5.5	7	pF

IDD Specification

Condition	Symbol	K9 (DDR3-1333)	F8 (DDR3-1066)	E7 (DDR3-800)	Unit
Operating one bank active-precharge current; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	315	315	315	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); tRCD= tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	378	360	360	mA
Precharge power-down current; All device banks idle; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F**	108	108	108	mA
	IDD2P-S**	90	90	90	mA
Precharge standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N**	135	135	135	mA
Precharge quiet standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	135	135	135	mA
Active power-down current; All device banks open; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	135	135	135	mA
Active standby current; All device banks open; tCK= tCK(IDD); tRP= tRP(IDD); tRAS= tRAS MAX(IDD)); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	180	180	180	mA
Operating burst read current; All device banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	630	540	540	mA
Operating burst write current; All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	630	540	540	mA
Burst refresh current; tCK=tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	810	765	765	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	90	90	90	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = tRCD(IDD) - 1*tCK(IDD); tCK= tCK(IDD); tRC= tRC(IDD); tRRD = tRRD(IDD); tRCD = 1*tCK(IDD) ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	1170	945	945	mA

Notes:
IDD specification is based on Samsung G-die components.
*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	1.5	<1.875	1.875	<2.5	2.5	3.3	ns
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ns
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-80	80	-90	90	-100	100	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	-80	80	-90	90	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160		180		200		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140		160		180		ps
Cumulative error across 2 cycles	tERR(2per)	-118	118	-132	132	-147	147	ps
Cumulative error across 3 cycles	tERR(3per)	-140	140	-157	157	-175	175	ps
Cumulative error across 4 cycles	tERR(4per)	-155	155	-175	175	-194	194	ps
Cumulative error across 5 cycles	tERR(5per)	-168	168	-188	188	-209	209	ps
Cumulative error across 6 cycles	tERR(6per)	-177	177	-200	200	-222	222	ps
Cumulative error across 7 cycles	tERR(7per)	-186	186	-209	209	-232	232	ps
Cumulative error across 8 cycles	tERR(8per)	-193	193	-217	217	-241	241	ps
Cumulative error across 9 cycles	tERR(9per)	-200	200	-224	224	-249	249	ps
Cumulative error across 10 cycles	tERR(10per)	-205	205	-231	231	-257	257	ps
Cumulative error across 11 cycles	tERR(11per)	-210	210	-237	237	-263	263	ps
Cumulative error across 12 cycles	tERR(12per)	-215	215	-242	242	-269	269	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(*n*per)	tERR(*n*per)min =(1+ 0.68ln(*n*))*tJIT(per)min tERR(*n*per)max =(1+ 0.68ln(*n*))*tJIT(per)max						ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	tCK(avg)
Data Timing								
DQS,DQS# to DQ skew, per group, per access	tDQSQ	-	125	-	150	-	200	ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-500	250	-600	300	-800	400	ps
DQ high-impedance time from CK, CK#	tHZ(DQ)	-	250	-	300	-	400	ps
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	tDS(base)	30	-	25	-	75	-	ps
Data hold time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	tDH(base)	65	-	100	-	150	-	ps
DQ and DM Input pulse width for each input	tDIPW	400	-	490	-	600	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Data Strobe Timing								
DQS, DQS# READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# output high time	tQSH	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS# output low time	tQSL	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS# WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-255	255	-300	300	-400	400	ps
DQS, DQS# low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	-600	300	-800	400	ps
DQS, DQS# high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	250	-	300	-	400	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS,DQS# failing edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)
DQS,DQS# failing edge hold time to CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)
Command and Address Timing								
DLL locking time	tDLLK	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns	-	max (12tCK,15ns	-	max (12tCK,15ns	-	
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))						nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	9*tREFI	37.5	9*tREFI	37.5	9*tREFI	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	max (4tCK,10ns)	-	
Four activate window for 1KB page size	tFAW	30	-	37.5	-	40	-	ns
Four activate window for 2KB page size	tFAW	45	-	50	-	50	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	125	-	200	-	ps
Command and Address hold time from CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	200	-	275	-	ps
Control & Address Input pulse width for each input	tIPW	620	-	780	-	900	-	ps

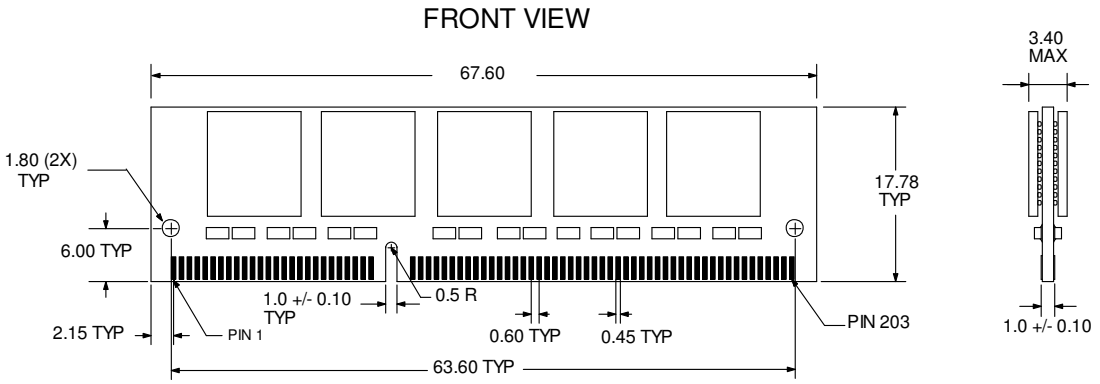
AC TIMING PARAMETERS & SPECIFICATIONS

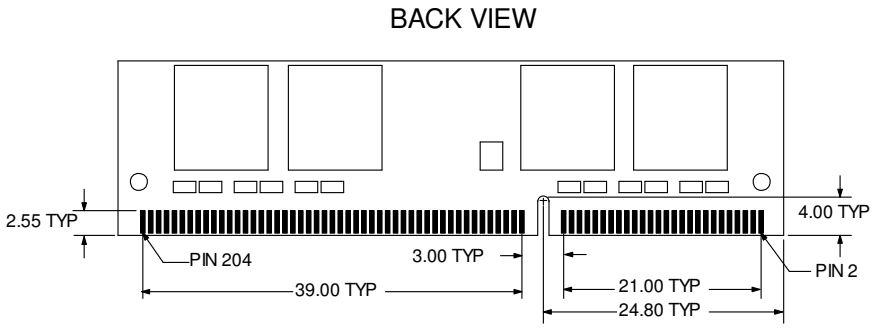
Parameter	Symbol	K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Refresh Timing								
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	110	-	110	-	110	-	ns
Average periodic refresh interval (0℃<= TCASE <= 85 ℃)	tREFI	7.8		7.8		7.8		us
Average periodic refresh interval (85℃<= TCASE <= 95 ℃)	tREFI	3.9		3.9		3.9		us
Calibration Timing								
Power-up and RESET calibration time	tZQinitI	512	-	512	-	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	tCK
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	tCK
Reset Timing								
Exit Reset from CKE HIGH to a valid command	tXPR	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	
Self Refresh Timing								
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK, tRFC +10ns)	-	max(5tCK, tRFC +10ns)	-	max(5tCK, tRFC +10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	
Power Down Timing								
Exit Power Down with DLL to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	max (3tCK,7.5ns)	-	max (3tCK,7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10tCK,24ns)	-	max (10tCK,24ns)	-	max (10tCK,24ns)	-	
CKE minimum pulse width	tCKE	max (3tCK, 5.625ns)	-	max (3tCK, 5.625ns)	-	max (3tCK, 7.5ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	
Timing of WR command to Power Down entry BL8 (OTF, MRS), BL4OTF	tWRPDEN	WL + 4 +(tWR/ tCK)	-	WL + 4 +(tWR/ tCK)	-	WL + 4 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry BL8 (OTF, MRS), BL4OTF	tWRAPDEN	WL+4+WR+ 1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK)	-	WL + 2 +(tWR/ tCK)	-	WL + 2 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL+2+WR+ 1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
ODT Timing								
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	ns
ODT turn-on	tAON	-250	250	-300	300	-400	400	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing								
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	245	-	325	-	ps
Hold time for tDQSS latch	tWLH	195	-	245	-	325	-	ps
Write leveling output delay	tWLO	0	9	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns

Package Dimensions





Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
02/25/2010	1.0	All	Spec released
03/19/2010	1.1	6	Update IDD specification table for using Samsung DRAM F-die
05/17/2011	1.2	1,5,6	Update General Information, modify temp range: -40 to +95°C on p. 1 Add note: Double refresh rate is required when 85°C<TOPER<=95°C on p.1, 5 Update IDD specification table for module using Samsung DRAM G-die on p. 6