



Product Specifications

PART NO.:

VL31D5263A-K0/K9/F8/E7S

REV: 1.4

General Information

4GB 512Mx72 DDR3 SDRAM LOW VOLTAGE ECC UNBUFFERED DIMM 240-PIN

Description

The VL31D5263A is a 512Mx72 DDR3 SDRAM high density UDIMM. This dual rank memory module consists of eighteen CMOS 256Mx8 bits with 8 banks DDR3 synchronous DRAMs in BGA packages, and a 2K EEPROM in an 8-pin MLF package. This module is a 240-pin dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features

- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Supports ECC error detection and correction
- Fast data transfer rates: PC3-12800, PC3-10600, PC3-8500, PC3-6400
- VDD = VDDQ = 1.35V (1.28V~1.45V) & 1.5V (1.425V~1.575V)
- JEDEC standard 1.35V (1.28V~1.45V) & 1.5V (1.425V~1.575V)
- VDDSPD = 3.0V to 3.6V
- Eight internal component banks for concurrent operation
- 8-bit pre-fetch architecture
- Bi-directional differential data-strobe
- Nominal and dynamic on-die termination (ODT)
- ZQ calibration support
- Programmable CAS# latency:
11 (DDR3-1600), 9 (DDR3-1333), 7 (DDR3-1066), 6 (DDR3-800)
- Programmable burst; length (8)
- Average refresh period 7.8 us
- Asynchronous reset
- Fly-by topology
- On board terminated command, address, and control bus
- Serial presence detect (SPD) EEPROM with thermal sensor
- Thermal sensor range: -40°C to +125°C (Max +/-3°C accuracy)
- JEDEC pinout
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 30.00mm (1.181"), double sided component
- Operating temperature (T_{OPER}): - Commercial (0°C ≤ T_c ≤ 95°C)
- Industrial (-40°C ≤ T_c ≤ 95°C)

Notes: Double refresh rate is required when 85°C < T_{OPER} ≤ 95°C.
T_{OPER} is DRAM case temperature (T_c).

Pin Description

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Input/ Autoprecharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
DM0~DM8	Data Masks
CB0~CB7	Data Check Bits I/O
CK0, CK0#, CK1, CK1#	Clock Input
ODT0, ODT1	On-die Termination Control
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
RESET#	Register and SDRAM Control
VDD	Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
EVENT#	Temperature Event Output
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply
VTT	Termination Voltage
NC	No Connect

Order Information:

VL31D5263A-K0 S X-X

OPERATING TEMPERATURE

None: Commercial
S1: Industrial screening

DRAM DIE (Option)

DRAM MANUFACTURER
S - SAMSUNG

MODULE SPEED

K0: PC3-12800 @ CL11
K9: PC3-10600 @ CL9
F8: PC3-8500 @ CL7
E7: PC3-6400 @ CL6

VL: Lead-free/RoHS



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Pin Configuration

240-PIN DDR3 UDIMM FRONT SIDE

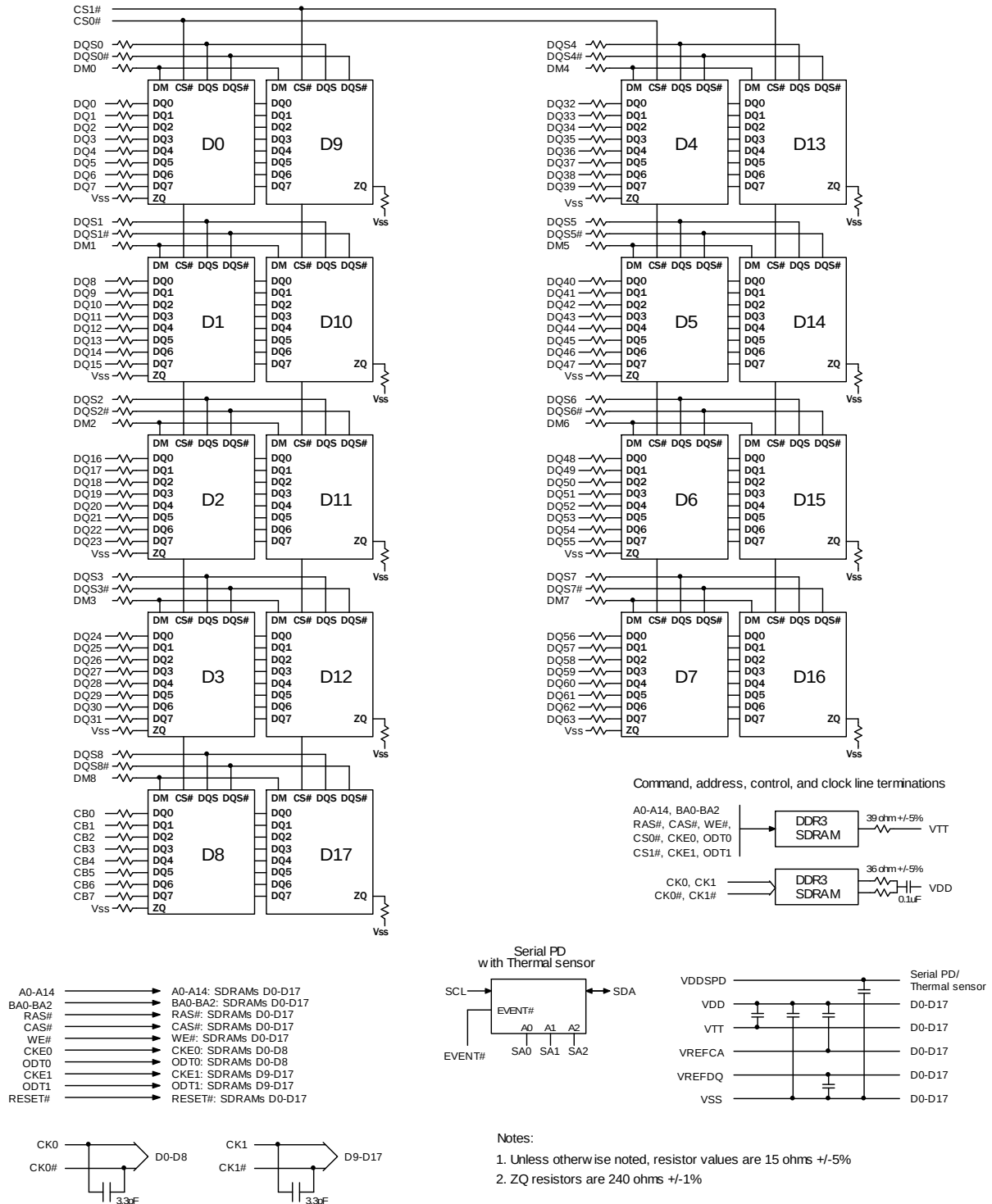
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	31	DQ25	61	A2	91	DQ41
2	VSS	32	VSS	62	VDD	92	VSS
3	DQ0	33	DQS3#	63	CK1	93	DQS5#
4	DQ1	34	DQS3	64	CK1#	94	DQS5
5	VSS	35	VSS	65	VDD	95	VSS
6	DQS0#	36	DQ26	66	VDD	96	DQ42
7	DQS0	37	DQ27	67	VREFCA	97	DQ43
8	VSS	38	VSS	68	PAR_IN *	98	VSS
9	DQ2	39	CB0	69	VDD	99	DQ48
10	DQ3	40	CB1	70	A10/AP	100	DQ49
11	VSS	41	VSS	71	BA0	101	VSS
12	DQ8	42	DQS8#	72	VDD	102	DQS6#
13	DQ9	43	DQS8	73	WE#	103	DQS6
14	VSS	44	VSS	74	CAS#	104	VSS
15	DQS1#	45	CB2	75	VDD	105	DQ50
16	DQS1	46	CB3	76	CS1#	106	DQ51
17	VSS	47	VSS	77	ODT1	107	VSS
18	DQ10	48	VTT	78	VDD	108	DQ56
19	DQ11	49	VTT	79	NC	109	DQ57
20	VSS	50	CKE0	80	VSS	110	VSS
21	DQ16	51	VDD	81	DQ32	111	DQS7#
22	DQ17	52	BA2	82	DQ33	112	DQS7
23	VSS	53	Err_Out# *	83	VSS	113	VSS
24	DQS2#	54	VDD	84	DQS4#	114	DQ58
25	DQS2	55	A11	85	DQS4	115	DQ59
26	VSS	56	A7	86	VSS	116	VSS
27	DQ18	57	VDD	87	DQ34	117	SA0
28	DQ19	58	A5	88	DQ35	118	SCL
29	VSS	59	A4	89	VSS	119	SA2
30	DQ24	60	VDD	90	DQ40	120	VTT

240-PIN DDR3 UDIMM BACK SIDE

Pin	Name	Pin	Name	Pin	Name	Pin	Name
121	VSS	151	VSS	181	A1	211	VSS
122	DQ4	152	DM3	182	VDD	212	DM5
123	DQ5	153	NC	183	VDD	213	NC
124	VSS	154	VSS	184	CK0	214	VSS
125	DM0	155	DQ30	185	CK0#	215	DQ46
126	NC	156	DQ31	186	VDD	216	DQ47
127	VSS	157	VSS	187	EVENT#	217	VSS
128	DQ6	158	CB4	188	A0	218	DQ52
129	DQ7	159	CB5	189	VDD	219	DQ53
130	VSS	160	VSS	190	BA1	220	VSS
131	DQ12	161	DM8	191	VDD	221	DM6
132	DQ13	162	NC	192	RAS#	222	NC
133	VSS	163	VSS	193	CS0#	223	VSS
134	DM1	164	CB6	194	VDD	224	DQ54
135	NC	165	CB7	195	ODT0	225	DQ55
136	VSS	166	VSS	196	A13	226	VSS
137	DQ14	167	TEST *	197	VDD	227	DQ60
138	DQ15	168	RESET#	198	NC	228	DQ61
139	VSS	169	CKE1	199	VSS	229	VSS
140	DQ20	170	VDD	200	DQ36	230	DM7
141	DQ21	171	A15 *	201	DQ37	231	NC
142	VSS	172	A14	202	VSS	232	VSS
143	DM2	173	VDD	203	DM4	233	DQ62
144	NC	174	A12/ BC#	204	NC	234	DQ63
145	VSS	175	A9	205	VSS	235	VSS
146	DQ22	176	VDD	206	DQ38	236	VDDSPD
147	DQ23	177	A8	207	DQ39	237	SA1
148	VSS	178	A6	208	VSS	238	SDA
149	DQ28	179	VDD	209	DQ44	239	VSS
150	DQ29	180	A3	210	DQ45	240	VTT

*: These pins are not used in this module.

Function Block Diagram





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Absolute Maximum Ratings

Symbol	Parameter		Min	Max	Unit
VDD	Voltage on VDD pin relative to VSS		-0.4	1.975	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.4	1.975	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.4	1.975	V
TSTG	Storage temperature		-55	100	°C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, BA	-36	36	uA
		CS#, CKE, ODT, CK, CK#	-18	18	uA
		DM	-4	4	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-18	18	uA

DC Operating Conditions

Symbol	Parameter	Operating Voltage	Min	Typical	Max	Unit	Notes
VDD	Supply Voltage	1.35V	1.283	1.35	1.45	V	1,2
		1.5V	1.425	1.5	1.575		
VDDQ	I/O Supply Voltage	1.35V	1.283	1.35	1.45	V	1,2
		1.5V	1.425	1.5	1.575		
VREFDQ (DC)	I/O reference voltage DQ bus		$0.49 \times VDD$	$0.5 \times VDD$	$0.51 \times VDD$	V	3,4
VREFCA (DC)	Input reference voltage CMD/ADD bus		$0.49 \times VDD$	$0.5 \times VDD$	$0.51 \times VDD$	V	3,4
VTT	Termination Reference Voltage		$-0.483 \times VDDQ$	$0.5 \times VDDQ$	$+0.517 \times VDDQ$	V	5

Note:

- Under all conditions VDDQ must be less than or equal to VDD.
- VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
- The AC peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/-1% VDD
- For reference: approximate $VDD/2 \pm 15mV$.
- VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to 95	°C	1,2
		Industrial	-40 to +95		

Notes:

- Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
- At -40 to +85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when $85^{\circ}C < TOPER \leq 95^{\circ}C$.



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Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
1.35V				
Command and Address				
VIHCA(DC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.090	VDD	V
VILCA(DC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	VSS	VREF - 0.090	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.090	VDD	V
VILDQ(DC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	VSS	VREF - 0.090	V
1.5V				
Command and Address				
VIHCA(DC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.100	VDD	V
VILCA(DC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	VSS	VREF - 0.100	V
DQ and DM				
VIHDQ(DC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.100	VDD	V
VILDQ(DC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	VSS	VREF - 0.100	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
1.35V				
Command and Address				
VIHCA(AC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.160	-	V
VILCA(AC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	-	VREF - 0.160	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1) Voltage (DDR3-800/1066)	VREF + 0.160	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage (DDR3-800/1066)	-	VREF - 0.160	V
VIHDQ(AC)	Input High (Logic 1) Voltage (DDR3-1333/1600)	VREF + 0.135	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage (DDR3-1333/1600)	-	VREF - 0.135	V
1.5V				
Command and Address				
VIHCA(AC)	Input High (Logic 1) Voltage (DDR3-800/1066/1333/1600)	VREF + 0.175	-	V
VILCA(AC)	Input Low (Logic 0) Voltage (DDR3-800/1066/1333/1600)	-	VREF - 0.175	V
DQ and DM				
VIHDQ(AC)	Input High (Logic 1) Voltage (DDR3-800/1066)	VREF + 0.175	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage (DDR3-800/1066)	-	VREF - 0.175	V
VIHDQ(AC)	Input High (Logic 1) Voltage (DDR3-1333/1600)	VREF + 0.150	-	V
VILDQ(AC)	Input Low (Logic 0) Voltage (DDR3-1333/1600)	-	VREF - 0.150	V



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Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		Min	Max	Min	Max	Min	Max	Min	Max	
1.35V										
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	17.5	27.4	17.5	27.4	17.5	27.4	17.5	27.4	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	10.75	15.7	10.75	15.7	10.75	15.7	10.75	15.7	pF
Input capacitance (CK0, CK0#), (CK1, CK1#)	CIN3	11.2	16.6	11.2	16.6	11.2	18.4	11.2	18.4	pF
Input/Output capacitance (DQ, DQS, DQS#, CB, DM)	CIO	6.4	8.6	7	8.6	7	9	7	9	pF
1.5V										
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	17.5	27.4	17.5	27.4	17.5	31	17.5	31	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	10.75	15.7	10.75	15.7	10.75	17.5	10.75	17.5	pF
Input capacitance (CK0, CK0#), (CK1, CK1#)	CIN3	11.2	16.6	11.2	16.6	11.2	18.4	11.2	18.4	pF
Input/Output capacitance (DQ, DQS, DQS#, CB, DM)	CIO	6.8	8.6	7	9	7	9.4	7	10	pF



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Basic IDD and IDDQ Measurement Conditions

Symbol	Condition
IDD0*	Operating one bank active-precharge current; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD1*	Operating one bank active-read-precharge current; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRC= tRC(IDD); tRAS= tRAS MIN(IDD); tRCD= tRCD(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.
IDD2P-F**	Precharge power-down current Fast Exit; All device banks idle; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
IDD2P-S**	Precharge power-down current Low Exit; All device banks idle; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
IDD2N**	Precharge standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD2Q**	Precharge quiet standby current; All device banks idle; tCK= tCK(IDD); CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
IDD3P**	Active power-down current; All device banks open; tCK= tCK(IDD); CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.
IDD3N**	Active standby current; All device banks open; tCK= tCK(IDD); tRP= tRP(IDD); tRAS= tRAS MAX(IDD); CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD4R*	Operating burst read current; All device banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.
IDD4W*	Operating burst write current; All device banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; tCK= tCK(IDD); tRAS= tRAS MAX(IDD); tRP= tRP(IDD); CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD5**	Burst refresh current; tCK=tCK(IDD); Refresh command at every tRFC(IDD) interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.
IDD6**	Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.
IDD7*	Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = tRCD(IDD) - 1*tCK(IDD); tCK= tCK(IDD); tRC= tRC(IDD); tRRD = tRRD(IDD); tRCD = 1*tCK(IDD); CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.
Notes:	
*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.	
**: Value calculated reflects all module ranks in this operating condition.	



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IDD Specification

Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
	1.35V	1.5V	1.35V	1.5V	1.35V	1.5V	1.35V	1.5V	
IDD0	450	513	405	468	360	423	360	423	mA
IDD1	540	603	495	558	450	513	450	513	mA
IDD2P-F	270	270	234	270	234	270	234	270	mA
IDD2P-S	180	216	180	216	180	216	180	216	mA
IDD2N	306	360	270	360	270	306	270	306	mA
IDD2Q	306	360	270	360	270	306	270	306	mA
IDD3P	306	360	270	306	270	306	270	306	mA
IDD3N	540	630	450	630	450	540	450	540	mA
IDD4R	675	918	630	783	540	693	540	693	mA
IDD4W	765	963	675	828	585	738	585	738	mA
IDD5	2070	2160	2070	2070	1980	1980	1980	1980	mA
IDD6	180	216	180	216	180	216	180	216	mA
IDD7	1215	1368	1170	1323	945	1053	945	1053	mA

Note: IDD specification is based on Samsung D-die components.



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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
Clock Timing											
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	8	-	ns	
Average Clock Period	tCK(avg)	1.25	<1.50	1.5	<1.875	1.875	<2.5	2.5	3.3	ns	
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ns	
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)	
Clock Period Jitter	tJIT(per)	-70	70	-80	80	-90	90	-100	100	ps	
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-70	70	-80	80	-90	90	ps	
Cycle to Cycle Period Jitter	tJIT(cc)	140		160		180		200		ps	
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		140		160		180		ps	
Cumulative error across 2 cycles	tERR(2per)	-103	103	-118	118	-132	132	-147	147	ps	
Cumulative error across 3 cycles	tERR(3per)	-122	122	-140	140	-157	157	-175	175	ps	
Cumulative error across 4 cycles	tERR(4per)	-136	136	-155	155	-175	175	-194	194	ps	
Cumulative error across 5 cycles	tERR(5per)	-147	147	-168	168	-188	188	-209	209	ps	
Cumulative error across 6 cycles	tERR(6per)	-155	155	-177	177	-200	200	-222	222	ps	
Cumulative error across 7 cycles	tERR(7per)	-163	163	-186	186	-209	209	-232	232	ps	
Cumulative error across 8 cycles	tERR(8per)	-169	169	-193	193	-217	217	-241	241	ps	
Cumulative error across 9 cycles	tERR(9per)	-175	175	-200	200	-224	224	-249	249	ps	
Cumulative error across 10 cycles	tERR(10per)	-180	180	-205	205	-231	231	-257	257	ps	
Cumulative error across 11 cycles	tERR(11per)	-184	184	-210	210	-237	237	-263	263	ps	
Cumulative error across 12 cycles	tERR(12per)	-188	188	-215	215	-242	242	-269	269	ps	
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min =(1+ 0.68ln(n))*tJIT(per)min tERR(nper)max=(1+ 0.68ln(n))*tJIT(per)max								ps	
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	
Absolute clock Low pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)	
Data Timing											
DQS,DQS# to DQ skew, per group, per access		tDQSQ	-	100	-	125	-	150	-	200	ps
DQ output hold time from DQS, DQS#		tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#		tLZ(DQ)	-450	225	-500	250	-600	300	-800	400	ps
DQ high-impedance time from CK, CK#		tHZ(DQ)	-	225	-	250	-	300	-	400	ps
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	1.35V	tDS(base) (AC160)	-	-	-	-	40	-	90	-	ps
		tDS(base) (AC135)	25	-	45	-	-	-	-	-	ps
Data setup time to DQS, DQS# referenced to Vih(ac)Vil(ac) levels	1.5V	tDS(base) (AC175)	-	-	-	-	25	-	75	-	ps
		tDS(base) (AC150)	10	-	30	-	-	-	-	-	ps



Product Specifications

PART NO.:

VL31D5263A-K0/K9/F8/E7S

REV: 1.4

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Data hold time to DQS, DQS# referenced to Vih(ac)/Vil(ac) levels	tDH(base)	55	-	75	-	110	-	160	-	ps
DQ and DM Input pulse width for each input	tDIPW	360	-	400	-	490	-	600	-	ps
Data Strobe Timing										
DQS, DQS# READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# output high time	tQSH	0.4	-	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS# output low time	tQSL	0.4	-	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS# WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS# WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS# rising edge output access time from rising CK, CK#	tDQCK	-225	225	-255	255	-300	300	-400	400	ps
DQS, DQS# low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-500	250	-600	300	-800	400	ps
DQS, DQS# high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	225	-	250	-	300	-	400	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.27	0.27	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS,DQS# failing edge setup time to CK, CK# rising edge	tDSS	0.18	-	0.2	-	0.2	-	0.2	-	tCK(avg)
DQS,DQS# failing edge hold time to CK, CK# rising edge	tDSH	0.18	-	0.2	-	0.2	-	0.2	-	tCK(avg)
Command and Address Timing										
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	4	-	nCK
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	max (12tCK,15ns)	-	max (12tCK,15ns)	-	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))								nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	35	9*tREFI	36	9*tREFI	37.5	9*tREFI	37.5	9*tREFI	ns
ACTIVE to internal read or write delay time	tRCD	13.75	-	13.5	-	13.13	-	15	-	ns
PRECHARGE command period	tRP	13.75	-	13.5	-	13.13	-	15	-	ns
ACTIVE to ACTIVE or REF command period	tRC	48.75	-	49.5	-	50.63	-	52.5	-	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	max (4tCK,6ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	max (4tCK,10ns)	-	
Four activate window for 1KB page size	tFAW	30	-	30	-	37.5	-	40	-	ns
Four activate window for 2KB page size	tFAW	40	-	45	-	50	-	50	-	ns
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	1.35V	tIS(base) (AC160)	-	-	-	140	-	215	-	ps
		tIS(base) (AC135)	185	-	205	-	-	-	-	ps



Product Specifications

PART NO.:

VL31D5263A-K0/K9/F8/E7S

REV: 1.4

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	1.5V	tIS(base) (AC175)	45	-	65	-	125	-	200	ps
		tIS(base) (AC150)	45 + 125	-	65 + 125	-	125 + 150	-	200 + 150	ps
Command and Address hold time from CK, CK# referenced to Vih(ac) / Vil(ac) levels		tIH(base)	130	-	150	-	210	-	285	ps
Control & Address Input pulse width for each input		tIPW	560	-	620	-	780	-	900	ps
Refresh Timing										
2Gb REFRESH to REFRESH or REFRESH to ACTIVE command interval		tRFC	160	-	160	-	160	-	160	ns
Average periodic refresh interval (0°C ≤ TCASE ≤ 85 °C)		tREFI	7.8	-	7.8	-	7.8	-	7.8	us
Average periodic refresh interval (85°C ≤ TCASE ≤ 95 °C)		tREFI	3.9	-	3.9	-	3.9	-	3.9	us
Calibration Timing										
Power-up and RESET calibration time		tZQinitl	512	-	512	-	512	-	512	tCK
Normal operation Full calibration time		tZQoper	256	-	256	-	256	-	256	tCK
Normal operation Short calibration time		tZQCS	64	-	64	-	64	-	64	tCK
Reset Timing										
Exit Reset from CKE HIGH to a valid command		tXPR	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	-	max (5tCK, tRFC + 10ns)	
Self Refresh Timing										
Exit Self Refresh to commands not requiring a locked DLL		tXS	max(5tC, tRFC+10ns)	-	max(5tC, tRFC+10ns)	-	max(5tC, tRFC +10ns)	-	max(5tC, tRFC +10ns)	
Exit Self Refresh to commands requiring a locked DLL		tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	nCK
Minimum CKE low width for Self refresh entry to exit timing		tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	
Valid Clock Requirement after Self Refresh Entry (SRE)		tCKSRE	max(5tC, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	
Valid Clock Requirement before Self Refresh Exit (SRX)		tCKSRX	max(5tC, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	-	max(5tCK, 10ns)	
Power Down Timing										
Exit Power Down with DLL to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL		tXP	max (3tCK, 6ns)	-	max (3tCK, 6ns)	-	max (3tCK, 7.5ns)	-	max (3tCK, 7.5ns)	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL		tXPDLL	max (10tCK, 24ns)	-	max (10tCK, 24ns)	-	max (10tCK, 24ns)	-	max (10tCK, 24ns)	
CKE minimum pulse width		tCKE	max (3tCK, 5ns)	-	max (3tCK, 5.625ns)	-	max (3tCK, 5.625ns)	-	max (3tCK, 7.5ns)	
Command pass disable delay		tCPDED	1	-	1	-	1	-	1	nCK
Power Down Entry to Exit Timing		tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	tCK
Timing of ACT command to Power Down entry		tACTPDEN	1	-	1	-	1	-	1	nCK
Timing of PRE command to Power Down entry		tPRPDEN	1	-	1	-	1	-	1	nCK
Timing of RD/RDA command to Power Down entry		tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	
Timing of WR command to Power Down entry BL8 (OTF, MRS), BL4OTF		tWRPDEN	WL + 4 + (tWR/ tCK(avg))	-	WL + 4 + (tWR/ tCK(avg))	-	WL + 4 + (tWR/ tCK(avg))	-	WL + 4 + (tWR/ tCK(avg))	nCK
Timing of WRA command to Power Down entry BL8 (OTF, MRS), BL4OTF		tWRAPDEN	WL+4 +WR+1	-	WL+4 +WR+1	-	WL+4 +WR+1	-	WL+4 +WR+1	nCK



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AC TIMING PARAMETERS & SPECIFICATIONS

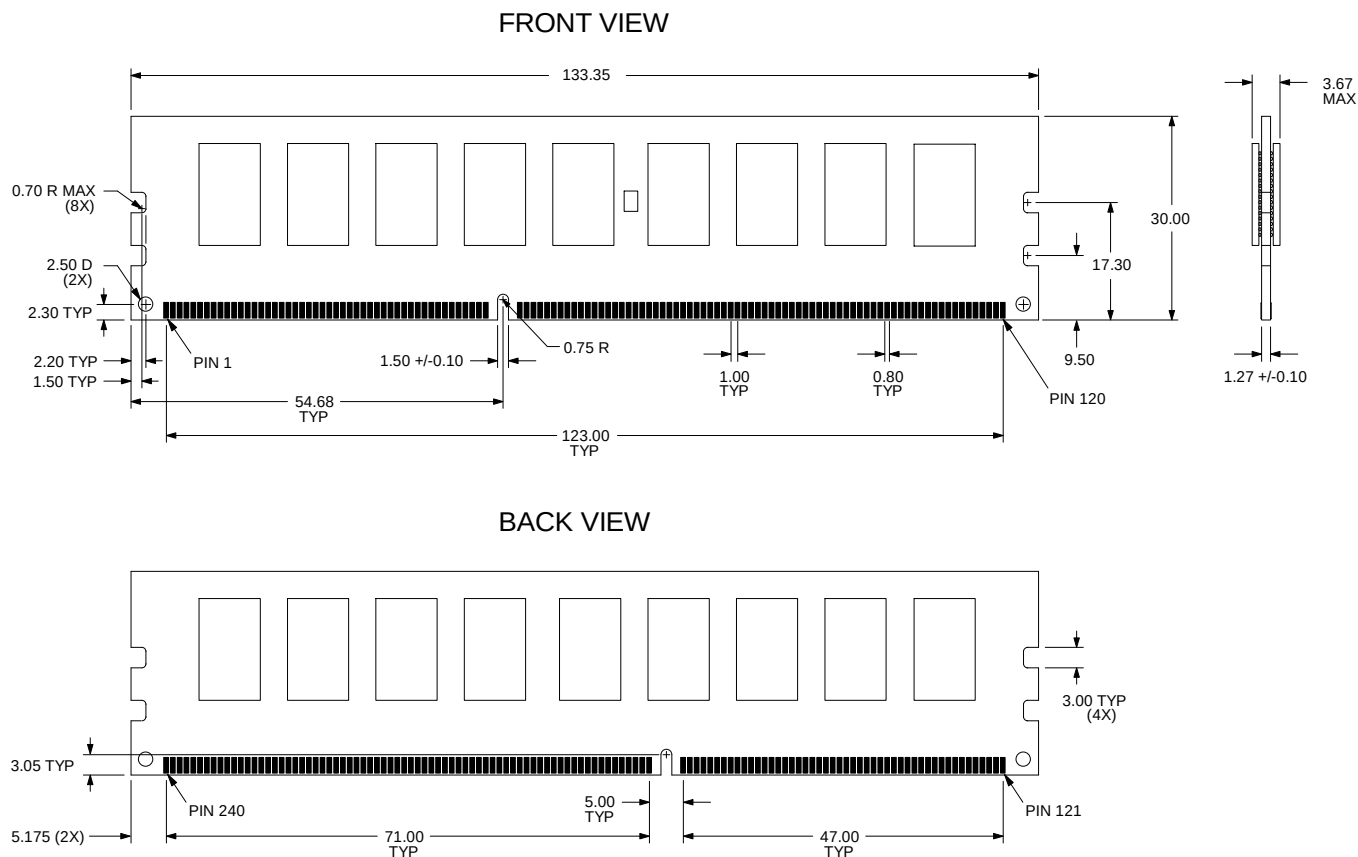
Parameter	Symbol	K0 (DDR3-1600)		K9 (DDR3-1333)		F8 (DDR3-1066)		E7 (DDR3-800)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 + (tWR/ tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	WL + 2 + (tWR/ tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL+2 +WR+1	-	WL+2 +WR+1	-	WL+2 +WR+1	-	WL+2 +WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	
ODT Timing										
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
ODT turn-on	tAON	-225	225	-250	250	-300	300	-400	400	ps
RTT_NOM and RTT_WR turn-off time from ODTL off reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing										
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	tCK
DQS/DQS delay after tDQSS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	165	-	195	-	245	-	325	-	ps
Hold time for tDQSS latch	tWLH	165	-	195	-	245	-	325	-	ps
Write leveling output delay	tWLO	0	7.5	0	9	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns

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REV: 1.4

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.



Product Specifications

PART NO.:

VL31D5263A-K0/K9/F8/E7S

REV: 1.4

Revision History:

Date	Rev.	Page	Changes
05/11/2011	1.0	All	Spec released
08/04/2011	1.1	7, 8	Update tIS(base), tIH(base), tDS(base), tDH(base) for module 1.35V.
04/17/2012	1.2	All	Update information for temperature sensor. Adding parameters for module 1.5V
05/04/2012	1.3	5	Update Input AC Logic Level table
05/07/2012	1.4	5	Typo correction