Product Specifications		
PART NO.:	**VL495T2863E-E6/D5/CCS**	**REV: 1.0**

General Information

1GB 128Mx72 DDR2 SDRAM VLP ECC REGISTERED Mini-DIMM 244-PIN

Description

The VL495T2863E is a 128Mx72 DDR2 SDRAM high density Mini-DIMM. This memory module is single rank, consists of nine CMOS 128Mx8 bits with 8 banks DDR2 synchronous DRAMs in BGA packages, a 25-bit registered buffers in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin TSSOP package. This module is a 244-pin mini dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

- 244-pin, mini dual in-line memory module (Mini-DIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rates: PC2-5300, PC2-4200, PC2-3200
- VDD = VDDQ = 1.8V +/-0.1V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency:
  5 (DDR2-667), 4 (DDR2-533), 3 (DDR2-400)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 18.29mm (0.720”), double sided component
- Operating temperature (TOPER): - Commercial ($0^{o}C <= Tc <= 95^{o}C$)
  - Industrial ($-40^{o}C <= Tc <= 95^{o}C$)

Notes: Double refresh rate is required when $85^{o}C < TOPER <= 95^{o}C$.
TOPER is DRAM case temperature (Tc)

Order Information:

VL495T2863E - E6 S X - X

- OPERATING TEMPERATURE
  None: Commercial
  S1: Industrial screening
- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  E6: PC2-5300 @ CL5
  D5: PC2-4200 @ CL4
  CC: PC2-3200 @ CL3
- VL: Lead-free/RoHS

Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
CB0~CB7	Check Bits
DM0~DM8	Data Masks
CK0, CK0#	Clock Input
ODT0	On-die Termination Control
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
RESET#	Reset Input
VDD	Voltage Supply
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply
VREF	SSTL_18 Reference Voltage
NC	No Connect

Virtium Technology, Inc.

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Pin Configuration

244-PIN DDR2 Mini-DIMM FRONT SIDE

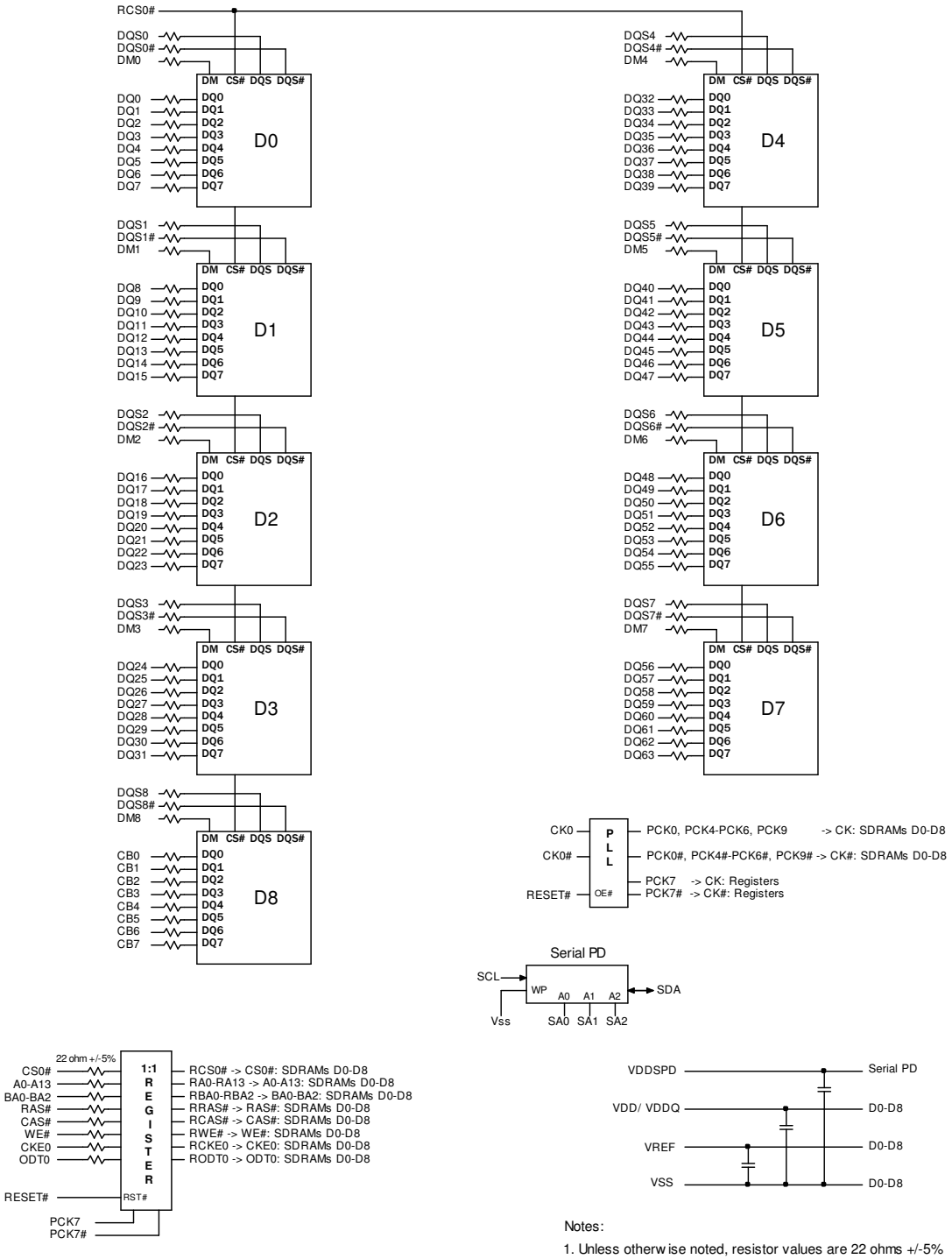
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	32	VSS	63	VDDQ	93	VSS
2	VSS	33	DQ24	64	A2	94	DQS5#
3	DQ0	34	DQ25	65	VDD	95	DQS5
4	DQ1	35	VSS	KEY		96	VSS
5	VSS	36	DQS3#	66	VSS	97	DQ42
6	DQS0#	37	DQS3	67	VSS	98	DQ43
7	DQS0	38	VSS	68	NC	99	VSS
8	VSS	39	DQ26	69	VDD	100	DQ48
9	DQ2	40	DQ27	70	A10/AP	101	DQ49
10	DQ3	41	VSS	71	BA0	102	VSS
11	VSS	42	CB0	72	VDD	103	SA2
12	DQ8	43	CB1	73	WE#	104	NC
13	DQ9	44	VSS	74	VDDQ	105	VSS
14	VSS	45	DQS8#	75	CAS#	106	DQS6#
15	DQS1#	46	DQS8	76	VDDQ	107	DQS6
16	DQS1	47	VSS	77	CS1#*	108	VSS
17	VSS	48	CB2	78	OTD1*	109	DQ50
18	RESET#	49	CB3	79	VDDQ	110	DQ51
19	NC	50	VSS	80	NC	111	VSS
20	VSS	51	NC	81	VSS	112	DQ56
21	DQ10	52	VDDQ	82	DQ32	113	DQ57
22	DQ11	53	CKE0	83	DQ33	114	VSS
23	VSS	54	VDD	84	VSS	115	DQS7#
24	DQ16	55	BA2	85	DQS4#	116	DQS7
25	DQ17	56	NC	86	DQS4	117	VSS
26	VSS	57	VDDQ	87	VSS	118	DQ58
27	DQS2#	58	A11	88	DQ34	119	DQ59
28	DQS2	59	A7	89	DQ35	120	VSS
29	VSS	60	VDD	90	VSS	121	SA0
30	DQ18	61	A5	91	DQ40	122	SA1
31	DQ19	62	A4	92	DQ41		

244-PIN DDR2 Mini-DIMM BACK SIDE

Pin	Name	Pin	Name	Pin	Name	Pin	Name
123	VSS	154	DQ28	185	A3	215	DM5
124	DQ4	155	DQ29	186	A1	216	NC
125	DQ5	156	VSS	187	VDD	217	VSS
126	VSS	157	DM3	KEY		218	DQ46
127	DM0	158	NC	188	CK0	219	DQ47
128	NC	159	VSS	189	CK0#	220	VSS
129	VSS	160	DQ30	190	VDD	221	DQ52
130	DQ6	161	DQ31	191	A0	222	DQ53
131	DQ7	162	VSS	192	BA1	223	VSS
132	VSS	163	CB4	193	VDD	224	NC
133	DQ12	164	CB5	194	RAS#	225	NC
134	DQ13	165	VSS	195	VDDQ	226	VSS
135	VSS	166	DM8	196	CS0#	227	DM6
136	DM1	167	NC	197	VDDQ	228	NC
137	NC	168	VSS	198	ODT0	229	VSS
138	VSS	169	CB6	199	A13	230	DQ54
139	NC	170	CB7	200	VDD	231	DQ55
140	NC	171	VSS	201	NC	232	VSS
141	VSS	172	NC	202	VSS	233	DQ60
142	DQ14	173	VDDQ	203	DQ36	234	DQ61
143	DQ15	174	CKE1*	204	DQ37	235	VSS
144	VSS	175	VDD	205	VSS	236	DM7
145	DQ20	176	A15 *	206	DM4	237	NC
146	DQ21	177	A14 *	207	NC	238	VSS
147	VSS	178	VDDQ	208	VSS	239	DQ62
148	DM2	179	A12	209	DQ38	240	DQ63
149	NC	180	A9	210	DQ39	241	VSS
150	VSS	181	VDD	211	VSS	242	SDA
151	DQ22	182	A8	212	DQ44	243	SCL
152	DQ23	183	A6	213	DQ45	244	VDDSPD
153	VSS	184	VDDQ	214	VSS		

*: These pins are not used in this module.
RESET# (Pin 18) is connected to both OE of the PLL and RESET# of the register

Function Block Diagram



Notes:

1. Unless otherwise noted, resistor values are 22 ohms +/-5%

Absolute Maximum Ratings

Symbol	Parameter		MIN	MAX	Unit
VDD	Voltage on VDD pin relative to VSS		-1.0	2.3	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.5	2.3	V
VDDL	Voltage on VDDL pin relative to VSS		-0.5	2.3	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.5	2.3	V
TSTG	Storage temperature		-55	100	^{0}C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-5	5	uA
		CS#, CKE, ODT	-5	5	uA
		CK, CK#	-250	250	uA
		DM	-5	5	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-18	18	uA

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Notes:
1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

Operating Temperature Condition

Symbol	Parameter		Rating	Units	Notes
TOPER	Operating temperature	Commercial	0 to +95	^{0}C	1,2
		Industrial	-40 to +95		

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At -40 to +85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage (DDR2-400/533/667)	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage (DDR2-400/533/667)	-0.300	VREF - 0.125	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage (DDR2-533/400)	VREF + 0.250	-	V
VIL(AC)	Input Low (Logic 0) Voltage (DDR2-533/400)	-	VREF - 0.250	V
VIH(AC)	Input High (Logic 1) Voltage (DDR2-667)	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage (DDR2-667)	-	VREF - 0.200	V

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	E6 (DDR2-667)		D5 (DDR2-553)		CC (DDR2-400)		Unit
		Min	Max	Min	Max	Min	Max	
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	6.5	7.5	6.5	7.5	6.5	7.5	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	6.5	7.5	6.5	7.5	6.5	7.5	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	6	7	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	6.5	7.5	6.5	8	6.5	8	pF

IDD Specification

Condition		Symbol	E6 (DDR2-667)	D5 (DDR2-533)	CC (DDR2-400)	Unit
Operating one bank active-pre-charge current; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0*	1065	1020	675	mA
Operating one bank active-read-pre-charge current; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; t_{RCD}= $t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W		IDD1*	1155	1110	1065	mA
Pre-charge power-down current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P**	435	435	435	mA
Pre-charge quiet standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q**	660	660	615	mA
Pre-charge standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING		IDD2N**	705	705	660	mA
Active power-down current; All banks open; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	IDD3P**	660	615	615	mA
	Slow PDN Exit MRS(12) = 1		462	462	462	mA
Active standby current; All banks open; t_{CK}= $t_{CK(IDD)}$; t_{RP}= $t_{RP(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N**	840	840	795	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD4W*	1470	1380	1245	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD4R*	1560	1470	1335	mA
Burst refresh current; t_{CK} = $t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5**	1650	1650	1605	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	135	135	135	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)}$ - 1*$t_{CK(IDD)}$; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RRD} = $t_{RRD(IDD)}$; t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		IDD7*	2460	2460	2325	mA

Notes:

IDD specification is based on Samsung D-die components.
*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
**: Value calculated reflects all module ranks in this operating condition.

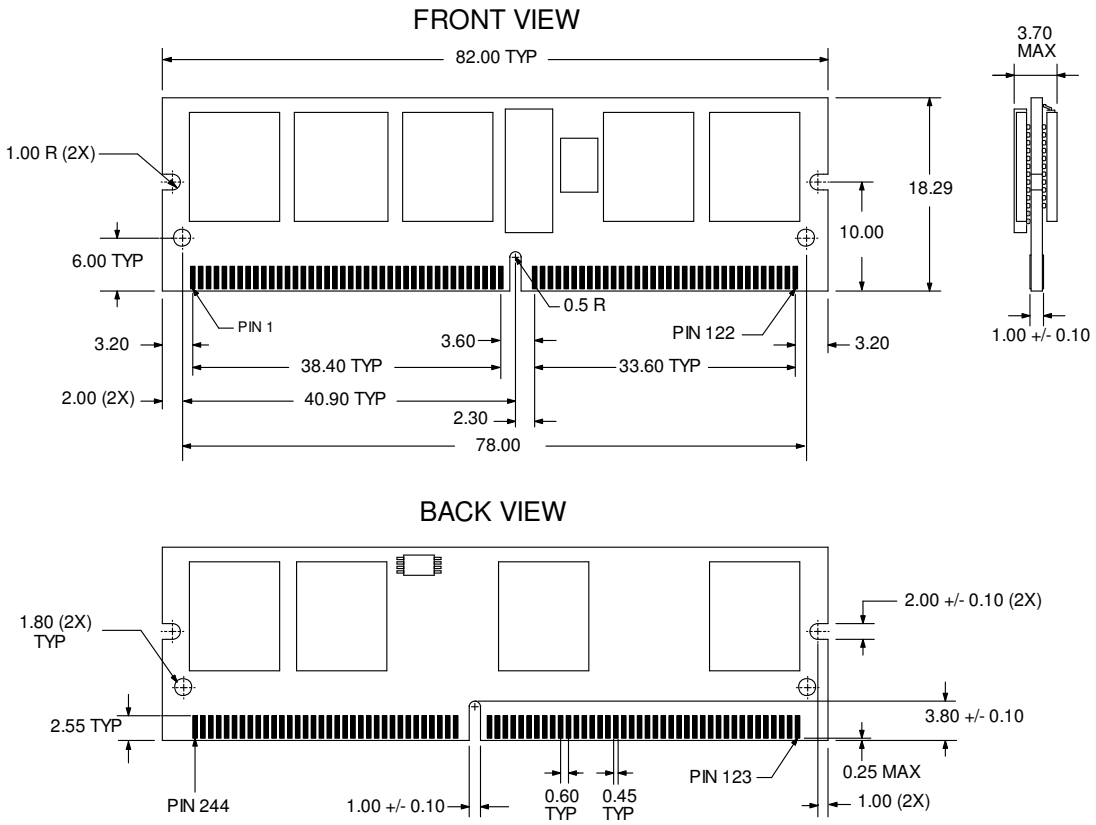
AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	E6 (DDR2-667)		D5 (DDR2-533)		CC (DDR2-400)		Unit
			Max	Min	Max	Min	Max	Min	
Clock Timing									
Clock Cycle Time	CL5	$t_{CK}(5)$	3,000	8,000	-	-	-	-	ps
	CL4	$t_{CK}(4)$	3,750	8,000	3,750	8,000	-	-	ps
	CL3	$t_{CK}(3)$	5000	8000	5000	8000	5000	8000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	0.48	0.52	0.45	0.55	t_{CK}
CK low-level width		$t_{CL(avg)}$	0.48	0.52	0.48	0.52	0.45	0.55	t_{CK}
Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})	-	MIN (t_{CH}, t_{CL})	-	MIN (t_{CH}, t_{CL})	-	ps
Clock jitter		t_{JIT}	-125	125	-	-	-	-	ps
Data Timing									
DQ output access time from CK/CK#		t_{AC}	-450	+450	-500	500	-600	600	ps
Data-out high impedance window from CK/CK#		t_{HZ}	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		t_{LZ}	$t_{AC(MiN)}$	$t_{AC(MAX)}$	$t_{AC(MiN)}$	$t_{AC(MAX)}$	$t_{AC(MiN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		t_{DS}	100	-	100	-	150	-	ps
DQ and DM input hold time relative to DQS		t_{DH}	175	-	225	-	275	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35	-	0.35	-	0.35	-	t_{CK}
Data hold skew factor		t_{QHS}	-	340	-	400	-	450	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	t_{HP} - t_{QHS}	-	ps
Data valid output window (DVW)		t_{DVW}	t_{QH}-t_{DQSQ}	-	t_{QH}-t_{DQSQ}	-	t_{QH}-t_{DQSQ}	-	ns
Data Strobe Timing									
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS output access time from CK/CK#		t_{DQSCK}	-400	+400	-450	+450	-500	+500	ps
DQS failing edge to CK rising-setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS failing edge from CK rising-hold time		t_{DSH}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	240	-	300	-	350	ps
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read preamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS read preamble setup time		t_{WPRES}	0	-	0	-	0	-	ps
DQS read preamble		t_{WPRE}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS read preamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Write command to first DQS latching transition		t_{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	E6 (DDR2-667)		D5 (DDR2-533)		CC (DDR2-400)		Unit
		Min	Max	Min	Max	Min	Max	
Command and Address Timing								
Address and control input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	t_{CK}
Address and control input setup time	t_{IS}	200	-	250	-	350	-	ps
Address and control input hold time	t_{IH}	275	-	375	-	475	-	ps
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	2	-	ps
ACTIVE to ACTIVE (same bank) command	t_{RC}	60	-	60	-	55	-	ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	15	-	15	-	ns
Four Bank Activate period	t_{FAW}	37.5	-	37.5	-	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	40	70,000	ns
Internal READ to precharge Command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns
Write recovery time	t_{WR}	15	-	15	-	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{nRP}$	-	ns
Internal WRITE to READ Command delay	t_{WTR}	7.5	-	7.5	-	10	-	ns
PRECHARGE command period	t_{RP}	15	-	15	-	15	-	ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP}+t_{CK}$	-	$t_{RP}+t_{CK}$	-	$t_{RP}+t_{CK}$	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	ns
Self Refresh								
Refresh to Active or Refresh to Refresh command interval	t_{RFC}	127.5	-	127.5	-	127.5	-	ns
Average periodic Refresh interval	t_{REFI}	-	7.8	-	7.8	-	7.8	us
Exit Self Refresh to non-READ command	t_{XSNR}	$t_{RFC(MIN)}+10$	-	$t_{RFC(MIN)}+10$	-	$t_{RFC(MIN)}+10$	-	ns
Exit Self Refresh to READ	t_{XSRD}	200	-	200	-	200	-	t_{CK}
Exit Self Refresh timing reference	t_{ISXR}	t_{IS}	-	t_{IS}	-	t_{IS}	-	ps
ODT								
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)}+700$	$t_{AC(MIN)}$	$t_{AC(MAX)}+1,000$	$t_{AC(MIN)}$	$t_{AC(MAX)}+1000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	$t_{AC(MIN)}$	$t_{AC(MAX)}+600$	ps
ODT turn-on(power-down mode)	t_{AONPD}	$t_{AC(MIN)}+2,000$	$2 \times t_{CK} + t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2,000$	$2 \times t_{CK} + t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2000$	$2t_{CK} + t_{AC(MAX)}+1000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{AC(MIN)}+2,000$	$2.5 xt_{CK}+ t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2,000$	$2.5 xt_{CK}+ t_{AC(MAX)}+1,000$	$t_{AC(MIN)}+2000$	$2.5xt_{CK} + t_{AC(MAX)}+1000$	ps
ODT to power-down entry latency	t_{ANPD}	3	-	3	-	3	-	t_{CK}
ODT power-down exit latency	t_{AXPD}	8	-	8	-	8	-	t_{CK}
Power Down								
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	2	-	2	-	t_{CK}
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	7-AL	-	6-AL	-	6-AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	2	-	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	3	-	3	-	t_{CK}

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
05/11/2011	1.0	All	Spec released