Product Specifications		
PART NO.:	**VL493T5263T-F7Y/E7Y/E6Y**	**REV: 1.1**

General Information

4GB 512Mx72 DDR2 SDRAM ECC REGISTERED SO-RDIMM 200-PIN WITH THERMAL SENSOR

Description

The VL493T5263T is a 512Mx72 DDR2 SDRAM high density SO-RDIMM. This memory module is dual rank, consists of eighteen CMOS 256Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, two 25-bit registered buffers in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROMs with thermal sensor in an 8-pin MLF package. This module is a 200-pin registered small-outline dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

- 200-pin, registered small-outline dual in-line memory module (SO-RDIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rates: PC2-6400, PC2-5300
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 3.0V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 5, 6 (DDR2-800), 5 (DDR2-667)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM built-in thermal sensor
- Thermal sensor range: -20°C to +125°C (+/-1°C accuracy)
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 30.00mm (1.181”), double sided components

Order Information:

VL493T5263T-F7 Y X

- DRAM DIE (Option)
- DRAM MANUFACTURER
  Y - HYNIX
- MODULE SPEED
  F7: PC2-6400 @ CL5
  E7: PC2-6400 @ CL6
  E6: PC2-5300 @ CL5
- VL: Lead-free/RoHS

Pin Description

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
CB0~CB7	Check Bits
DM0~DM8	Data Masks
CK0, CK0#	Clock Input
ODT0, ODT1	On-die Termination Control
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 3.0V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

Pin Configuration

200-PIN DDR2 SO-RDIMM FRONT

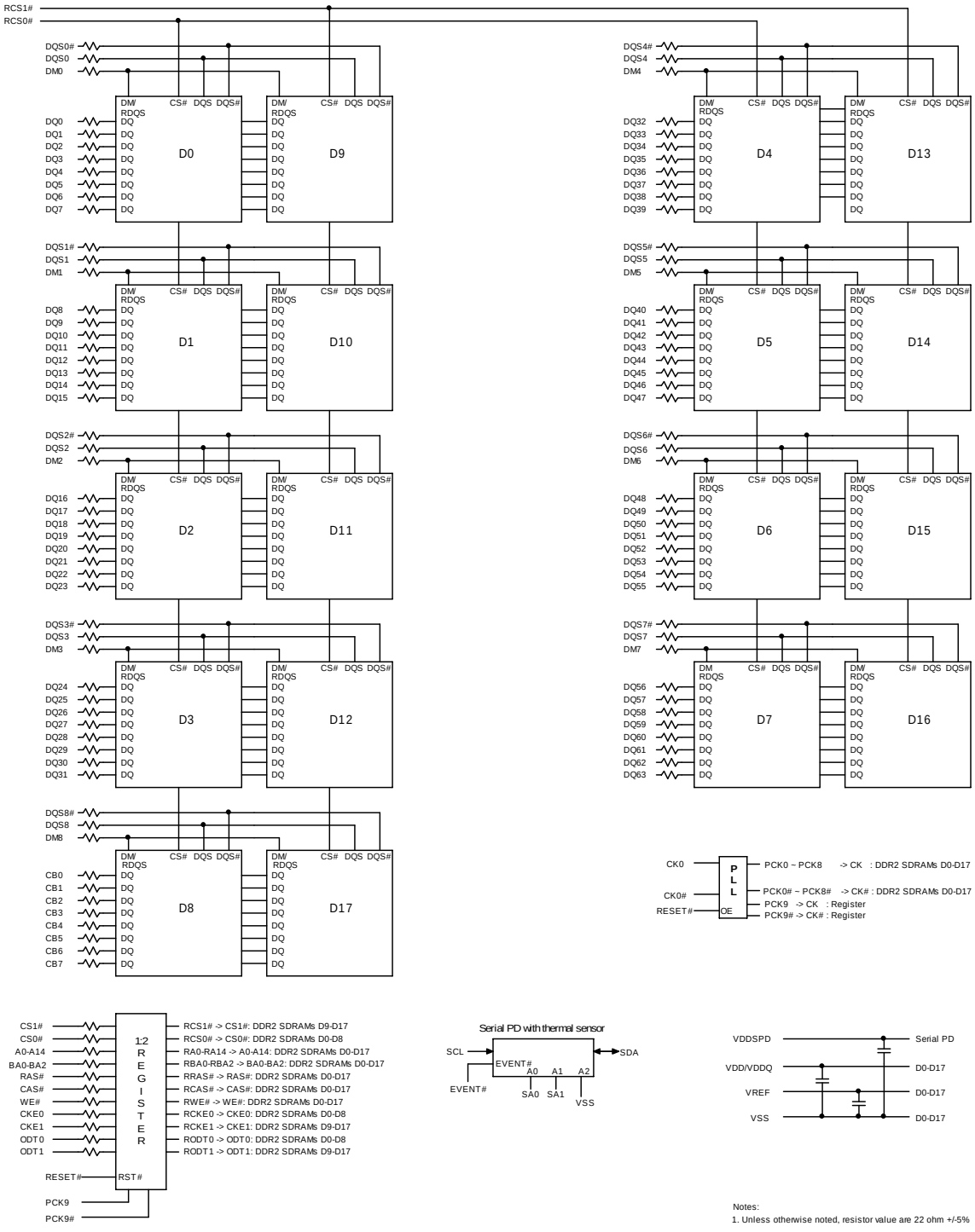
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	51	DQ18	101	VDD	151	VSS
3	DQ0	53	DQ19	103	A5	153	DQS5#
5	VSS	55	VSS	105	A3	155	DQS5
7	DQ1	57	DQ24	107	A2	157	VSS
9	DQS0#	59	DQ25	109	VDD	159	DQ42
11	DQS0	61	VSS	111	A10/AP	161	DQ43
13	VSS	63	DQS3#	113	BA0	163	VSS
15	DQ2	65	DQS3	115	RAS#	165	DQ48
17	DQ3	67	VSS	117	VDD	167	DQ49
19	VSS	69	DQ26	119	CAS#	169	VSS
21	DQ8	71	DQ27	121	CS1#	171	DQS6#
23	DQ9	73	VSS	123	VDD	173	DQS6
25	VSS	75	CB0	125	ODT1	175	VSS
27	DQS1#	77	CB1	127	CS3# *	177	DQ50
29	DQS1	79	VSS	129	DQ32	179	DQ51
31	VSS	81	DQS8#	131	VSS	181	VSS
33	DQ10	83	DQS8	133	DQ33	183	DQ56
35	DQ11	85	VSS	135	DQS4#	185	DQ57
37	VSS	87	CKE0	137	DQS4	187	VSS
39	DQ16	89	CKE1	139	VSS	189	DQS7#
41	DQ17	91	CS2# *	141	DQ34	191	DQS7
43	VSS	93	VDD	143	DQ35	193	DQ58
45	DQS2#	95	A12	145	VSS	195	VSS
47	DQS2	97	A9	147	DQ40	197	DQ59
49	VSS	99	A7	149	DQ41	199	VDDSPD

200-PIN DDR2 SO-RDIMM BACK

Pin	Name	Pin	Name	Pin	Name	Pin	Name
2	VSS	52	VSS	102	A6	152	VSS
4	DQ4	54	DQ28	104	A4	154	DM5
6	DQ5	56	DQ29	106	VDD	156	VSS
8	VSS	58	VSS	108	A1	158	DQ46
10	DM0	60	DM3	110	A0	160	DQ47
12	VSS	62	VSS	112	BA1	162	VSS
14	DQ6	64	DQ30	114	VDD	164	DQ52
16	DQ7	66	DQ31	116	WE#	166	DQ53
18	VSS	68	VSS	118	CS0#	168	VSS
20	DQ12	70	CB4	120	ODT0	170	DM6
22	DQ13	72	CB5	122	A13	172	VSS
24	VSS	74	VSS	124	VDD	174	DQ54
26	DM1	76	DM8	126	CK0	176	DQ55
28	VSS	78	VSS	128	CK0#	178	VSS
30	DQ14	80	CB6	130	VSS	180	DQ60
32	DQ15	82	CB7	132	DQ36	182	DQ61
34	VSS	84	VSS	134	DQ37	184	VSS
36	DQ20	86	CB2	136	VSS	186	DM7
38	DQ21	88	CB3	138	DM4	188	DQ62
40	VSS	90	VSS	140	VSS	190	VSS
42	RESET#	92	BA2	142	DQ38	192	DQ63
44	DM2	94	A14	144	DQ39	194	SDA
46	VSS	96	A11	146	VSS	196	SCL
48	DQ22	98	VDD	148	DQ44	198	SA1
50	DQ23	100	A8	150	DQ45	200	SA0

*: These pins are not used in this module.
Note: RESET# (pin 42) is connected to both OE of the PLL and Reset of the register for 72-bit registered SO-RDIMM only.

Function Block Diagram



Notes:
1. Unless otherwise noted, resistor value are 22 ohm +/-5%

Absolute Maximum Ratings

Symbol	Parameter		MIN	MAX	Unit
VDD	Voltage on VDD pin relative to VSS		-1.0	2.3	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.5	2.3	V
VDDL	Voltage on VDDL pin relative to VSS		-0.5	2.3	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.5	2.3	V
TSTG	Storage temperature		-55	100	^{0}C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#, CKE, ODT	-5	5	uA
		CS#	-10	10	uA
		CK, CK#	-250	+250	uA
		DM	-4	4	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-36	36	uA

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Note:
1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.

Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 95	^{0}C	1,2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2.
2. At 0 – 85^{o}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{o}C < TOPER <= 95^{o}C.

Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.200	V

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	9	11	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	9	11	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	9	11	pF

IDD Specification

Condition		Symbol	F7 (DDR2-800)	E7 (DDR2-800)	E6 (DDR2-667)	Unit
Operating one bank active-pre-charge; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0*	1463	1463	1418	mA
Operating one bank active-read-pre-charge; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; t_{RCD}= $t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1*	1553	1553	1508	mA
Pre-charge power-down current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P**	716	716	716	mA
Pre-charge quiet standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q**	1400	1400	1310	mA
Pre-charge standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING.		IDD2N**	1490	1490	1400	mA
Active power-down current; All banks open; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	IDD3P**	1130	1130	1130	mA
	Slow PDN Exit MRS(12) = 1		824	824	824	mA
Active standby current; All banks open; t_{CK}= $t_{CK(IDD)}$; t_{RP}= $t_{RP(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N**	1940	1940	1760	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; $t_{RAS=\ tRAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD4W*	2768	2768	2408	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$); t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD4R*	2588	2588	2273	mA
Burst refresh current; t_{CK}=$t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5**	4640	4640	4460	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	270	270	270	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)}$ - 1*$t_{CK(IDD)}$; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RRD} = $t_{RRD(IDD)}$; t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		IDD7*	3353	3353	3128	mA

Notes: IDD specification is based on Hynix A-die components.
*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
**: Value calculated reflects all module ranks in this operating condition.

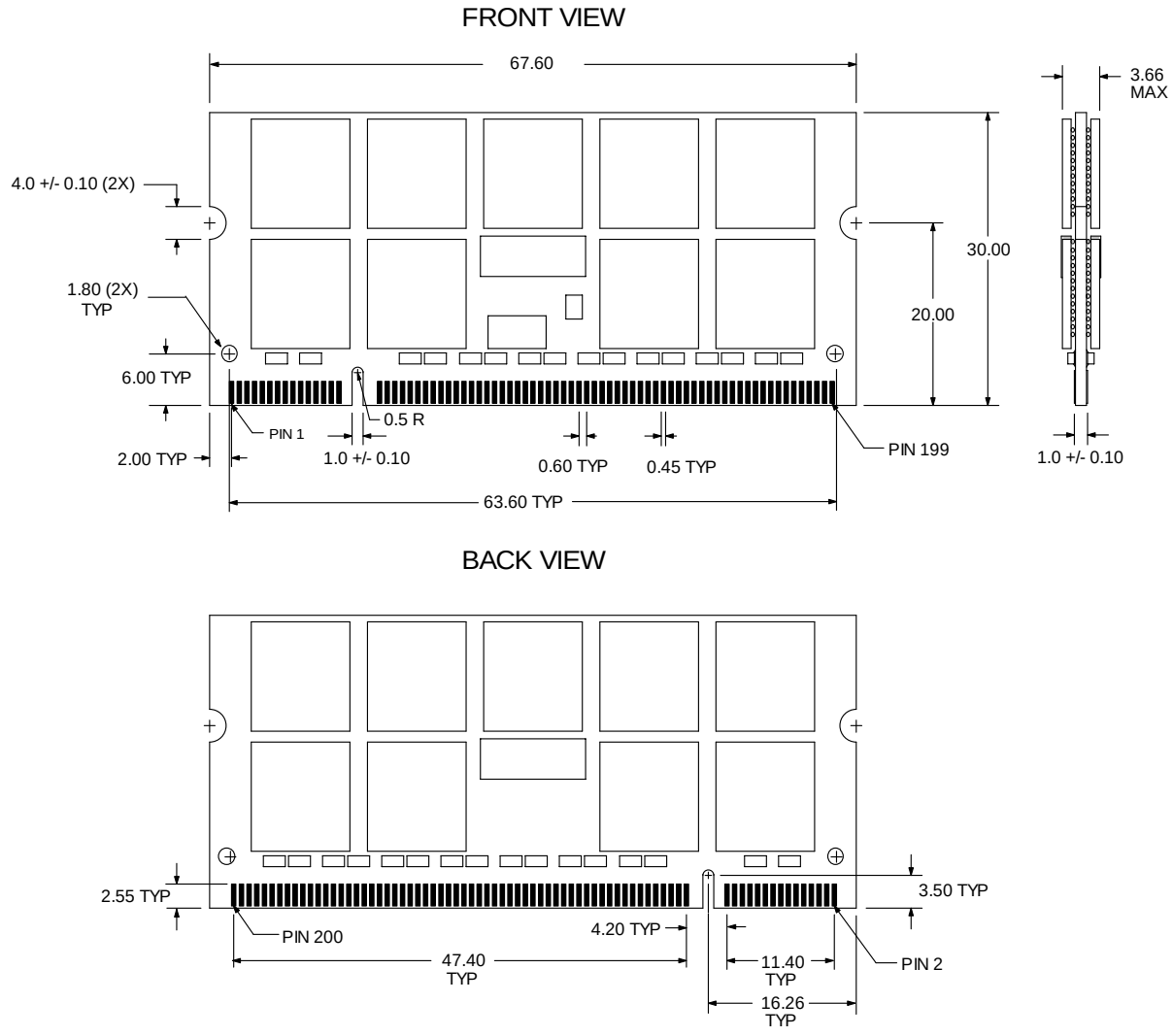
AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	F7 (DDR2-800)		E7 (DDR2-800)		E6 (DDR2-667)		Unit
			Min	Max	Min	Max	Min	Max	
Clock Timing									
Clock Cycle Time	CL6	$t_{CK}(6)$	-	8000	2,500	8,000	-	-	ps
	CL5	$t_{CK}(5)$	2500	8000	3,000	8,000	3,000	8,000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
CK low-level width		$t_{CL(avg)}$	0.48	0.52	0.48	0.52	0.48	0.52	t_{CK}
Half clock period		t_{HP}	MIN (tCH,tCL)	-	MIN (t_{CH}, t_{CL})	-	MIN (t_{CH}, t_{CL})	-	ps
Clock jitter		t_{JIT}	-100	100	-100	100	-125	125	ps
Data Timing									
DQ output access time from CK/CK#		t_{AC}	-400	400	-400	400	-450	+450	ps
Data-out high impedance window from CK/CK#		t_{HZ}	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		t_{LZ}	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		t_{DS}	50	-	50	-	100	-	ps
DQ and DM input hold time relative to DQS		t_{DH}	125	-	125	-	175	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35	-	0.35	-	0.35	-	t_{CK}
Data hold skew factor		t_{QHS}	-	300	-	300	-	340	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	$t_{HP} - t_{QHS}$	-	ps
Data Strobe Timing									
DQS input high pulse width		t_{DQSH}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS output access time from CK/CK#		t_{DQSCK}	-350	+350	-350	+350	-400	+400	ps
DQS failing edge to CK rising-setup time		t_{DSS}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS failing edge from CK rising-hold time		t_{DSH}	0.2	-	0.2	-	0.2	-	t_{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	200	-	200	-	240	ps
DQS read preamble		t_{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t_{CK}
DQS read preamble		t_{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
DQS read preamble		t_{WPRE}	0.35	-	0.35	-	0.35	-	t_{CK}
DQS read preamble		t_{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t_{CK}
Write command to first DQS latching transition		t_{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t_{CK}

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	F7 (DDR2-800)		E7 (DDR2-800)		E6 (DDR2-667)		Unit
		Min	Max	Min	Max	Min	Max	
Command and Address Timing								
Address and control input pulse width for each input	t_{IPW}	0.6	-	0.6	-	0.6	-	t_{CK}
Address and control input setup time	t_{IS}	175	-	175	-	200	-	ps
Address and control input hold time	t_{IH}	250	-	250	-	275	-	ps
CAS# to CAS# command delay	t_{CCD}	2	-	2	-	2	-	ps
ACTIVE to ACTIVE (same bank) command	t_{RC}	57.5	-	57.5/60	-	60	-	ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}			7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	12.5	-	12.5/15	-	15	-	ns
Four Bank Activate period	t_{FAW}	37.5	-	35	-	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	45	70,000	45	70,000	45	70,000	ns
Internal READ to precharge Command delay	t_{RTP}	7.5	-	7.5	-	7.5	-	ns
Write recovery time	t_{WR}	15	-	15	-	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR}+t_{RP}$	-	$t_{WR}+t_{nRP}$	-	$t_{WR}+t_{nRP}$	-	nCK
Internal WRITE to READ Command delay	t_{WTR}	7.5	-	7.5	-	7.5	-	ns
PRECHARGE command period	t_{RP}	12.5	-	15	-	15	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	2	-	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	$t_{IS}+t_{CK}+t_{IH}$	-	ns
Self Refresh								
Refresh to Active or Refresh to Refresh command interval	t_{RFC}	127.5	-	195	-	195	-	ns
Average periodic Refresh interval	t_{REFI}	-	7.8	-	7.8	-	7.8	us
Exit Self Refresh to non-READ command	t_{XSNR}	$t_{RFC(MIN)}$ +10	-	$t_{RFC(MIN)}$ +10	-	$t_{RFC(MIN)}$ +10	-	ns
Exit Self Refresh to READ	t_{XSRD}	200	-	200	-	200	-	t_{CK}
ODT								
ODT turn-on delay	t_{AOND}	2	2	2	2	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 600	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 700	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 700	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 600	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 600	$t_{AC(MIN)}$	$t_{AC(MAX)}$+ 600	ps
ODT turn-on(power-down mode)	t_{AONPD}	$t_{AC(MIN)}$+ 2000	2 x t_{CK} + $t_{AC(MAX)}$+ 1000	$t_{AC(MIN)}$+ 2,000	$2t_{CK}$ + $t_{AC(MAX)}$+ 1,000	$t_{AC(MIN)}$+ 2,000	$2t_{CK}$ + $t_{AC(MAX)}$+ 1,000	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{AC(MIN)}$+ 2000	2.5 x t_{CK}+ $t_{AC(MAX)}$+ 1000	$t_{AC(MIN)}$+ 2,000	$2.5t_{CK}$ + $t_{AC(MAX)}$+ 1,000	$t_{AC(MIN)}$+ 2,000	$2.5t_{CK}$ + $t_{AC(MAX)}$+ 1,000	ps
ODT to power-down entry latency	t_{ANPD}	3	-	3	-	3	-	t_{CK}
ODT power-down exit latency	t_{AXPD}	8	-	8	-	8	-	t_{CK}
OCD drive mode output delay	t_{OIT}	0	1,200	0	1,200	0	1,200	ps
Power Down								
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	2	-	2	-	t_{CK}
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	8-AL	-	8-AL	-	7-AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	2	-	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	3	-	3	-	t_{CK}

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
12/21/2009	1.0	All	Spec release
12/14/2010	1.1	All	Update spec