

Product Specifications

PART NO.:

VL393T5663E-E7M/E6M/D5M
REV: 1.1

General Information

2GB 256Mx72 DDR2 SDRAM VLP ECC REGISTERED DIMM 240-PIN

Description

The VL393T5663E is a 256Mx72 DDR2 SDRAM high density DIMM. This memory module is dual rank, consists of eighteen CMOS 128Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, two 25-bit registered buffers in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin MLF package. This module is a 240-pin dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

- 240-pin, registered dual in-line memory module (RDIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rates: PC2-6400, PC2-5300, PC2-4200
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 6 (DDR2-800), 5 (DDR2-667)
4 (DDR2-533)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 18.29mm (0.720"), double sided components

Pin Description

Pin Name	Function
A0-A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0-BA2	Bank Address Inputs
DQ0-DQ63	Data Input/Output
DQS0-DQS8	Data Strobes
DQS0#-DQS8#	Data Strobes Complement
CB0-CB7	Check Bits
DM0-DM8	Data Masks
CK0, CK0#	Clock Input
ODT0, ODT1	On-die Termination Control
CKE0, CKE1	Clock Enables
CS0#, CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
RESET#	Reset Input
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0-SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

Order Information:

VL393T5663E - E7 M X

DRAM DIE (Option)

DRAM MANUFACTURER
M - MICRON

MODULE SPEED
E7: PC2-6400 @ CL6
E6: PC2-5300 @ CL5
D5: PC2-4200 @ CL4

VL: Lead-free/RoHS

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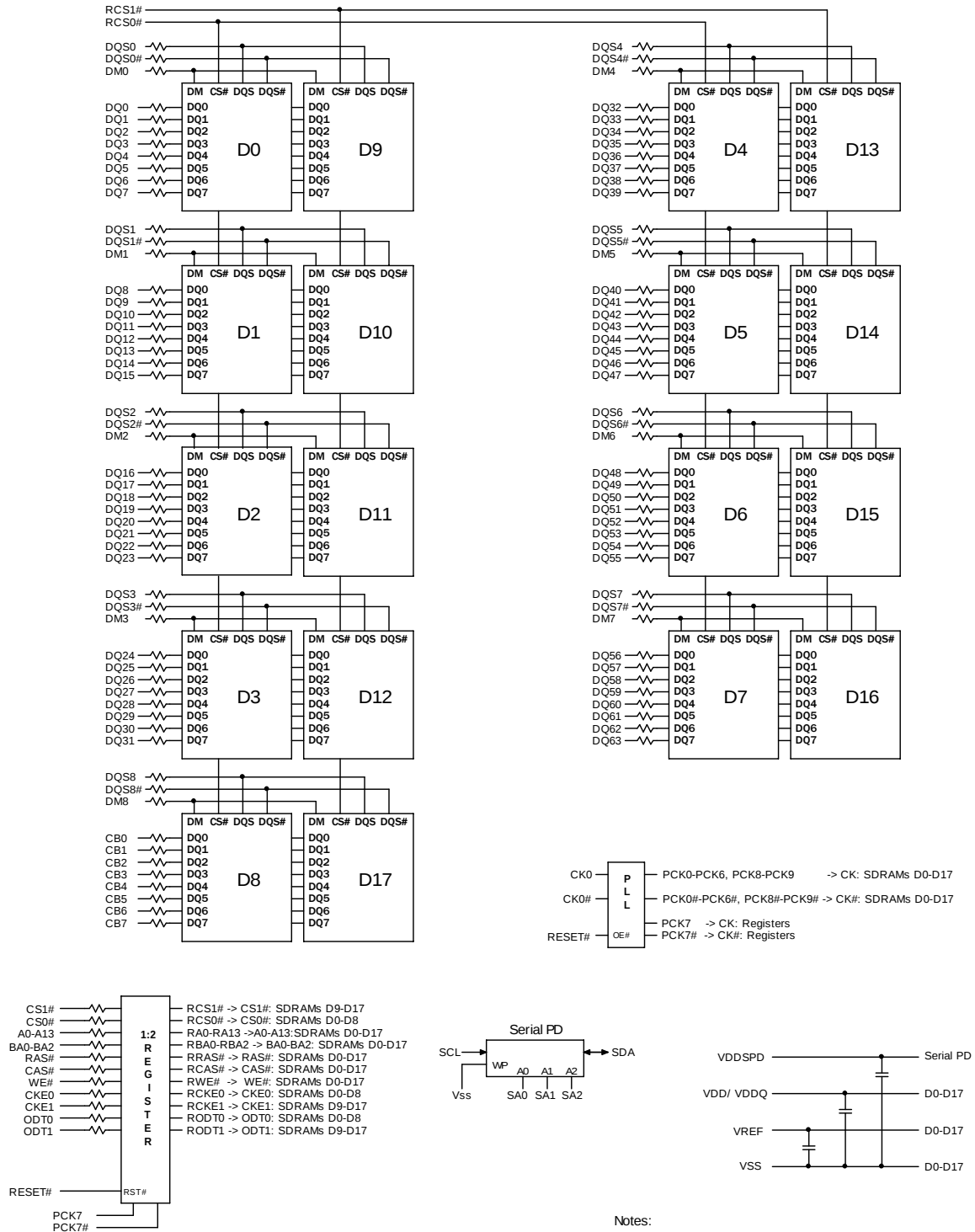
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Pin Configuration

240-PIN DDR2 RDIMM FRONT								240-PIN DDR2 RDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC	156	NC	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	NC
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	CB4	191	VDDQ	221	NC
12	DQ8	42	CB0	72	VDDQ	102	NC	132	DQ13	162	CB5	192	RAS#	222	VSS
13	DQ9	43	CB1	73	WE#	103	VSS	133	VSS	163	VSS	193	CS0#	223	DM6
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1	164	DM8	194	VDDQ	224	NC
15	DQS1#	45	DQS8#	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	DQS8	76	CS1#	106	VSS	136	VSS	166	VSS	196	A13	226	DQ54
17	VSS	47	VSS	77	ODT1	107	DQ50	137	NC	167	CB6	197	VDD	227	DQ55
18	RESET#	48	CB2	78	VDDQ	108	DQ51	138	NC	168	CB7	198	VSS	228	VSS
19	NC	49	CB3	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC/A15	203	NC	233	NC
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	NC/A14	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

Function Block Diagram



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Absolute Maximum Ratings

Absolute Maximum Ratings					
Symbol	Parameter		MIN	MAX	Unit
VDD	Voltage on VDD pin relative to VSS		-1.0	2.3	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.5	2.3	V
VDDL	Voltage on VDDL pin relative to VSS		-0.5	2.3	V
VIN, VOUT	Voltage on any pin relative to VSS		-0.5	2.3	V
TSTG	Storage temperature		-55	150	°C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-5	5	uA
		CS#, CKE, ODT	-5	5	uA
		CK, CK#	-250	250	uA
		DM	-10	10	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-36	36	uA

DC Operating Conditions

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Note:

- VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
- VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
- VDDQ tracks with VDD; VDDL tracks with VDD.

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Operating Temperature Condition

Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 85	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 – 85°C, operation temperature range, all DRAM specifications will be supported.				

Input DC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level

All voltages referenced to VSS

Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage DDR2-533	VREF + 0.250	-	V
VIL(AC)	Input Low (Logic 0) Voltage DDR2-533	-	VREF - 0.250	V
VIH(AC)	Input High (Logic 1) Voltage DDR2-800/667	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage DDR2-800/667	-	VREF - 0.200	V

Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	6.5	7.5	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	6.5	7.5	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	9	12	pF

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IDD Specification

Condition		Symbol	E7 (DDR2-800)	E6 (DDR2-667)	D5 (DDR2-533)	Unit
Operating one bank active-pre-charge; t _{CK} = t _{CK(IDD)} ; t _{RC} = t _{RC(IDD)} ; t _{RAS} = t _{RAS MIN(IDD)} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD0*	1273	1228	1093	mA
Operating one bank active-read-pre-charge; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t _{CK} = t _{CK(IDD)} ; t _{RC} = t _{RC(IDD)} ; t _{RAS} = t _{RAS MIN(IDD)} ; t _{RCD} = t _{RCD(IDD)} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD1*	1453	1363	1318	mA
Pre-charge power-down current; All banks idle; t _{CK} = t _{CK(IDD)} ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2P**	526	526	526	mA
Pre-charge quiet standby current; All banks idle; t _{CK} = t _{CK(IDD)} ; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING		IDD2Q**	1300	1120	1120	mA
Pre-charge standby current; All banks idle; t _{CK} = t _{CK(IDD)} ; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING.		IDD2N**	1300	1120	1120	mA
Active power-down current; All banks open; t _{CK} = t _{CK(IDD)} ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	IDD3P**	1120	940	940	mA
	Slow PDN Exit MRS(12) = 1		580	580	580	mA
Active standby current; All banks open; t _{CK} = t _{CK(IDD)} ; t _{RP} = t _{RP(IDD)} ; t _{RAS} = t _{RAS MAX(IDD)} ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD3N**	1480	1390	1210	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; t _{CK} = t _{CK(IDD)} ; t _{RAS} = t _{RAS MAX(IDD)} ; t _{RP} = t _{RP(IDD)} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING		IDD4W*	1903	1678	1588	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; t _{CK} = t _{CK(IDD)} ; t _{RAS} = t _{RAS MAX(IDD)} ; t _{RP} = t _{RP(IDD)} ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.		IDD4R*	1903	1678	1588	mA
Burst refresh current; t _{CK} =t _{CK(IDD)} ; Refresh command at every t _{RFC(IDD)} interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.		IDD5**	4630	4270	4180	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	126	126	126	mA
Operating bank interleaved read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL=CL(IDD); AL = t _{RCD(IDD)} - 1*t _{CK(IDD)} ; t _{CK} = t _{CK(IDD)} ; t _{RC} = t _{RC(IDD)} ; t _{RRD} = t _{RRD(IDD)} ; t _{RCD} = 1*t _{CK(IDD)} ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.		IDD7*	3478	2983	2893	mA

Notes: IDD specification is based on Micron H-die components.

*: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.

**: Value calculated reflects all module ranks in this operating condition.

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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	E7 (DDR2-800)		E6 (DDR2-667)		D5 (DDR2-533)		Unit
			Min	Max	Min	Max	Max	Min	
Clock Timing									
Clock Cycle Time	CL6	t _{CK} (6)	2500	8000	-	-	-	-	ps
	CL5	t _{CK} (5)	3000	8000	3000	8000	-	-	ps
	CL4	t _{CK} (4)	3750	8000	3750	8000	3750	8000	ps
CK high-level width		t _{CH} (avg)	0.48	0.52	0.48	0.52	0.48	0.52	t _{CK}
CK low-level width		t _{CL} (avg)	0.48	0.52	0.48	0.52	0.48	0.52	t _{CK}
Half clock period		t _{HP}	MIN (t _{CH} , t _{CL})	-	MIN (t _{CH} , t _{CL})	-	MIN (t _{CH} , t _{CL})	-	ps
Clock jitter		t _{JIT}	-100	100	-125	125	-125	125	ps
Data Timing									
DQ output access time from CK/CK#		t _{AC}	-400	400	-450	+450	-500	500	ps
Data-out high impedance window from CK/CK#		t _{HZ}	-	t _{AC} (MAX)	-	t _{AC} (MAX)	-	t _{AC} (MAX)	ps
Data-out low impedance window from CK/CK#		t _{LZ}	t _{AC} (MIN)	t _{AC} (MAX)	t _{AC} (MIN)	t _{AC} (MAX)	t _{AC} (MIN)	t _{AC} (MAX)	ps
DQ and DM input setup time relative to DQS		t _{DS}	50	-	100	-	100	-	ps
DQ and DM input hold time relative to DQS		t _{DH}	125	-	175	-	225	-	ps
DQ and DM input pulse width (for each input)		t _{DIPW}	0.35	-	0.35	-	0.35	-	t _{CK}
Data hold skew factor		t _{QHS}	-	300	-	340	-	400	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t _{QH}	t _{HP} - t _{QHS}	-	t _{HP} - t _{QHS}	-	t _{HP} - t _{QHS}	-	ps
Data valid output window (DVW)		t _{DVW}	t _{QH} -t _{DQSQ}	-	t _{QH} -t _{DQSQ}	-	t _{QH} -t _{DQSQ}	-	ns
Data Strobe Timing									
DQS input high pulse width		t _{DQSH}	0.35	-	0.35	-	0.35	-	t _{CK}
DQS input low pulse width		t _{DQSL}	0.35	-	0.35	-	0.35	-	t _{CK}
DQS output access time from CK/CK#		t _{DQSCK}	-350	+350	-400	+400	-450	+450	ps
DQS failing edge to CK rising-setup time		t _{DSS}	0.2	-	0.2	-	0.2	-	t _{CK}
DQS failing edge from CK rising-hold time		t _{DSH}	0.2	-	0.2	-	0.2	-	t _{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t _{DQSQ}	-	200	-	240	-	300	ps
DQS read preamble		t _{RPRE}	0.9	1.1	0.9	1.1	0.9	1.1	t _{CK}
DQS read preamble		t _{RPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}
DQS read preamble setup time		t _{WPRES}	0	-	0	-	0	-	ps
DQS read preamble		t _{WPRE}	0.35	-	0.35	-	0.25	-	t _{CK}
DQS read preamble		t _{WPST}	0.4	0.6	0.4	0.6	0.4	0.6	t _{CK}
Write command to first DQS latching transition		t _{DQSS}	WL-0.25	WL+0.25	WL-0.25	WL+0.25	WL-0.25	WL+0.25	t _{CK}

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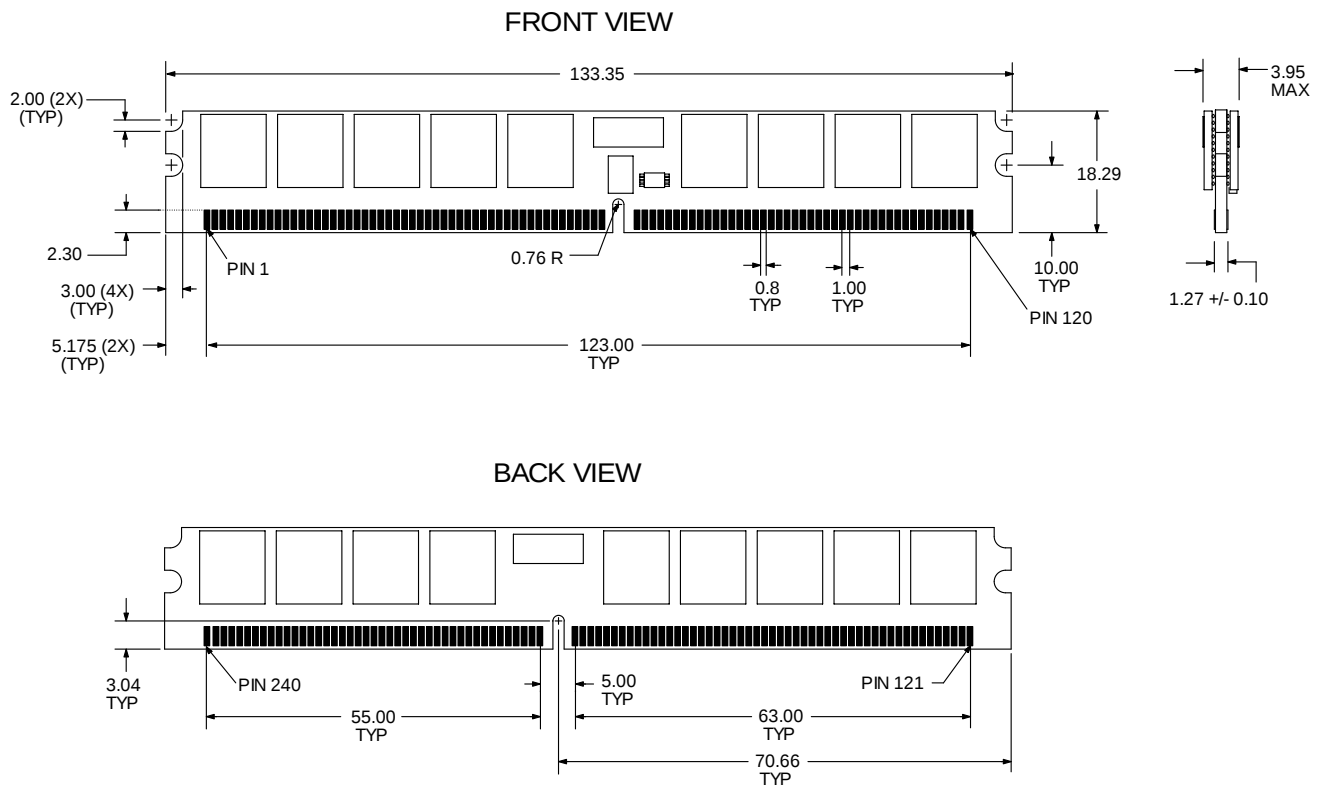
Parameter	Symbol	E7 (DDR2-800)		E6 (DDR2-667)		D5 (DDR2-533)		Unit
		Min	Max	Min	Max	Min	Max	
Command and Address Timing								
Address and control input pulse width for each input	t _{IPW}	0.6	-	0.6	-	0.6	-	t _{CK}
Address and control input setup time	t _{IS}	175	-	200	-	250	-	ps
Address and control input hold time	t _{IH}	250	-	275	-	375	-	ps
CAS# to CAS# command delay	t _{CCD}	2	-	2	-	2	-	t _{CK}
ACTIVE to ACTIVE (same bank) command	t _{RC}	60	-	60	-	60	-	ns
ACTIVE bank a to ACTIVE bank b command	t _{RRD}	7.5	-	7.5	-	7.5	-	ns
ACTIVE to READ or WRITE delay	t _{RCD}	15	-	15	-	15	-	ns
Four Bank Activate period	t _{FAW}	37.5	-	37.5	-	37.5	-	ns
ACTIVE to PRECHARGE command	t _{RAS}	45	70,000	45	70,000	45	70,000	ns
Internal READ to precharge Command delay	t _{RTP}	7.5	-	7.5	-	7.5	-	ns
Write recovery time	t _{WR}	15	-	15	-	15	-	ns
Auto precharge write recovery + precharge time	t _{DAL}	t _{WR} +t _{RP}	-	t _{WR} +t _{RP}	-	t _{WR} +t _{RP}	-	t _{CK}
Internal WRITE to READ Command delay	t _{WTR}	7.5	-	7.5	-	7.5	-	ns
PRECHARGE command period	t _{RP}	15	-	15	-	15	-	ns
PRECHARGE ALL command period	t _{RPA}	t _{RP} +t _{CK}	-	t _{RP} +t _{CK}	-	t _{RP} +t _{CK}	-	ns
LOAD MODE command cycle time	t _{MRD}	2	-	2	-	2	-	t _{CK}
CKE low to CK, CK# uncertainty	t _{DELAY}	t _{IS} +t _{CK} +t _{IH}	-	t _{IS} +t _{CK} +t _{IH}	-	t _{IS} +t _{CK} +t _{IH}	-	ns
Self Refresh								
Refresh to Active or Refresh to Refresh command interval	t _{RFC}	127.5	-	127.5	-	127.5	-	ns
Average periodic Refresh interval	t _{REFI}	-	7.8	-	7.8	-	7.8	us
Exit Self Refresh to non-READ command	t _{XSNR}	t _{RFC(MIN)} +10	-	t _{RFC(MIN)} +10	-	t _{RFC(MIN)} +10	-	ns
Exit Self Refresh to READ	t _{XSRD}	200	-	200	-	200	-	t _{CK}
Exit Self Refresh timing reference	t _{ISXR}	t _{IS}	-	t _{IS}	-	t _{IS}	-	ps
ODT								
ODT turn-on delay	t _{AOND}	2	2	2	2	2	2	t _{CK}
ODT turn-on	t _{AON}	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +700	t _{AC(MIN)}	t _{AC(MAX)} +1000	ps
ODT turn-off delay	t _{AOFD}	2.5	2.5	2.5	2.5	2.5	2.5	t _{CK}
ODT turn-off	t _{AOF}	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	t _{AC(MIN)}	t _{AC(MAX)} +600	ps
ODT turn-on(power-down mode)	t _{AONPD}	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2 x t _{CK} + t _{AC(MAX)} +1000	ps
ODT turn-off (power-down mode)	t _{AOFPD}	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	t _{AC(MIN)} +2000	2.5 x t _{CK} + t _{AC(MAX)} +1000	ps
ODT to power-down entry latency	t _{ANPD}	3	-	3	-	3	-	t _{CK}
ODT power-down exit latency	t _{AXPD}	8	-	8	-	8	-	t _{CK}
Power Down								
Exit active power-down to READ command, MR[bit12=0]	t _{XARD}	2	-	2	-	2	-	t _{CK}
Exit active power-down to READ command, MR[bit12=1]	t _{XARDS}	8-AL	-	7-AL	-	6-AL	-	t _{CK}
Exit precharge power-down to any non-READ command	t _{XP}	2	-	2	-	2	-	t _{CK}
CKE minimum high/low time	t _{CKE}	3	-	3	-	3	-	t _{CK}

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Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.

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Revision History:

Date	Rev.	Page	Changes
07/01/2008	1.0	All	Spec release
12/21/2010	1.1	1, 6	Update General Information on page 1 Update IDD specification table for using Micron DRAM H-die on page 6