Product Specifications

PART NO: **VL53B5263A-K9S-F8S-E7S** | **REV: 1.0**

General Information

4GB 512MX72 DDR3 SDRAM ECC 244 PIN Mini-RDIMM

Description: The VL53B5263A is a 512Mx72 DDR3 SDRAM high density Mini-RDIMM. This memory module consists of eighteen CMOS 256Mx8 bit with 8 banks DDR3 Synchronous DRAMs in BGA packages, a 28-bit registered buffer/PLL clock in BGA package, and a 2K EEPROM with thermal sensor in an 8-pin MLF package. This module is a 244-pin mini dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features:

- 244-pin, mini dual in-line memory module (Mini-RDIMM)
- JEDEC pin-out
- Fast data transfer rates: PC3-10600, PC3-8500, PC3-6400
- VDD = VDDQ = 1.5V +/- 0.075V
- VDDSPD = 3V to 3.6V
- JEDEC standard 1.5V +/- 0.075V I/O (SSTL_15 compatible)
- Eight internal component banks for concurrent operation
- 8-bit pre-fetch architecture
- Bi-directional Differential Data-Strobe
- Programmable CAS# latency: 9 (DDR3-1333), 7 (DDR3-1066), 6 (DDR3-800)
- Programmable burst; length (8)
- On-die termination (ODT)
- Average refresh period 7.8 us
- Asynchronous Reset
- Fly-by topology
- Terminated command, address, and control bus
- Gold edge PCB contacts
- Lead-free, RoHS compliant
- Serial presence detect (SPD) with EEPROM with thermal sensor
- Thermal sensor range: -20^{0}C to +125^{0}C (+/- 1^{0}C Accuracy)
- PCB: Height 30mm (1.181”), double sided components

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Inputs/ Auto Precharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
ODT0, ODT1	On-die Termination Control
CK0, CK0#	Clock Input
CKE0, CKE1	Clock Enables
CS0#~CS1#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply 1.5V +/- 0.075V
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
DM0~DM8	Data Masks
CB0~CB7	Data Check Bits I/O
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage Supply 3V to 3.6V
VTT	Termination Voltage
RESET#	Register and SDRAM Control
EVENT#	Reserved for Temp Sensing
NC	No Connect

Order Information:

VL53B5263A-K9 S X

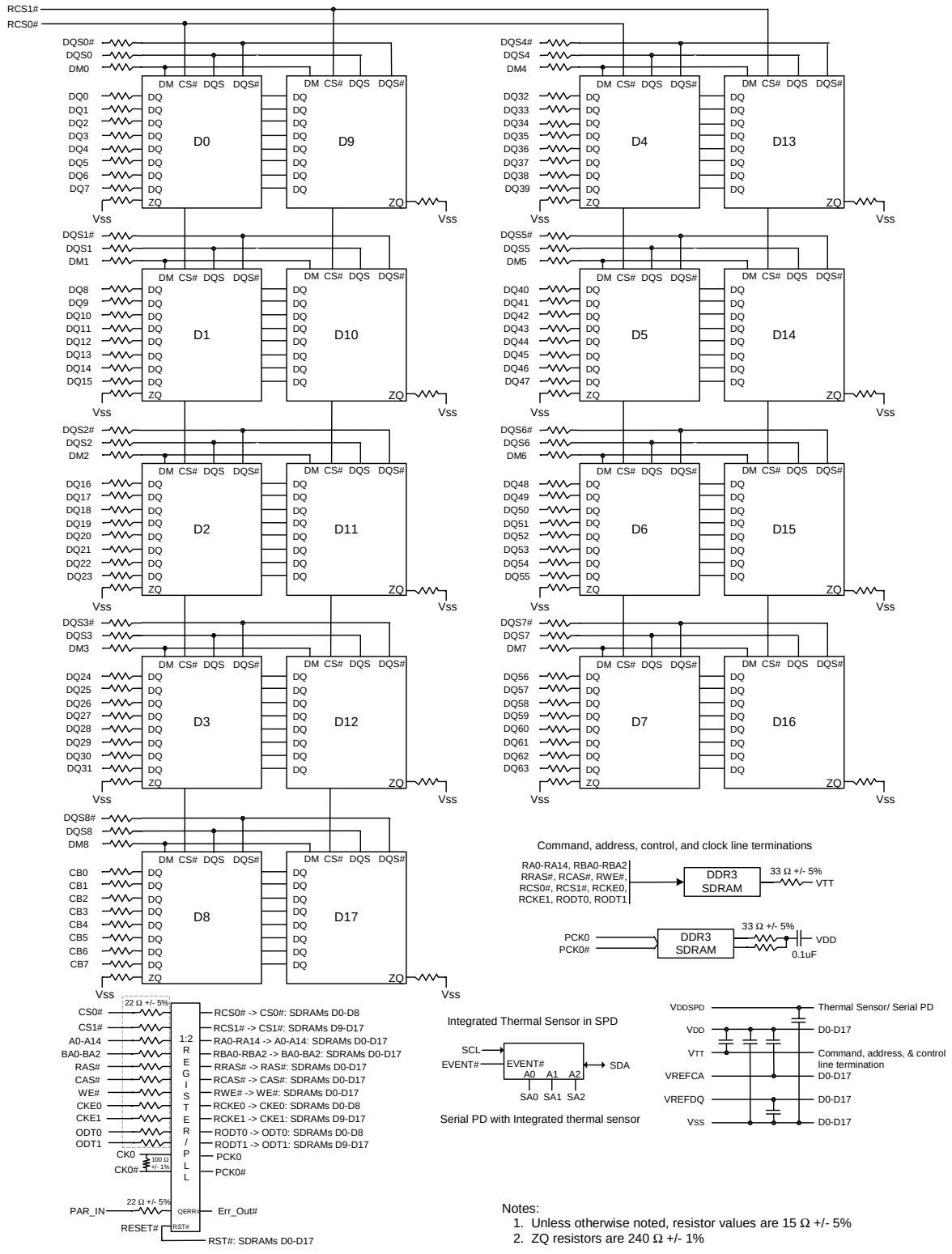
- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  K9: PC3-10600 @ CL9
  F8: PC3-8500 @ CL7
  E7: PC3-6400 @ CL6
- VL : Lead-free/RoHS

Pin Configuration

244-PIN DDR3 Mini-RDIMM FRONT								244-PIN DDR3 Mini-RDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VTT	31	DQ24	62	A2	92	DQ40	123	VTT	153	DQ29	184	A1	214	DQ45
2	VREFDQ	32	DQ25	63	VDD	93	DQ41	124	VSS	154	VSS	185	VDD	215	VSS
3	VSS	33	VSS	64	CK1*	94	VSS	125	DQ4	155	DM3/DQS12/ TDQS12	186	CK0	216	DM5/DQS14/ TDQS14
4	DQ0	34	DQS3#	65	CK1#*	95	DQS5#	126	DQ5	156	NC/DQS12#/ TDQS12#	187	CK0#	217	NC/DQS14#/ TDQS14#
5	DQ1	35	DQS3	KEY		96	DQS5	127	VSS	157	VSS	KEY		218	VSS
6	VSS	36	VSS	66	VDD	97	VSS	128	DM0/DQS9/ TDQS9	158	DQ30	188	VDD	219	DQ46
7	DQS0#	37	DQ26	67	VREFCA	98	DQ42	129	NC/DQS9#/ TDQS9#	159	DQ31	189	VDD	220	DQ47
8	DQS0	38	DQ27	68	VDD	99	DQ43	130	VSS	160	VSS	190	EVENT#	221	VSS
9	VSS	39	VSS	69	PAR_IN	100	VSS	131	DQ6	161	CB4	191	A0	222	DQ52
10	DQ2	40	CB0	70	VDD	101	DQ48	132	DQ7	162	CB5	192	VDD	223	DQ53
11	DQ3	41	CB1	71	A10/AP	102	DQ49	133	VSS	163	VSS	193	BA1	224	VSS
12	VSS	42	VSS	72	BA0	103	VSS	134	DQ12	164	DM8/DQS17/ TDQS17	194	VDD	225	DM6/DQS15/ TDQS15
13	DQ8	43	DQS8#	73	VDD	104	DQS6#	135	DQ13	165	NC/DQS17#/ TDQS17#	195	RAS#	226	NC/DQS15#/ TDQS15#
14	DQ9	44	DQS8	74	WE#	105	DQS6	136	VSS	166	VSS	196	CS0#	227	VSS
15	VSS	45	VSS	75	CAS#	106	VSS	137	DM1/DQS10/ TDQS10	167	CB6	197	VDD	228	DQ54
16	DQS1#	46	CB2	76	VDD	107	DQ50	138	NC/DQS10#/ TDQS10#	168	CB7	198	ODT0	229	DQ55
17	DQS1	47	CB3	77	CS1#	108	DQ51	139	VSS	169	VSS	199	A13	230	VSS
18	VSS	48	VSS	78	ODT1	109	VSS	140	DQ14	170	NC	200	VDD	231	DQ60
19	DQ10	49	NC	79	VDD	110	DQ56	141	DQ15	171	NC/TEST	201	NC/CS3#	232	DQ61
20	DQ11	50	RESET#	80	NC/CS2#	111	DQ57	142	VSS	172	CKE1	202	NC	233	VSS
21	VSS	51	CKE0	81	NC	112	VSS	143	DQ20	173	VDD	203	VSS	234	DM7/DQS16/ TDQS16
22	DQ16	52	VDD	82	VSS	113	DQS7#	144	DQ21	174	NC/A15	204	DQ36	235	NC/DQS16#/ TDQS16#
23	DQ17	53	BA2	83	DQ32	114	DQS7	145	VSS	175	A14	205	DQ37	236	VSS
24	VSS	54	Err_Out#/ NC	84	DQ33	115	VSS	146	DM2/DQS11/ TDQS11	176	VDD	206	VSS	237	DQ62
25	DQS2#	55	VDD	85	VSS	116	DQ58	147	NC/DQS11#/ TDQS11#	177	A12/BC#	207	DM4/DQS13/ TDQS13	238	DQ63
26	DQS2	56	A11	86	DQS4#	117	DQ59	148	VSS	178	A9	208	NC/DQS13#/ TDQS13#	239	VSS
27	VSS	57	A7	87	DQS4	118	VSS	149	DQ22	179	VDD	209	VSS	240	VDDSPD
28	DQ18	58	VDD	88	VSS	119	SA0	150	DQ23	180	A8	210	DQ38	241	SA1
29	DQ19	59	A5	89	DQ34	120	SCL	151	VSS	181	A6	211	DQ39	242	SDA
30	VSS	60	A4	90	DQ35	121	SA2	152	DQ28	182	VDD	212	VSS	243	VSS
		61	VDD	91	VSS	122	VTT			183	A3	213	DQ44	244	VTT

Note:
1. NC: No Connect.
2. * These pins are not used in this module.

Functional Block Diagram



Notes:
1. Unless otherwise noted, resistor values are 15 Ω +/- 5%
2. ZQ resistors are 240 Ω +/- 1%

Absolute Maximum Ratings

Symbol	Parameter		MIN	MAX	Unit
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}		-0.4	1.975	V
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}		-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.4	1.975	V
T_{STG}	Storage temperature		-55	100	^{0}C
I_L	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE, ODT, BA	-5	5	uA
		CK, CK#	-5	5	uA
		DM	-4	4	uA
I_{OZ}	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-10	10	uA
I_{VREF}	VREF leakage current; VREF = Valid VREF level		-18	18	uA

DC Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	VDD	1.425	1.5	1.575	V	1,2
Supply Voltage for Output	VDDQ	1.425	1.5	1.575	V	1,2
I/O Reference voltage (DQ)	VREFDQ (DC)	0.49 x VDDQ	0.5 x VDD	0.51 x VDDQ	V	3,4
I/O Reference voltage (CMD/ADD)	VREFCA (DC)	0.49 x VDDQ	0.5 x VDD	0.51 x VDDQ	V	3,4
Termination Reference Voltage	VTT	-0.483 x VDD	0.5 x VDD	+0.517 x VDD	V	5

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD and VDDQ tied together.
3. The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/- 1% VDD.
4. For reference: approximate VDD/2 +/- 15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition

Parameter	Symbol	Rating	Units	Notes
Operating temperature	T_{OPER}	0 - 95	^{0}C	1,2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD5-2
2. At 0 - 85^{0}C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85^{0}C < T_{OPER} <= 95^{0}C

Input DC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Command and Address				
Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHCA(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILCA(DC)	VSS	VREF - 0.100	V
DQ and DM				
Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHDQ(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILDQ(DC)	VSS	VREF - 0.100	V

Input AC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Command and Address				
AC Input High (Logic 1) Voltage DDR3-800/1066/1333	VIHCA(AC)	VREF + 0.175	-	V
AC Input Low (Logic 0) Voltage DDR3-800/1066/1333	VILCA(AC)	-	VREF - 0.175	V
DQ and DM				
AC Input High (Logic 1) Voltage DDR3-800/1066	VIHDQ(AC)	VREF + 0.175	-	V
AC Input Low (Logic 0) Voltage DDR3-800/1066	VILDQ(AC)	-	VREF - 0.175	V
AC Input High (Logic 1) Voltage DDR3-1333	VIHDQ(AC)	VREF + 0.150	-	V
AC Input Low (Logic 0) Voltage DDR3-1333	VILDQ(AC)	-	VREF - 0.150	V

Input/Output Capacitance

TA=25^{0}C, f=100MHz

Parameter	Symbol	DDR3-800/1066		DDR3-1333		Unit
		Min	Max	Min	Max	
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	5.5	6.5	5.5	6.5	pF
Input capacitance (CKE0, CKE1), (ODT0, ODT1), (CS0#, CS1#)	CIN2	5.5	6.5	5.5	6.5	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	7	10/9.4	7	9	pF

IDD Specification

Condition	Symbol	DDR3-1333 -K9	DDR3-1066 -F8	DDR3-800 -E7	Unit
Operating one bank active-precharge current; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	883	838	793	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; t_{RCD}= $t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1*	1018	973	928	mA
Precharge power-down current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F**	730	640	550	mA
	IDD2P-S**	316	316	316	mA
Precharge standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD2N**	820	820	730	mA
Precharge quiet standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	820	730	676	mA
Active power-down current; All banks open; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P**	730	730	640	mA
Active standby current; All banks open; t_{CK}= $t_{CK(IDD)}$; t_{RP}= $t_{RP(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD))}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	1180	1090	1000	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1513	1333	1153	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W*	1558	1378	1198	mA
Burst refresh current; t_{CK}=$t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	3430	3430	3430	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6**	216	216	216	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)-1}$*$t_{CK(IDD)}$; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RRD} = $t_{RRD(IDD)}$; t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7*	2728	2278	2098	mA

Note: IDD specification is based on Samsung B-die components.
* : Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode.
**: Value calculated reflects all module ranks in this operating condition.

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Clock Timing								
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)	1.5	<1.875	1.875	<2.5	2.5	3.3	ns
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Clock Period Jitter (Period)	tJIT(per)	-80	80	-90	90	-100	100	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-70	70	-80	80	-90	90	ps
Cycle to Cycle Period Jitter	tJIT(cc)	160		180		200		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	140		160		180		ps
Cumulative error across 2 cycles	tERR(2per)	-118	118	-132	132	-147	147	ps
Cumulative error across 3 cycles	tERR(3per)	-140	140	-157	157	-175	175	ps
Cumulative error across 4 cycles	tERR(4per)	-155	155	-175	175	-194	194	ps
Cumulative error across 5 cycles	tERR(5per)	-168	168	-188	188	-209	209	ps
Cumulative error across 6 cycles	tERR(6per)	-177	177	-200	200	-222	222	ps
Cumulative error across 7 cycles	tERR(7per)	-186	186	-209	209	-232	232	ps
Cumulative error across 8 cycles	tERR(8per)	-193	193	-217	217	-241	241	ps
Cumulative error across 9 cycles	tERR(9per)	-200	200	-224	224	-249	249	ps
Cumulative error across 10 cycles	tERR(10per)	-205	205	-231	231	-257	257	ps
Cumulative error across 11 cycles	tERR(11per)	-210	210	-237	237	-263	263	ps
Cumulative error across 12 cycles	tERR(12per)	-215	215	-242	242	-269	269	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max						
Absolute clock HIGH pulse width	tCH(abs)	0.43		0.43		0.43		tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43		0.43		0.43		tCK(avg)
Data Timing								
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	125	-	150	-	200	ps
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK	tLZ(DQ)	-500	250	-600	300	-800	400	ps
DQ high-impedance time from CK, CK	tHZ(DQ)	-	250	-	300	-	400	ps
Data setup time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	-10	-	25	-	75	-	ps
Data hold time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	65	-	100	-	150	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Data Strobe Timing								
DQS, DQS READ Preamble	tRPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS differential READ Postamble	tRPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS output high time	tQSH	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS output low time	tQSL	0.4	-	0.38	-	0.38	-	tCK(avg)
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	tCK
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	tCK
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-255	255	-300	300	-400	400	ps
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-500	250	-600	300	-800	400	ps
DQS, DQS high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	250	-	300	-	400	ps
DQS, DQS differential input low pulse width	tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DQS, DQS differential input high pulse width	tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	tCK(avg)
DQS,DQS failing edge setup time to CK, CK rising edge	tDSS	0.2	-	0.2	-	0.2	-	tCK(avg)
DQS,DQS failing edge hold time to CK, CK rising edge	tDSH	0.2	-	0.2	-	0.2	-	tCK(avg)
Command and Address Timing								
DLL locking time	tDLLK	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	4	-	tCK(avg)
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	max (12tCK,15ns)	-	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)			WR + roundup (tRP / tCK(AVG))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	36	70,000	37.5	70,000	37.5	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	max (4tCK,10ns)	-	max (4tCK,10ns)	-	
Four activate window for 1KB page size	tFAW	30	-	37.5	-	40	-	ns
Four activate window for 2KB page size	tFAW	45	-	50	-	50	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	65	-	125	-	200	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	140	-	200	-	275	-	ps

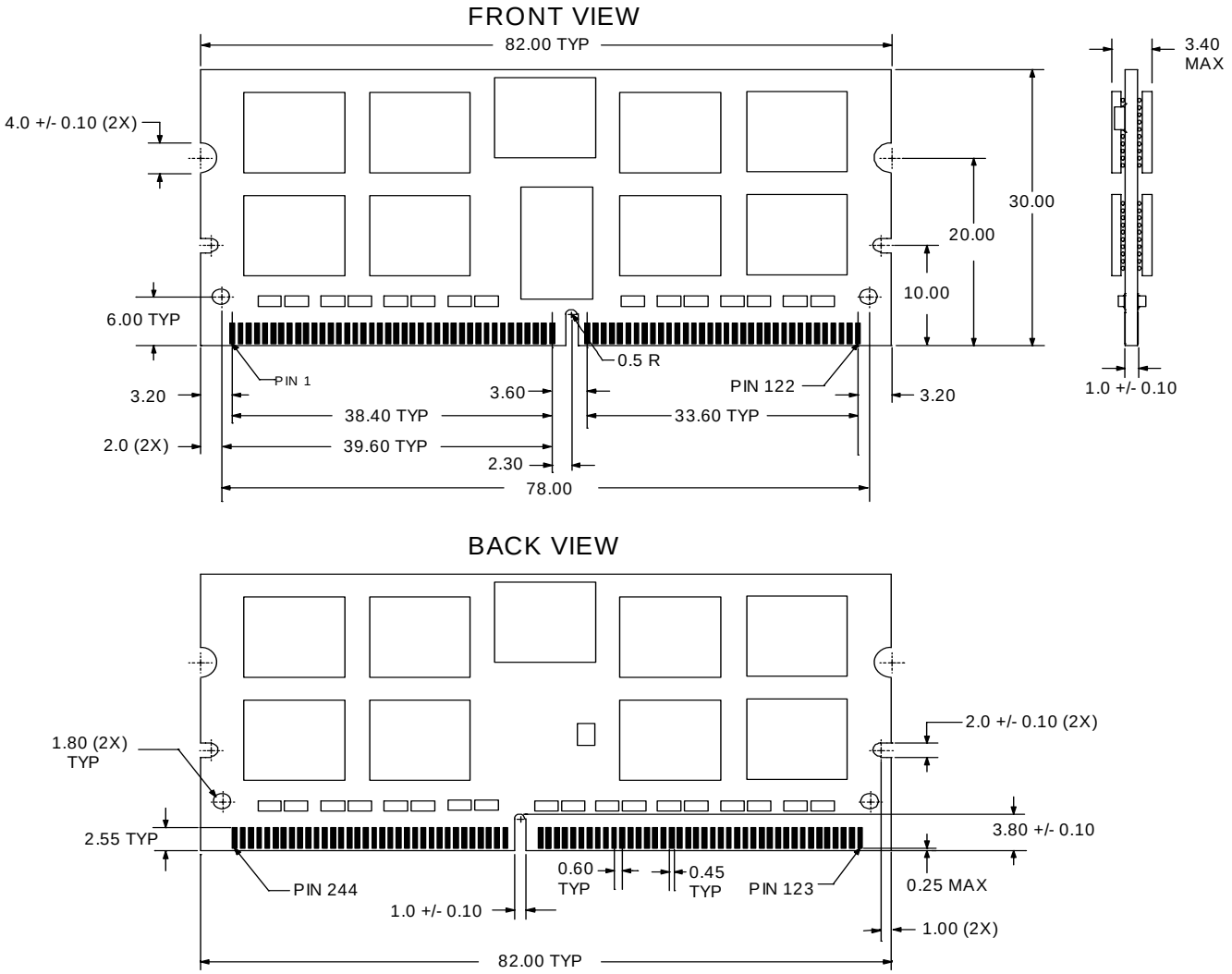
AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Refresh Timing								
2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	160	-	160	-	160	-	ns
Average periodic refresh interval (0℃<= TC ASE <= 85 ℃)	tREFI	7.8		7.8		7.8		us
Average periodic refresh interval (85℃<= TCASE <= 95 ℃)	tREFI	3.9		3.9		3.9		us
Calibration Timing								
Power-up and RESET calibration time	tZQinitI	512	-	512	-	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	256	-	256	-	tCK
Normal operation Short calibration time	tZQCS	64	-	64	-	64	-	tCK
Reset Timing								
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	
Self Refresh Timing								
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tRFC + 10ns)	-	max(5tCK,tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK,10ns)	-	max(5tCK,10ns)	-	max(5tCK,10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK,10ns)	-	max(5tCK,10ns)	-	max(5tCK,10ns)	-	
Power Down Timing								
Exit Power Down with DLL to any valid command;Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	max (3tCK,7.5ns)	-	max (3tCK,7.5ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10tCK,24ns)	-	max (10tCK,24ns)	-	max (10tCK,24ns)	-	
CKE minimum pulse width	tCKE	max (3tCK,5.625ns)	-	max (3tCK,5.625ns)	-	max (3tCK,7.5ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	1	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR3-1333 (-K9)		DDR3-1066 (-F8)		DDR3-800 (-E7)		Unit
		MIN	MAX	MIN	MAX	MIN	MAX	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK)	-	WL + 4 +(tWR/ tCK)	-	WL + 4 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK)	-	WL + 2 +(tWR/ tCK)	-	WL + 2 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tCK
ODT Timing								
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	nCK
Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	1	9	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	1	9	ns
ODT turn-on	tAON	-250	250	-300	300	-400	400	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing								
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	195	-	245	-	325	-	ps
Hold time for tDQSS latch	tWLH	195	-	245	-	325	-	ps
Write leveling output delay	tWLO	0	9	0	9	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	ns

Package Dimensions



Note: 1. All dimension are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
02/26/09	0.01	All	Preliminary
04/16/09	0.02	4	Operating Temperature Condition update
02/19/10	1.0	11	Update Dimension Package Final release