Product Specifications

PART NO: **VL43B2863A-H0S-G9S-K9S** | **REV: 1.0**

General Information

1GB 128MX72 DDR3 SDRAM ECC 204 PIN SO-RDIMM

Description: The VL43B2863A is a 128M X 72 DDR3 SDRAM high density SO-RDIMM. This memory module consists of nine CMOS 128Mx8 bit with 8 banks DDR3 Synchronous DRAMs in BGA packages, a 28-bit registered buffer/ PLL clock in BGA package, and a 2K EEPROM in 8-pin MLF package. This module is a 204-pin Dual In-line Memory Module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR3 SDRAM.

Features:

. 204-pin, dual in-line memory module (SO-RDIMM)
. JEDEC pin-out
. Fast data transfer rate: PC3-12800, PC3-10600
. VDD = VDDQ = 1.5V +/- 0.075V
. VDDSPD = 3V to 3.6V
. JEDEC standard 1.5V +/- 0.075V I/O (SSTL_15 compatible)
. 8 Banks
. 8-bit pre-fetch architecture
. Bi-directional Differential Data-Strobe
. Programmable CAS# Latency: 8, 9
. Programmable Burst ; length (8)
. On-die termination (ODT)
. Average Refresh Period 7.8 us
. Serial presence detect (SPD) with EEPROM
. Asynchronous Reset
. Fly-by topology
. Terminated command, address, and control bus
. Gold edge PCB
. Lead-free, RoHS compliant
. PCB: **Height 30mm (1.181")**, double sided components

Order Information:

VL43B2863A-H0 S X

- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  H0: PC3-12800 @ CL9
  G9: PC3-10600 @ CL8
  K9: PC3-10600 @ CL9
- VL : Lead-free/RoHS

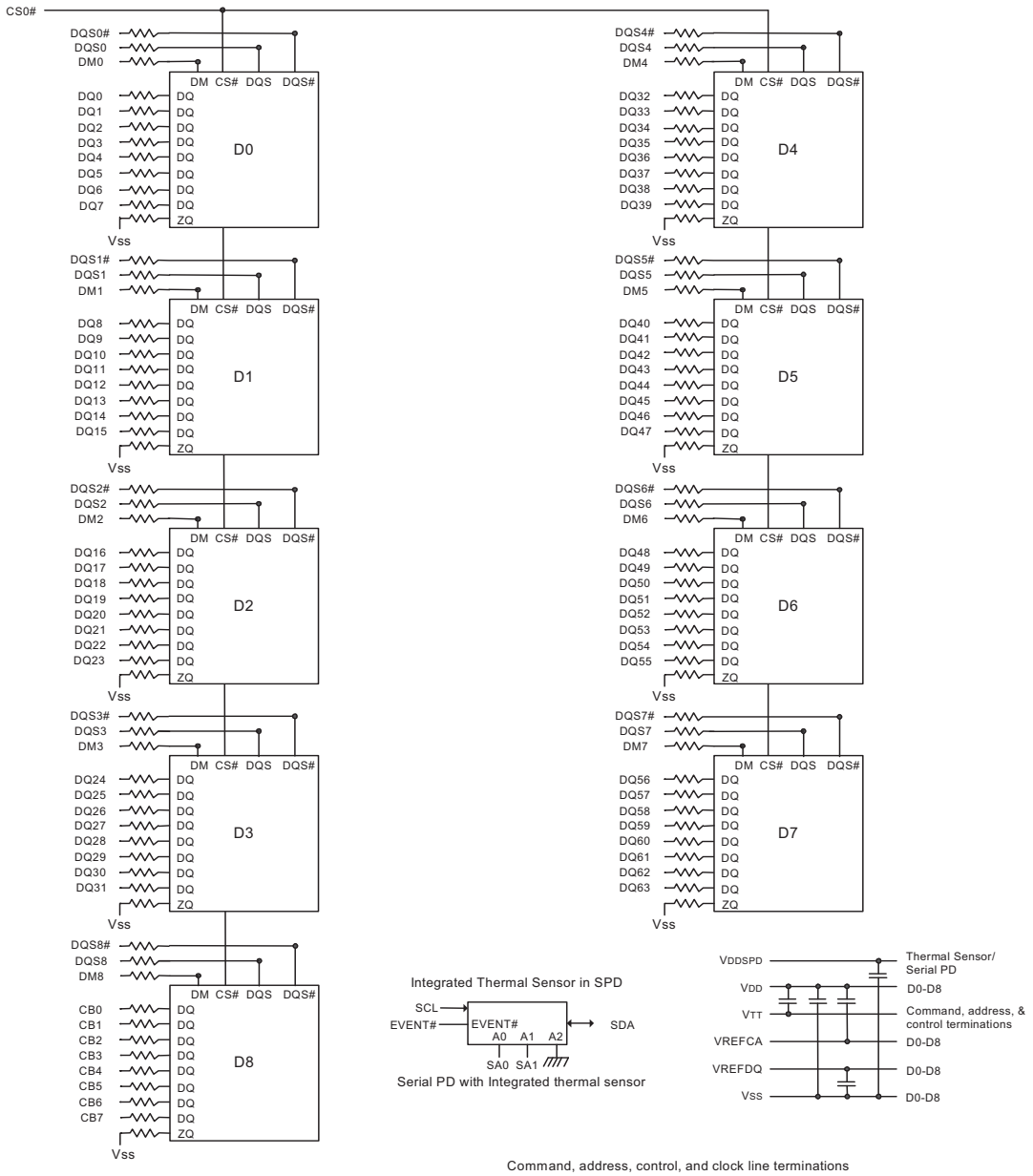
Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Inputs/ Auto Precharge
A12/BC#	Address Input/ Burst Chop
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
ODT0	On-die Termination Control
CK0,CK0#	Clock Input
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply 1.5V +/- 0.075V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
DM0~DM8	Data Masks
CB0~CB7	Data check bits I/O
VREFCA	Reference Voltage for CA
VREFDQ	Reference Voltage for DQ
VDDSPD	SPD Voltage supply 3V to 3.6V
VTT	Termination Voltage
RESET#	Register and SDRAM control
EVENT#	Reserved for Temp Sensing
NC	No Connect

Pin Configuration

204-PIN DDR3 SO-RDIMM FRONT								204-PIN DDR3 SO-RDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREFDQ	53	VSS	105	A1	157	DM5	2	VSS	54	DQ28	106	A2	158	VSS
3	VSS	55	DQ24	107	A0	159	DQ42	4	DQ4	56	DQ29	108	BA1	160	DQ46
5	DQ0	57	DQ25	109	VDD	161	DQ43	6	DQ5	58	VSS	110	VDD	162	DQ47
7	DQ1	59	DM3	111	CK0	163	VSS	8	VSS	60	DQS3#	112	ParIn/NC/ CK1	164	VSS
9	VSS	61	VSS	113	CK0#	165	DQ48	10	DQS0#	62	DQS3	114	ErrOut/NC/ CK1#	166	DQ52
11	DM0	63	DQ26	115	VDD	167	DQ49	12	DQS0	64	VSS	116	VDD	168	DQ53
13	DQ2	65	DQ27	117	A10/AP	169	VSS	14	VSS	66	DQ30	118	NC/CS3#	170	VSS
15	DQ3	67	VSS	119	BA0	171	DQS6#	16	DQ6	68	DQ31	120	NC/CS2#	172	DM6
17	VSS	69	CB0	121	WE#	173	DQS6	18	DQ7	70	VSS	122	RAS#	174	DQ54
19	DQ8	71	CB1	123	VDD	175	VSS	20	VSS	72	CB4	124	VDD	176	DQ55
21	DQ9	73	VSS	125	CAS#	177	DQ50	22	DQ12	74	CB5	126	ODT0	178	VSS
23	VSS	75	DQS8#	127	CS0#	179	DQ51	24	DQ13	76	DM8	128	NC/ODT1	180	DQ60
25	DQS1#	77	DQS8	129	NC/CS1#	181	VSS	26	VSS	78	VSS	130	A13	182	DQ61
27	DQS1	79	VSS	131	VDD	183	DQ56	28	DM1	80	CB6	132	VDD	184	VSS
29	VSS	81	CB2	133	DQ32	185	DQ57	30	RESET#	82	CB7	134	DQ36	186	DQS7#
31	DQ10	83	CB3	135	DQ33	187	VSS	32	VSS	84	VREFCA	136	DQ37	188	DQS7
33	DQ11	85	VDD	137	VSS	189	DM7	34	DQ14	86	VDD	138	VSS	190	VSS
35	VSS	87	CKE0	139	DQS4#	191	DQ58	36	DQ15	88	A15*	140	DM4	192	DQ62
37	DQ16	89	NC/CKE1#	141	DQS4	193	DQ59	38	VSS	90	A14*	142	DQ38	194	DQ63
39	DQ17	91	BA2	143	VSS	195	VSS	40	DQ20	92	A9	144	DQ39	196	VSS
41	VSS	93	VDD	145	DQ34	197	SA0	42	DQ21	94	VDD	146	VSS	198	EVENT#
43	DQS2#	95	A12/BC#	147	DQ35	199	VDDSPD	44	DM2	96	A11	148	DQ44	200	SDA
45	DQS2	97	A8	149	VSS	201	SA1	46	VSS	98	A7	150	DQ45	202	SCL
47	VSS	99	A5	151	DQ40	203	VTT	48	DQ22	100	A6	152	VSS	204	VTT
49	DQ18	101	VDD	153	DQ41			50	DQ23	102	VDD	154	DQS5#		
51	DQ19	103	A3	155	VSS			52	VSS	104	A4	156	DQS5		

Notes:
* These pins are not used in this module.
CS2#, CS3# (pin 120, 118) are used for a 4 rank module.

Functional Block Diagram



Notes:
1. Unless otherwise noted, resistor values are 15 Ω +/- 5%
2. ZQ resistors are 240 Ω +/- 1%

Absolute Maximum Ratings

Symbol	Parameter		MIN	MAX	Unit
V_{DD}	Voltage on V_{DD} pin relative to V_{SS}		-0.4	1.975	V
V_{DDQ}	Voltage on V_{DDQ} pin relative to V_{SS}		-0.4	1.975	V
V_{IN}, V_{OUT}	Voltage on any pin relative to V_{SS}		-0.4	1.975	V
T_{STG}	Storage temperature		-55	100	^{0}C
I_L	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, RAS#, CAS#, WE#, CS#, CKE, ODT, BA	-5	5	uA
		CK, CK#	-5	5	uA
		DM	-2	2	uA
I_{OZ}	Ouput leakage current; 0V<VOUT<VDDQ; DQs and ODT are disable	DQ, DQS, DQS#	-5	5	uA
I_{VREF}	VREF leakage current; VREF = Valid VREF level		-9	9	uA

DC Operating Conditions

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	VDD	1.425	1.5	1.575	V	1,2
Supply Voltage for Output	VDDQ	1.425	1.5	1.575	V	1,2
I/O Reference voltage (DQ)	VREFDQ (DC)	0.49 x VDDQ	0.5 x VDD	0.51 x VDDQ	V	3,4
I/O Reference voltage (CMD/ADD)	VREFCA (DC)	0.49 x VDDQ	0.5 x VDD	0.51 x VDDQ	V	3,4
Termination Reference Voltage	VTT	-0.483 x VDD	0.5 x VDD	+0.517 x VDD	V	5

Notes: 1. Under all conditions VDDQ must be less than or equal to VDD.
2. VDDQ tracks with VDD. AC parameters are measured with VDD andVDDQ tied together.
3. The ac peak noise on VREF may not allow VREF to deviate from VREF(DC) by more than +/- 1% VDD.
4. For reference: approximate VDD/2 +/- 15mV.
5. VTT termination voltage in excess of stated limit will adversely affect the command and address signals' voltage margin and will reduce timing margins.

Operating Temperature Condition

Parameter	Symbol	Rating	Units	Notes
Operating temperature	TOPER	0 - 85	^{0}C	1,2

Notes:
1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD5-2
2. At 0 - 85^{0}C, operation temperature range, all DRAM specification will be supported.

Input DC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Command and Address				
Input High (Logic 1) Voltage DDR3-1333/1600	VIHCA(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-1333/1600	VILCA(DC)	VSS	VREF - 0.100	V
DQ and DM				
Input High (Logic 1) Voltage DDR3-1333/1600	VIHDQ(DC)	VREF + 0.100	VDD	V
Input Low (Logic 0) Voltage DDR3-1333/1600	VILDQ(DC)	VSS	VREF - 0.100	V

Input AC Logic Level

All voltages referenced to VSS

Parameter	Symbol	Min	Max	Unit
Command and Address				
AC Input High (Logic 1) Voltage DDR3-1333/1600	VIHCA(AC)	VREF + 0.175	-	V
AC Input Low (Logic 0) Voltage DDR3-1333/1600	VILCA(AC)	-	VREF - 0.175	V
DQ and DM				
AC Input High (Logic 1) Voltage DDR3-1333/1600	VIHDQ(AC)	VREF + 0.150	-	V
AC Input Low (Logic 0) Voltage DDR3-1333/1600	VILDQ(AC)	-	VREF - 0.150	V

Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2,RAS#,CAS#,WE#)	CIN1	10.75	15.7	pF
Input capacitance (CKE0), (ODT0), (CS0#)	CIN2	10.75	15.7	pF
Input capacitance (CK0, CK0#)	CIN3	11.2	16.6	pF
Input/Output capacitance (DM0~DM8), (CB0~CB7). (DQ0~DQ63), (DQS0~DQS8, DQS0#~DQS8#)	CIO (H0)	5.5	6.3	pF
	CIO (G9, K9)	5.5	6.5	pF
Input/Output capacitance of ZQ pin	CZQ	-	31	pF

IDD Specification

Condition	Symbol	DDR3-1600	DDR3-1333		Unit
		-H0	-G9	-K9	
Operating one bank active-precharge current; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	TBD	955	955	mA
Operating one bank active-read-precharge current; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RAS}= $t_{RAS\ MIN(IDD)}$; t_{RCD}= $t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is sames as IDD4W.	IDD1	TBD	1135	1135	mA
Precharge power-down current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P-F	TBD	190	190	mA
	IDD2P-S	TBD	190	190	mA
Precharge standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are SWINGCHING; Data bus inputs are SWITCHING.	IDD2N	TBD	505	505	mA
Precharge quiet standby current; All banks idle; t_{CK}= $t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	TBD	505	505	mA
Active power-down current; All banks open; t_{CK}= $t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	IDD3P	TBD	640	640	mA
Active standby current; All banks open; t_{CK}= $t_{CK(IDD)}$; t_{RP}= $t_{RP(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	TBD	820	820	mA
Operating burst read current; All banks open; Continuous burst reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R	TBD	1990	1990	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; t_{CK}= $t_{CK(IDD)}$; t_{RAS}= $t_{RAS\ MAX(IDD)}$; t_{RP}= $t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD4W	TBD	1900	1900	mA
Burst refresh current; t_{CK}=$t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	TBD	2170	2170	mA
Self refresh current; CK and CK# at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	IDD6	TBD	90	90	mA
Operating bank interleave read current; All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)-1}$*$t_{CK(IDD)}$; t_{CK}= $t_{CK(IDD)}$; t_{RC}= $t_{RC(IDD)}$; t_{RRD} = $t_{RRD(IDD)}$; t_{RCD} = 1*$t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4R.	IDD7	TBD	2980	2980	mA
Note: IDD specification is based on Samsung D-die					

AC TIMING PARAMETERS & SPECIFICATIONS

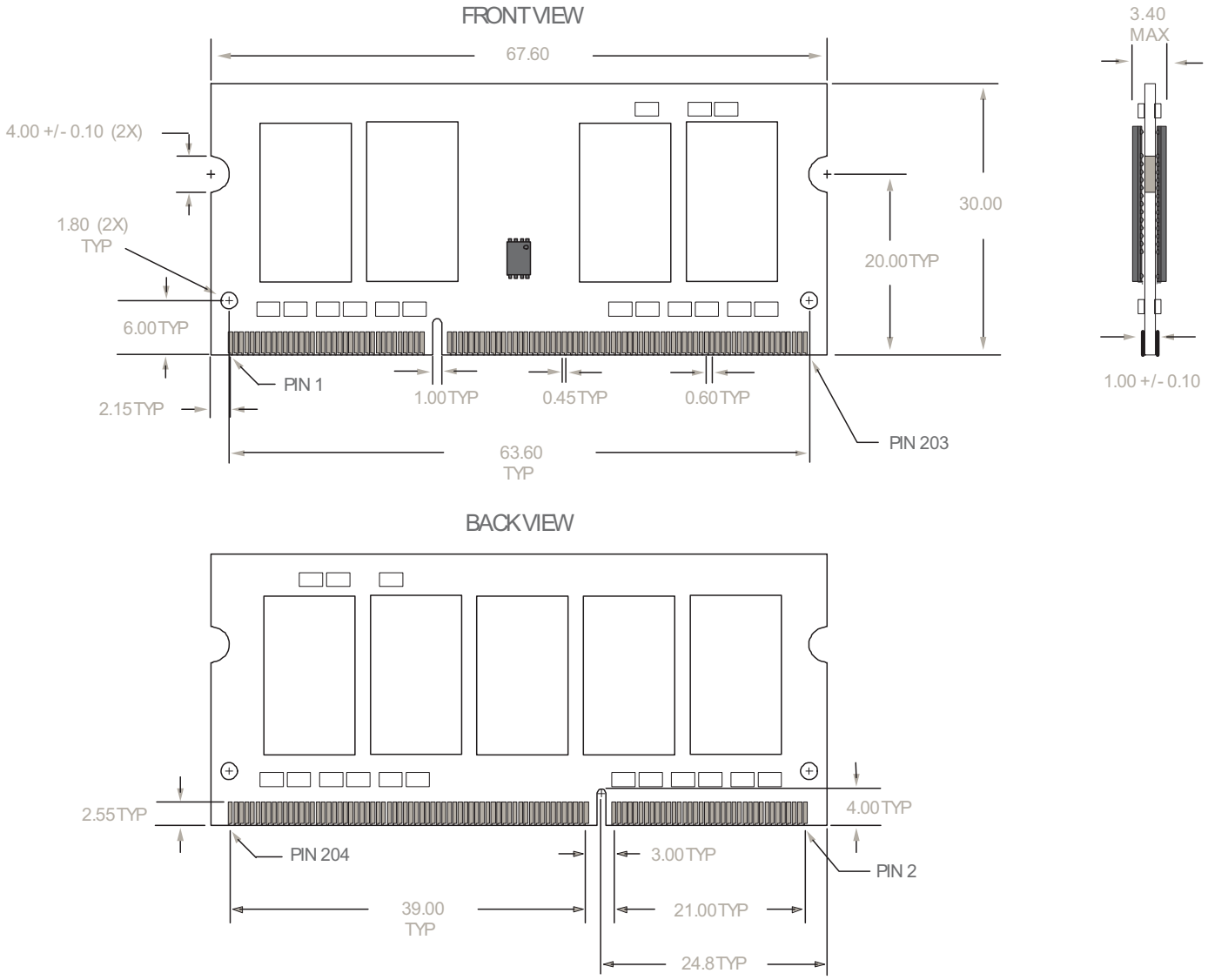
Parameter	Symbol	DDR3-1600 (-H0)		DDR3-1333 (-G9/-K9)		Unit
		MIN	MAX	MIN	MAX	
Clock Timing						
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	ns
Average Clock Period	tCK(avg)	See Speed Bins Table		See Speed Bins Table		ps
Clock Period	tCK(abs)	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	tCK(avg)min + tJIT(per)min	tCK(avg)max + tJIT(per)max	ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	tCK(avg)
Clock Period Jitter	tJIT(per)	-70	70	-80	80	ps
Clock Period Jitter during DLL locking period	tJIT(per, lck)	-60	60	-70	70	ps
Cycle to Cycle Period Jitter	tJIT(cc)	140		160		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc, lck)	120		140		ps
Cumulative error across 2 cycles	tERR(2per)	-103	103	-118	118	ps
Cumulative error across 3 cycles	tERR(3per)	-122	122	-140	140	ps
Cumulative error across 4 cycles	tERR(4per)	-136	136	-155	155	ps
Cumulative error across 5 cycles	tERR(5per)	-147	147	-168	168	ps
Cumulative error across 6 cycles	tERR(6per)	-155	155	-177	177	ps
Cumulative error across 7 cycles	tERR(7per)	-163	163	-186	186	ps
Cumulative error across 8 cycles	tERR(8per)	-169	169	-193	193	ps
Cumulative error across 9 cycles	tERR(9per)	-175	175	-200	200	ps
Cumulative error across 10 cycles	tERR(10per)	-180	180	-205	205	ps
Cumulative error across 11 cycles	tERR(11per)	-184	184	-210	210	ps
Cumulative error across 12 cycles	tERR(12per)	-188	188	-215	215	ps
Cumulative error across n = 13, 14 ... 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n))*tJIT(per)min tERR(nper)max = (1 = 0.68ln(n))*tJIT(per)max				
Absolute clock HIGH pulse width	tCH(abs)	0.43		0.43		tCK(avg)
Absolute clock Low pulse width	tCL(abs)	0.43		0.43		tCK(avg)
Data Timing						
DQS,DQS to DQ skew, per group, per access	tDQSQ	-	100	-	125	ps
DQ output hold time from DQS, DQS	tQH	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK	tLZ(DQ)	-450	225	-500	250	ps
DQ high-impedance time from CK, CK	tHZ(DQ)	-	225	-	250	ps
Data setup time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDS(base)	10	-	-10	-	ps
Data hold time to DQS, DQS referenced to Vih(ac)Vil(ac) levels	tDH(base)	45	-	65	-	ps
DQ and DM Input pulse width for each input	tDIPW	360	-	360	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS						
Parameter	**Symbol**	**DDR3-1600 (-H0)**		**DDR3-1333 (-G9/-K9)**		**Unit**
		MIN	**MAX**	**MIN**	**MAX**	
Data Strobe Timing						
DQS, DQS READ Preamble	tRPRE	0.9	-	0.9	-	tCK
DQS, DQS differential READ Postamble	tRPST	0.3	-	0.3	-	tCK
DQS, DQS output high time	tQSH	0.4	-	0.4	-	tCK(avg)
DQS, DQS output low time	tQSL	0.4	-	0.4	-	tCK(avg)
DQS, DQS WRITE Preamble	tWPRE	0.9	-	0.9	-	tCK
DQS, DQS WRITE Postamble	tWPST	0.3	-	0.3	-	tCK
DQS, DQS rising edge output access time from rising CK, CK	tDQSCK	-225	225	-255	255	ps
DQS, DQS low-impedance time (Referenced from RL-1)	tLZ(DQS)	-450	225	-500	250	ps
DQS, DQS high-impedance time (Referenced from RL+BL/ 2)	tHZ(DQS)	-	225	-	250	ps
DQS, DQS differential input low pulse width	tDQSL	0.45	0.55	0.4	0.6	tCK
DQS, DQS differential input high pulse width	tDQSH	0.45	0.55	0.4	0.6	tCK
DQS, DQS rising edge to CK, CK rising edge	tDQSS	-0.27	0.27	-0.25	0.25	tCK(avg)
DQS,DQS faling edge setup time to CK, CK rising edge	tDSS	0.18	-	0.2	-	tCK(avg)
DQS,DQS faling edge hold time to CK, CK rising edge	tDSH	0.18	-	0.2	-	tCK(avg)
Command and Address Timing						
DLL locking time	tDLLK	512	-	512	-	nCK
internal READ Command to PRECHARGE Command delay	tRTP	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
WRITE recovery time	tWR	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4	-	4	-	tCK(avg)
Mode Register Set command update delay	tMOD	max (12tCK,15ns)	-	max (12tCK,15ns)	-	
CAS# to CAS# command delay	tCCD	4	-	4	-	nCK
Auto precharge write recovery + precharge time	tDAL(min)	WR + roundup (tRP / tCK(AVG))				nCK
Multi-Purpose Register Recovery Time	tMPRR	1	-	1	-	nCK
ACTIVE to PRECHARGE command period	tRAS	35	70,000	36	70,000	ns
ACTIVE to ACTIVE command period for 1KB page size	tRRD	max (4tCK,6ns)	-	max (4tCK,6ns)	-	
ACTIVE to ACTIVE command period for 2KB page size	tRRD	max (4tCK,7.5ns)	-	max (4tCK,7.5ns)	-	
Four activate window for 1KB page size	tFAW	30	-	30	-	ns
Four activate window for 2KB page size	tFAW	40	-	45	-	ns
Command and Address setup time to CK, CK referenced to Vih(ac) / Vil(ac) levels	tIS(base)	TBD	-	65	-	ps
Command and Address hold time from CK, CK referenced to Vih(ac) / Vil(ac) levels	tIH(base)	TBD	-	140	-	ps

AC TIMING PARAMETERS & SPECIFICATIONS						
Parameter	**Symbol**	**DDR3-1600 (-H0)**		**DDR3-1333 (-G9/-K9)**		**Unit**
		MIN	**MAX**	**MIN**	**MAX**	
Command and Address setup time to CK, CK# referenced to Vih(ac) / Vil(ac) levels	tIS(base) AC150	TBD+125	-	TBD+125	-	ps
Control & Address Input pulse width for each input	tIPW	560	-	560	-	ps
Refresh Timing						
512Mb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	90	-	90	-	ns
1Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	110	-	110	-	ns
2Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	160	-	160	-	ns
4Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	300	-	300	-	ns
8Gb REFRESH to REFRESH OR REFRESH to ACTIVE command interval	tRFC	350	-	350	-	ns
Average periodic refresh interval (0°C<= TCASE <= 85 °C)	tREFI	7.8		7.8		us
Average periodic refresh interval (85°C<= TCASE <= 95 °C)	tREFI	3.9		3.9		us
Calibration Timing						
Power-up and RESET calibration time	tZQinitI	512	-	512	-	tCK
Normal operation Full calibration time	tZQoper	256	-	256	-	tCK
Normal operation short calibration time	tZQCS	64	-	64	-	tCK
Reset Timing						
Exit Reset from CKE HIGH to a valid command	tXPR	max(5tCK, tRFC + 10ns)	-	max(5tCK, tRFC + 10ns)	-	
Self Refresh Timing						
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5tCK,tR-FC + 10ns)	-	max(5tCK,tR-FC + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tCK
Minimum CKE low width for Self refresh entry to exit timing	tCKESR	tCKE(min) + 1tCK	-	tCKE(min) + 1tCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE)	tCKSRE	max(5tCK,1-0ns)	-	max(5tCK,1-0ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX)	tCKSRX	max(5tCK,1-0ns)	-	max(5tCK,1-0ns)	-	
Power Down Timing						
Exit Power Down with DLL on to any valid command;Exit Percharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max (3tCK,6ns)	-	max (3tCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max (10tCK,24ns)	-	max (10tCK,24ns)	-	
CKE minimum pulse width	tCKE	max (3tCK,5ns)	-	max (3tCK,5.625-ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	nCK

AC TIMING PARAMETERS & SPECIFICATIONS						
Parameter	**Symbol**	**DDR3-1600 (-H0)**		**DDR3-1333 (-G9/-K9)**		**Unit**
		MIN	**MAX**	**MIN**	**MAX**	
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCK
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	nCK
Timing of PRE command to Power Down entry	tPRPDEN	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL + 4 +1	-	RL + 4 +1	-	
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRPDEN	WL + 4 +(tWR/ tCK)	-	WL + 4 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BL4OTF)	tWRAPDEN	WL + 4 +WR +1	-	WL + 4 +WR +1	-	nCK
Timing of WR command to Power Down entry (BL4MRS)	tWRPDEN	WL + 2 +(tWR/ tCK)	-	WL + 2 +(tWR/ tCK)	-	nCK
Timing of WRA command to Power Down entry (BL4MRS)	tWRAPDEN	WL +2 +WR +1	-	WL +2 +WR +1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tCK
ODT Timing						
ODT high time without write command or with wirte com-mand and BC4	ODTH4	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	nCK
Asynchronous RTT tum-on delay (Power-Down with DLL frozen)	tAONPD	1	9	1	9	ns
Asynchronous RTT tum-off delay (Power-Down with DLL frozen)	tAOFPD	1	9	1	9	ns
ODT turn-on	tAON	-225	225	-250	250	ps
RTT_NOM and RTT_WR turn-off time from ODTLoff refer-ence	tAOF	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timing						
First DQS pulse rising edge after tDQSS margining mode is programmed	tWLMRD	40	-	40	-	tCK
DQS/DQS delay after tDQS margining mode is programmed	tWLDQSEN	25	-	25	-	tCK
Setup time for tDQSS latch	tWLS	TBD	-	195	-	ps
Hold time of tDQSS latch	tWLH	TBD	-	195	-	ps
Write leveling output delay	tWLO	0	7.5	0	9	ns
Write leveling output error	tWLOE	0	2	0	2	ns

Package Dimensions



Notes:

All dimensions are in millimeters with tolerance +/- 0.13mm unless otherwise specified.

Revision History:

Date	Rev.	Page	Changes
07/21/08	0.01	All	Initial draft
12/23/08	0.02	2	Updated Pinout Configuration
03/18/11	1.0	All	Spec release