Virtium Technology, Inc.

Product Specifications

PART NO:	REV:
VL366S6553-GAS/GHS/GLS	1.5

General Information

512MB 64Mx64 SDRAM PC100/PC133 UNBUFFERED 168 PIN DIMM

Description: The VL366S6553 is a 64M x 64 Synchronous Dynamic RAM high density memory module. This memory module consists of 16 CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in TSOP-II 400 mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 168-pin Dual In-line Memory Module and is intended for mounting into connector sockets. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Unbuffered 8 byte SDRAM 168pin DIMM
- High Speed - 100MHz, 133MHz , CL2, CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ±0.3 V power supply
- 13/10/4 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial Presence Detect
- Gold (Au) contacts
- Lead-free/RoHS compliant
- PCB height: **1150 (mil)**, single sided component

Pin Name	Function
A0-A12	Address inputs
BA0, BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CLK0, CLK1, CLK2, CLK3	Clock Input
CKE0, CKE1	Clock Enable Input
CS0#~CS3#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DQM0-DQM7	Data input/output mask
VDD	Power Supply (3.3V)
VSS	Ground
*VREF	Power Supply for Reference
SDA	Serial Data Input/Output
SCL	SPD Clock Input
SA0~SA2	Address in EEPROM
NC	No Connect
* These pins are not used in this module.	

Order Information:

VL366S6553-GA S X

- DRAM DIE (Option)
- DRAM MANUFACTURER
  S -SAMSUNG
- MODULE SPEED
  GA: PC133 @ CL3
  GH: PC100 @ CL2
  GL: PC100 @ CL3
- VL: Lead-free/RoHS

Pin Configuration

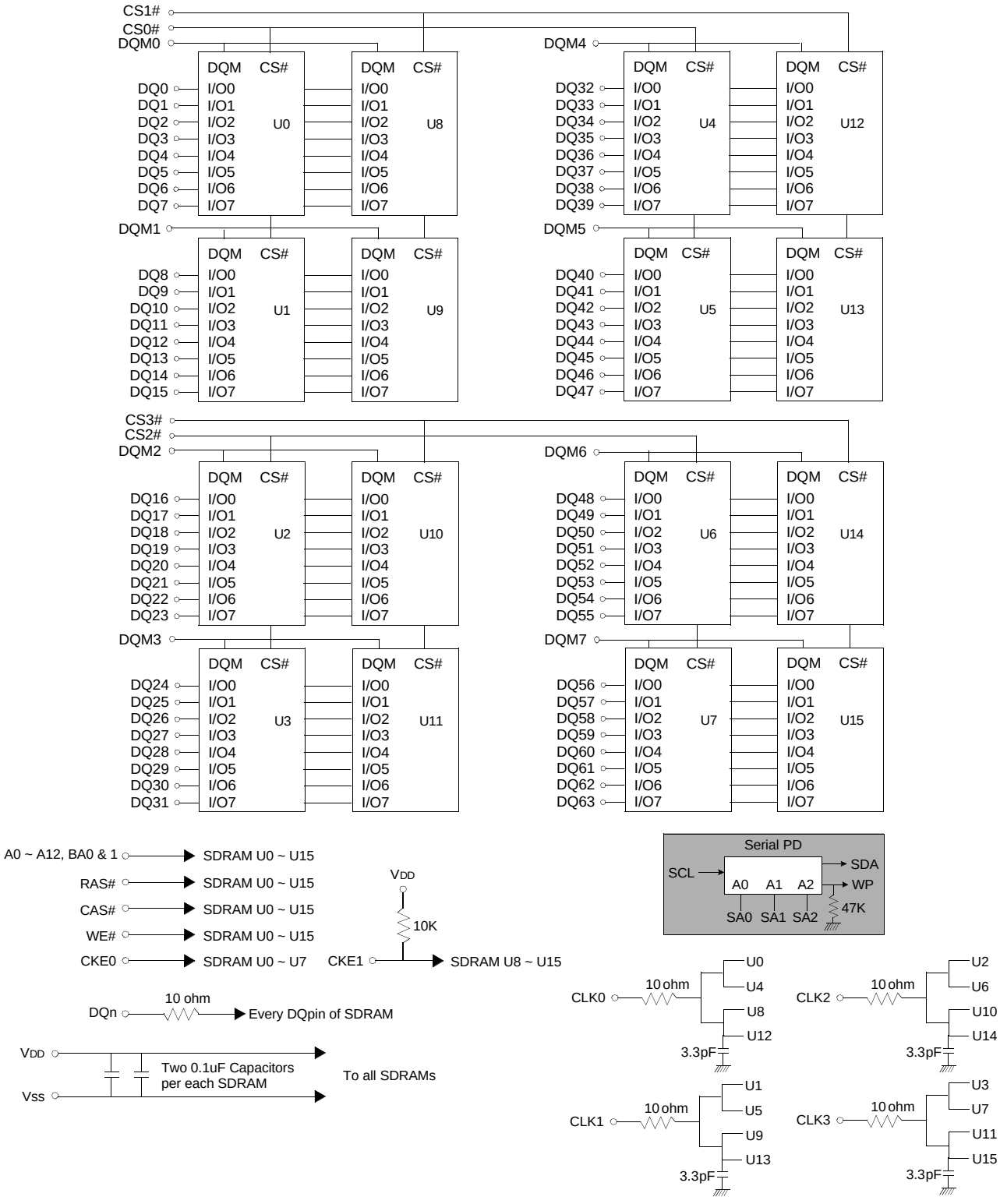
Pin Number	Front Side
1	V_{SS}
2	DQ0
3	DQ1
4	DQ2
5	DQ3
6	V_{DD}
7	DQ4
8	DQ5
9	DQ6
10	DQ7
11	DQ8
12	V_{SS}
13	DQ9
14	DQ10
15	DQ11
16	DQ12
17	DQ13
18	V_{DD}
19	DQ14
20	DQ15
21	NC
22	NC
23	V_{SS}
24	NC
25	NC
26	V_{DD}
27	WE#
28	DQM0
29	DQM1
30	CS0#
31	NC
32	V_{SS}
33	A0
34	A2
35	A4
36	A6
37	A8
38	A10/AP
39	BA1
40	V_{DD}
41	V_{DD}
42	CLK0

Pin Number	Front Side
43	V_{SS}
44	NC
45	CS2#
46	DQM2
47	DQM3
48	NC
49	V_{DD}
50	NC
51	NC
52	NC
53	NC
54	V_{SS}
55	DQ16
56	DQ17
57	DQ18
58	DQ19
59	V_{DD}
60	DQ20
61	NC
62	NC
63	CKE1
64	V_{SS}
65	DQ21
66	DQ22
67	DQ23
68	V_{SS}
69	DQ24
70	DQ25
71	DQ26
72	DQ27
73	V_{DD}
74	DQ28
75	DQ29
76	DQ30
77	DQ31
78	V_{SS}
79	CLK2
80	NC
81	WP
82	SDA
83	SCL
84	V_{DD}

Pin Number	Back Side
85	V_{SS}
86	DQ32
87	DQ33
88	DQ34
89	DQ35
90	V_{DD}
91	DQ36
92	DQ37
93	DQ38
94	DQ39
95	DQ40
96	V_{SS}
97	DQ41
98	DQ42
99	DQ43
100	DQ44
101	DQ45
102	V_{DD}
103	DQ46
104	DQ47
105	NC
106	NC
107	V_{SS}
108	NC
109	NC
110	V_{DD}
111	CAS#
112	DQM4
113	DQM5
114	CS1#
115	RAS#
116	V_{SS}
117	A1
118	A3
119	A5
120	A7
121	A9
122	BA0
123	A11
124	V_{DD}
125	CLK1
126	A12

Pin Number	Back Side
127	V_{SS}
128	CKE0
129	CS3#
130	DQM6
131	DQM7
132	NC
133	V_{DD}
134	NC
135	NC
136	NC
137	NC
138	V_{SS}
139	DQ48
140	DQ49
141	DQ50
142	DQ51
143	V_{DD}
144	DQ52
145	NC
146	NC
147	NC
148	V_{SS}
149	DQ53
150	DQ54
151	DQ55
152	V_{SS}
153	DQ56
154	DQ57
155	DQ58
156	DQ59
157	V_{DD}
158	DQ60
159	DQ61
160	DQ62
161	DQ63
162	V_{SS}
163	CLK3
164	NC
165	SA0
166	SA1
167	SA2
168	V_{DD}

Functional Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	^{0}C
Power dissipation	P_D	16	W
Short circuit current	I_{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A = 0^{0}C to +70^{0}C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD},V_{DDQ}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-10	-	10	uA	3
Input leakage current (I/O pins)	I_{IL}	-3	-	3	uA	3,4

Notes: 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is <= 3ns.
2. V_{IL} (min) = 2.0V AC. The undershoot voltage duration is <= 3ns.
3. Any input 0V <= V_{IN} <= V_{DDQ}.
4.D_{OUT} is desabled, 0V <= V_{OUT} <= V_{DDQ}.

Capacitance (T_A = 25^{0}C, f = 1MHz, V_{DD} = 3.3V)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1)	C_{IN1}	80	100	pF
Input capacitance (RAS#, CAS#, WE#)	C_{IN2}	80	100	pF
Input capacitance (CKE0, CKE1)	C_{IN3}	50	60	pF
Input capacitance (CLK0 ~ CLK3)	C_{IN4}	40	45	pF
Input capacitance (CS0# ~ CS3#)	C_{IN5}	25	35	pF
Input capacitance (DQM0 ~ DQM7)	C_{IN6}	15	20	pF
Data input/output capacitance (DQ0 ~ DQ63)	C_{OUT}	10	15	pF

DC Characteristics

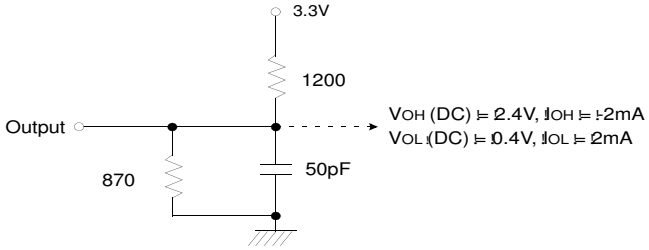
(Recommended operation condition unless otherwise noted, T_A = 0°C to +70°C)

Parameter	Symbol	Test Condion	Version			Unit	Note
			-GA	-GH	-GL		
Operating current (One bank active)	I_{CC1}	Burst length = 1 t_{RC} >= t_{RC}(min) I_{OL} = 0 mA	960	960	960	mA	1
Precharge standby current in power-down mode	I_{CC2P}	CKE <= V_{IL}(max), t_{CC} = 10ns	32			mA	
	I_{CC2PS}	CKE & CLK <=V_{IL}(max), tcc = ∞	32			mA	
Precharge standby current in non power-down mode	I_{CC2N}	CKE >= V_{IH} (min), CS# >= V_{IH} (min), t_{CC} = 10ns Input signals are changed one time during 20ns	320			mA	
	I_{CC2NS}	CKE >= V_{IH}(min), CLK <= V_{IL}(max), tcc = ∞ Input signals are stable	160			mA	
Active standby current in power-down mode	I_{CC3P}	CKE <= V_{IL}(max), tcc = 10ns	96			mA	
	I_{CC3PS}	CKE & CLK <= V_{IL}(max), tcc = ∞	96			mA	
Active standby current in non power-down mode (One bank active)	I_{CC3N}	CKE >= V_{IH}(min), CS# >= V_{IH}(min), tcc = 10ns Input signals are changed one time during 20ns	480			mA	
	I_{CC3NS}	CKE >= V_{IH}(min), CLK <= V_{IL} (max), tcc = ∞ Input signals are stable	400			mA	
Operating current (Burst mode)	I_{CC4}	I_{OL} = 0 mA Page burst 2 Banks actived t_{CCD} = 2CLKs	1120	1040	1040	mA	1
Refresh current	I_{CC5}	t_{RC} >= t_{RC}(min)	1840	1760	1760	mA	2
Self refresh current	I_{CC6}	CKE <= 0.2V	48			mA	

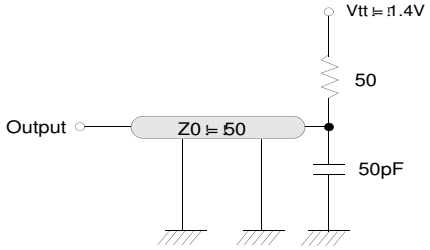
Note: 1. Measured with outputs open.
2.Refresh period is 64ms.

AC Operating Test Conditions (VDD = 3.3V, TA = 0°C to +70°C)

Parameter	Value	Unit
AC input levels (V_{IH}/V_{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Operating AC Parameter

Parameter		Symbol	Version			Unit	Note
			-GA	-GH	-GL		
Row active to row active delay		t_{RRD}(min)	15	20	20	ns	1
RAS# to CAS# delay		t_{RCD}(min)	20	20	20	ns	1
Row precharge time		t_{RP}(min)	20	20	20	ns	1
Row active time		t_{RAS}(min)	45	50	50	ns	1
		t_{RAS}(max)	100			us	
Row cycle time		t_{RC}(min)	65	70	70	ns	1
Last data in to row precharge		t_{RDL}(min)	2			CLK	2
Last data in to Active delay		t_{DAL}(min)	2 CLK + tRP			-	
Last data in to new col. addrees delay		t_{CDL}(min)	1			CLK	1
Last data in to burst stop		t_{BDL}(min)	1			CLK	2
Col. address to col. address delay		t_{CCD}(min)	1			CLK	2
Number of valid output data	CAS Latency = 3		2			CLK	3
	CAS Latency = 2		1			ea	4

Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

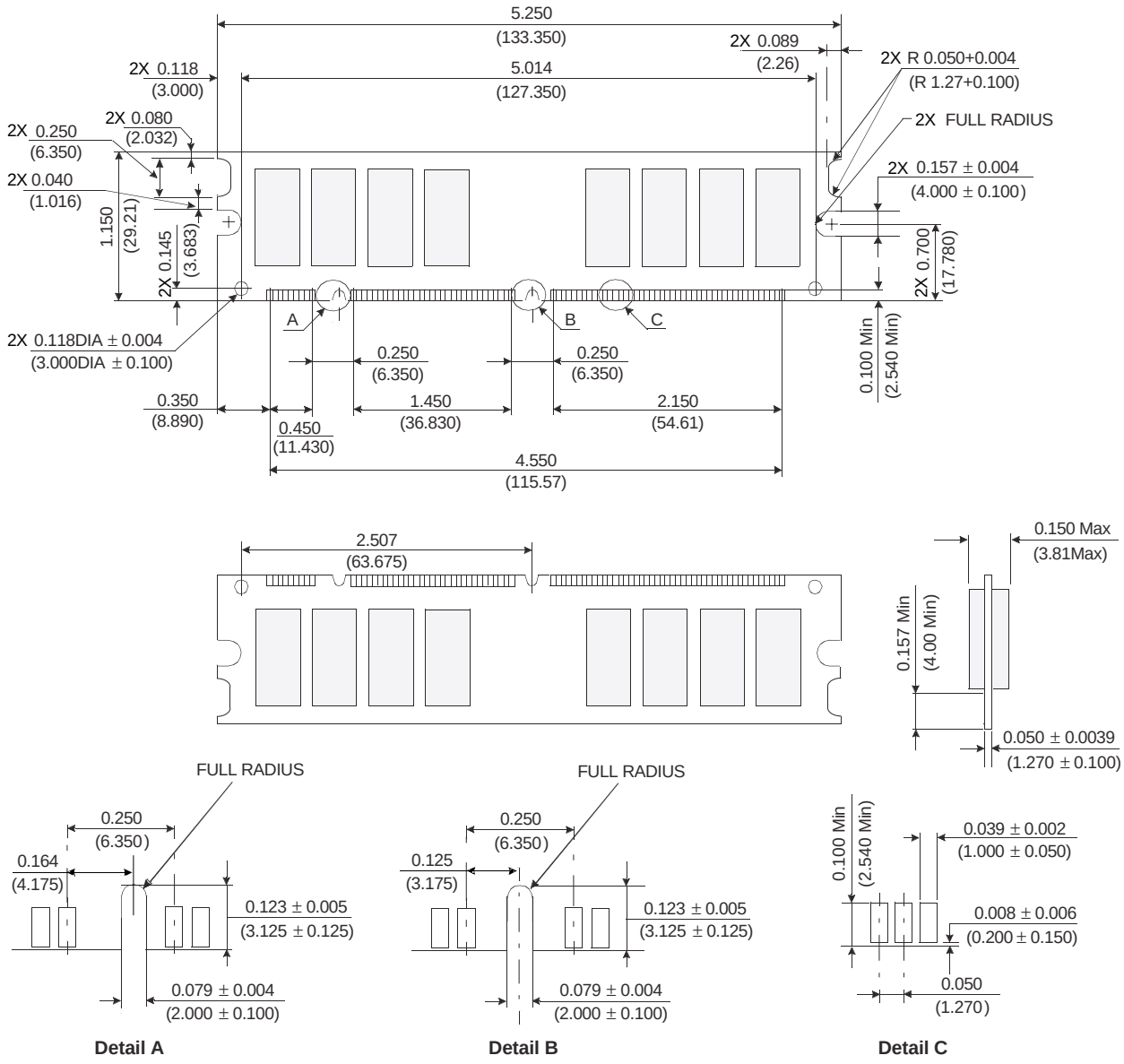
Operating AC Parameter

Parameter		Symbol	-GA		-GH		-GL		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency = 3	tCC	7.5	1000	-	1000	10	1000	ns	1
	CAS latency = 2		-		10		-			
CLK to valid output delay	CAS latency = 3	tSAC		5.4		-		6	ns	1,2
	CAS latency = 2			-		6		-		
Output data hold time	CAS latency = 3	tOH	3		-		3		ns	2
	CAS latency = 2		-		3		-			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	1.5		2		2		ns	3
Input hold time		tSH	0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-z	CAS latency = 3	tSHZ		5.4		-		6	ns	
	CAS latency = 2			-		6		-		

Notes: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
if tr & tf is longer than 1ns, transient timecompensation should be considered,
i.e. ,[(tr + tf)/2-1]ns should be added to the parameter.

Package Dimensions

Units : Inches (Millimeters)



Detail A **Detail B** **Detail C**

Tolerances : ± .005(.13) unless otherwise specified

Revision History:

Date	Rev.	Page	Changes
09/23/2010	1.5	All	Update datasheet