Virtium Technology, Inc.	Product Specification	
	1GB 128MX64 SDRAM PC100/PC133 SODIMM	Rev: 1.1

General Information

VL466S2853CC-GA/GH/GL

1GB 128Mx64 SDRAM PC100/PC133 SODIMM WITH CONFORMAL COATING

Description: The VL466S2853CC is a 128M x 64 Synchronous Dynamic RAM high density memory module. This memory module consists of thirty-two CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in TSOP-II package and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin stacked PCB Dual-In line-Memory Module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Unbuffered 8 byte SDRAM 144pin SODIMM
- High Speed - 100MHz/133MHz CL2/CL3
- Burst Mode Operation
- Auto & Self refresh Capability (4096 Cycles/64ms)
- LVTTL compatible inputs and outputs
- Single 3.3V ±0.3 V power supply
- 13/10/2 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial Presence Detect
- Gold (Au) contacts
- Stacked PCB 1.150”
- Conformal coating

Pin Name	Function
A0-A12	Address inputs
BA0, BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CLK0	Clock Input
CKE0 ~ CKE3	Clock Enable Input
CS0# ~ CS3#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DM0-DM7	Data Mask
VDD	Power Supply
VSS	Ground
*VREF	Power Supply for Reference
SDA	Serial Data Input/Output
SCL	SPD Clock Input
NC	No Connect
* These pins are not used in this module.	

Order Information:

VL466S2853CC-GA S X

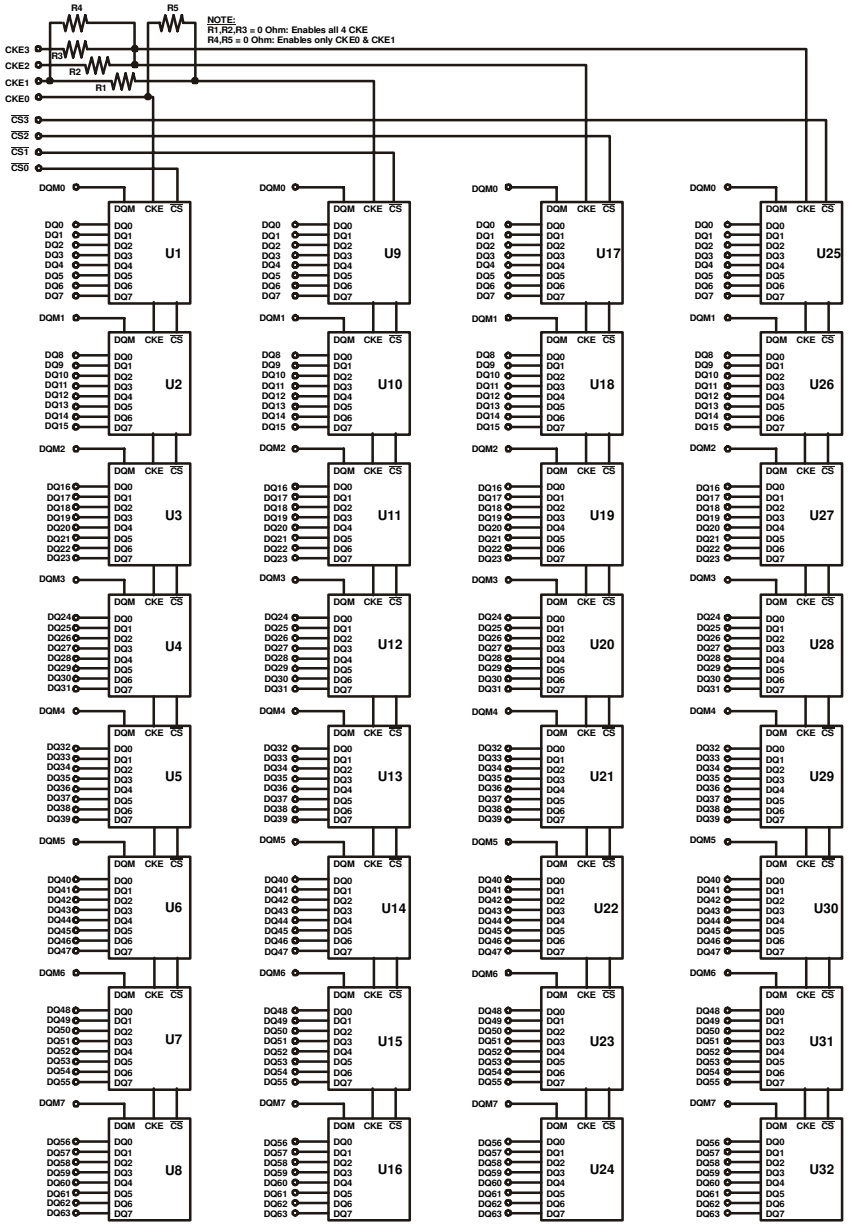
- DRAM DIE (Option)
- DRAM MANUFACTURER
  S -SAMSUNG
- MODULE SPEED
  GA: PC133 @ CL3
  GH: PC100 @ CL2
  GL: PC100 @ CL3
- CC: Conformal coating
- VL: Lead-free/RoHS

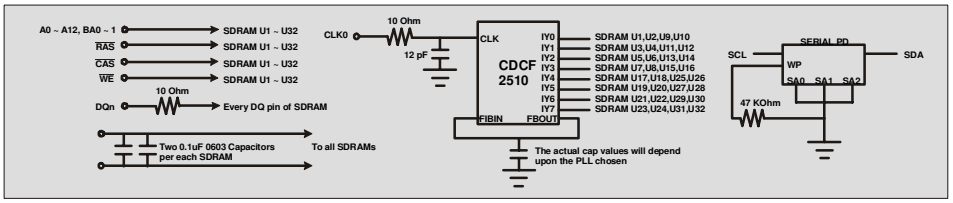
Pin Configuration

Pin Number	Front Side	Pin Number	Back Side	Pin Number	Front Side	Pin Number	Back Side
1	VSS	2	VSS	73	DU	74	*CLK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	CS2#	78	CKE2
7	DQ2	8	DQ34	79	CS3#	80	CKE3
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95`	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10/AP	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	VDD	46	VDD	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	CS0#	70	A12	141	SDA	142	SCL
71	CS1#	72	NC	143	VDD	144	VDD

* These pins are not used in this module.

Functional Block Diagram





Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-1.0 ~ 4.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}, V_{DDQ}	-1.0 ~ 4.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	32	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (T_A= 0℃ to +70℃)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	V_{DD}	3.0	3.3	3.6	V	
Input high voltage	V_{IH}	2.0	3.0	V_{DDQ}+0.3	V	1
Input low voltage	V_{IL}	-0.3	0	0.8	V	2
Output high voltage	V_{OH}	2.4	-	-	V	I_{OH} = -2mA
Output low voltage	V_{OL}	-	-	0.4	V	I_{OL} = 2mA
Input leakage current (Inputs)	I_{IL}	-10	-	10	uA	3

Notes : 1. V_{IH} (max) = 5.6V AC.The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = -2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ V_{DDQ}.
Input leakage currents include Hi-Z output leakage for all bi-directional buffers with Tri-State outputs.

Capacitance (T_A=25, f=1MHz, V_{DD}=3.3V)

Pin	Symbol	Min	Max	Unit
Address (A0 ~ A12, BA0 ~ BA1)	C_{ADD}	45	85	pF
RAS# , CAS# , WE#	C_{IN}	45	85	pF
CKE (CKE0 ~ CKE3)	C_{CKE}	25	45	pF
Clock (CLK0)	C_{CLK}	15	21	pF
CS (CS0# ~ CS3#)	C_{CS}	15	25	pF
DQM (DQM0 ~ DQM7)	C_{DQM}	10	15	pF
DQ (DQ0 ~ DQ63)	C_{OUT}	13	18	pF

DC Characteristics

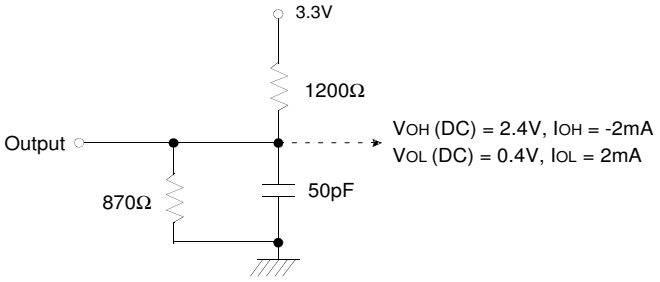
(Recommended operating condition unless otherwise noted, T_A = 0 to 70°C)

Parameter	Symbol	Test Condition	Value			Unit	Note
			-GA	-GH	-GL		
Operating current (One bank active)	I_{CC1}	Burst length = 1 $t_{RC} \geq t_{RC}$(min) I_O = 0 mA	960	960	960	mA	1
Precharge standby current in power-down mode	$I_{CC2}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns	32			mA	
	$I_{CC2}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	32				
Precharge standby current in non power-down mode	$I_{CC2}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	320			mA	
	$I_{CC2}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	160				
Active standby current in power-down mode	$I_{CC3}P$	CKE ≤ V_{IL}(max), t_{CC} = 10ns	80			mA	
	$I_{CC3}PS$	CKE & CLK ≤ V_{IL}(max), t_{CC} = ∞	80				
Active standby current in non power-down mode (One bank active)	$I_{CC3}N$	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC} = 10ns Input signals are changed one time during 20ns	480			mA	
	$I_{CC3}NS$	CKE ≥ V_{IH}(min), CLK ≤ V_{IL}(max), t_{CC} = ∞ Input signals are stable	400			mA	
Operating current (Burst mode)	I_{CC4}	I_O = 0 mA Page burst 4Banks activated t_{CCD} = 2CLKs	1120	1040	1040	mA	1
Refresh current	I_{CC5}	$t_{RC} \geq t_{RC}$(min)	1840	1760	1760	mA	2
Self refresh current	I_{CC6}	CKE ≤ 0.2V	32			mA	

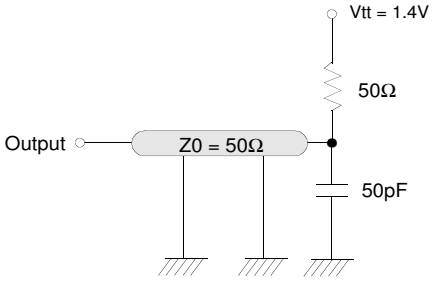
Notes : 1. Measured with outputs open.
2. Refresh period is 64ms.

AC Operating Test Conditions (Vdd=3.3v, 0 - 70°C)

Parameter	Value	Unit
AC input levels (Vih/Vil)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig. 2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

Operating AC Parameter

Parameter	Symbol	Version			Unit	Note
		-GA	-GH	-GL		
Row active to row active delay	tRRD(min)	15	20	20	ns	1
RAS# to CAS# delay	tRCD(min)	20	20	20	ns	1
Row precharge time	tRP(min)	20	20	20	ns	1
Row active time	tRAS(min)	45	50	50	ns	1
	tRAS(max)	100			us	
Row cycle time	tRC(min)	65	70	70	ns	1
Last data in to row precharge	tRDL(min)	2			CLK	2
Last data in to Active delay	tDAL(min)	2 CLK + 20 ns			-	
Last data in to new col. address delay	tCDL(min)	1			CLK	2
Last data in to burst stop	tBDL(min)	1			CLK	2
Col. address to col. address delay	tCCD(min)	1			CLK	3
Number of valid output data	CAS latency=3	2			ea	4
	CAS latency=2	1				

Notes : 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

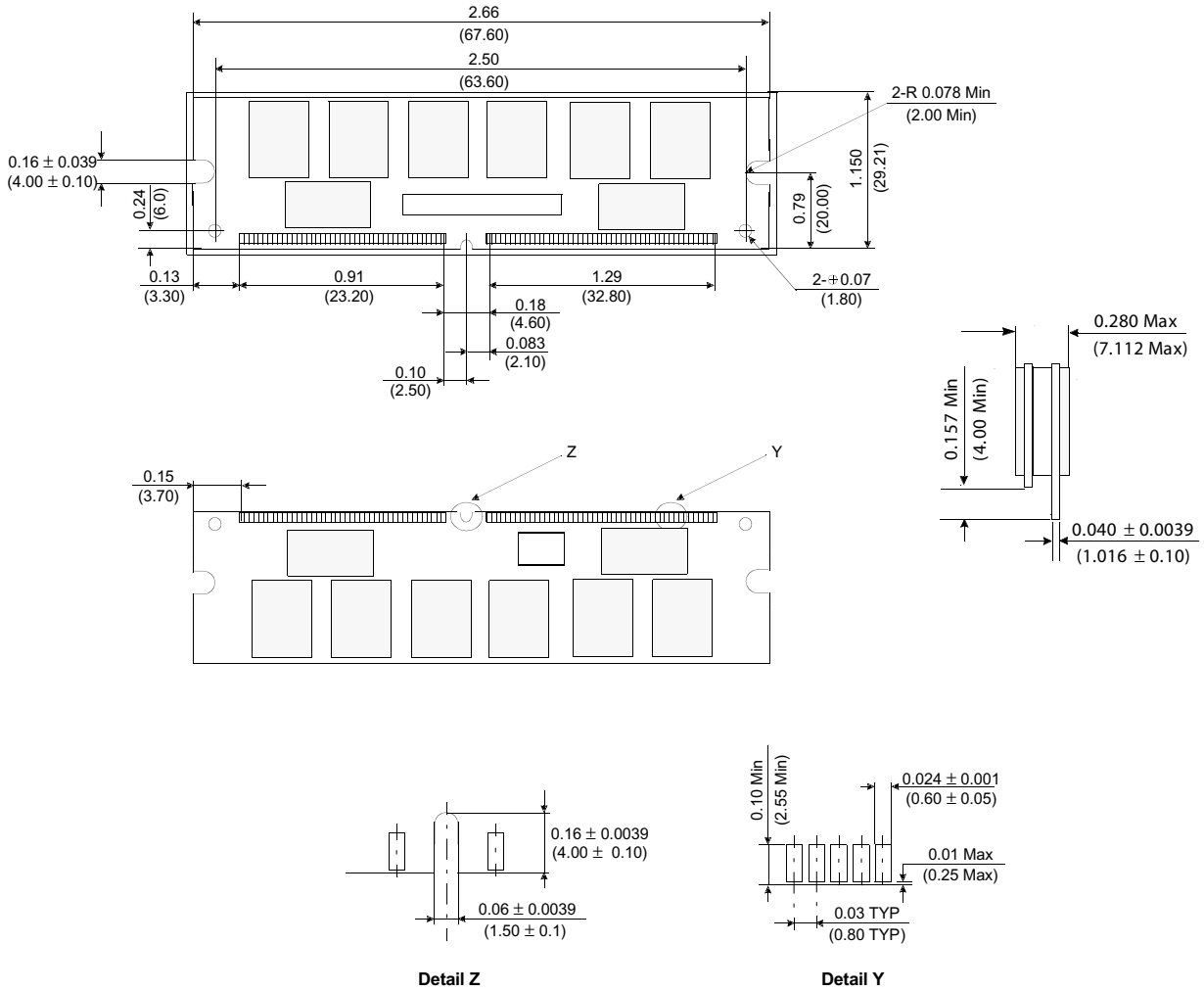
Operating AC Parameters

Parameter		Symbol	GA		Unit	Note
			Min	Max		
CLK cycle time	CAS latency = 3	tCC	7.5	1000	ns	1
	CAS latency = 2		-			
CLK to valid output delay	CAS latency = 3	tSAC		5.4	ns	1,2
	CAS latency = 2			6		
Output data hold time	CAS latency = 3	tOH	3		ns	2
	CAS latency = 2		-			
CLK high pulse width		tCH	2.5		ns	3
CLK low pulse width		tCL	2.5		ns	3
Input setup time		tSS	1.5		ns	3
Input hold time		tSH	0.8		ns	3
CLK to output in Low-Z		tSLZ	1		ns	2
CLK to output in Hi-z	CAS latency = 3	tSHZ		5.4	ns	
	CAS latency = 2			6		

Notes: 1. Parameters depend on programmed CAS latency.
2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
3. Assumed input rise and fall time (tr & tf) = 1ns.
if tr & tf is longer than 1ns, transient timecompensation should be considered,
i.e. ,[(tr + tf)/2-1]ns should be added to the parameter.

Package Dimensions

Units : Inches (Millimeters)



Detail Z **Detail Y**

Tolerances : ±.005(.13) unless otherwise specified