



Product Specifications

PART NO:

AM375S2850E-GA/GH/GL

REV:

1.5

General Information

1GB 128Mx72 SDRAM PC100/PC133 REGISTERED 168 PIN DIMM

Description: The AM375S2850E is a 128M X 72 Synchronous Dynamic RAM high density memory module. This memory module consists of 18 CMOS stacked 128Mx4 bit (stacked from 64Mx4bit) with 4 banks Synchronous DRAMs in TSOP-II 400 mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 168-pin Dual In-line Memory Module and is intended for mounting into connector sockets. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Registered 8 byte SDRAM 168pin DIMM
- High Speed - 100MHz/133MHz CL2/CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3 V power supply
- 13/11/4 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- EPROM Serial Presence Detect
- PCB height: **1125 (mil)**, double sided component
- Gold (Au) contacts

Pin Name	Function
A0-A12	Address inputs
BA0, BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CB0~CB7	Check bit (Data-in/data-out)
CLK0	Clock Input
CKE0	Clock Enable Input
CS0#~CS3#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DQM0-DQM7	Data input/output mask
VDD	Power Supply (3.3V)
VSS	Ground
*VREF	Power Supply for Reference
REGE	Register enable
SDA	Serial Data Input/Output
SCL	SPD Clock Input
SA0 ~ SA2	Address in EEPROM
NC	No Connect
* These pins are not used in this module.	

Order Information:

AM375S2850E-GA X X

DRAM DIE (Option)

DRAM MANUFACTURER
S - SAMSUNG
M - MICRON

MODULE SPEED
GA: PC133 @ CL3
GH: PC100 @ CL2
GL: PC100 @ CL3

M: Leaded

THIS MODULE ASSEMBLED FOR CUSTOMER ONLY.

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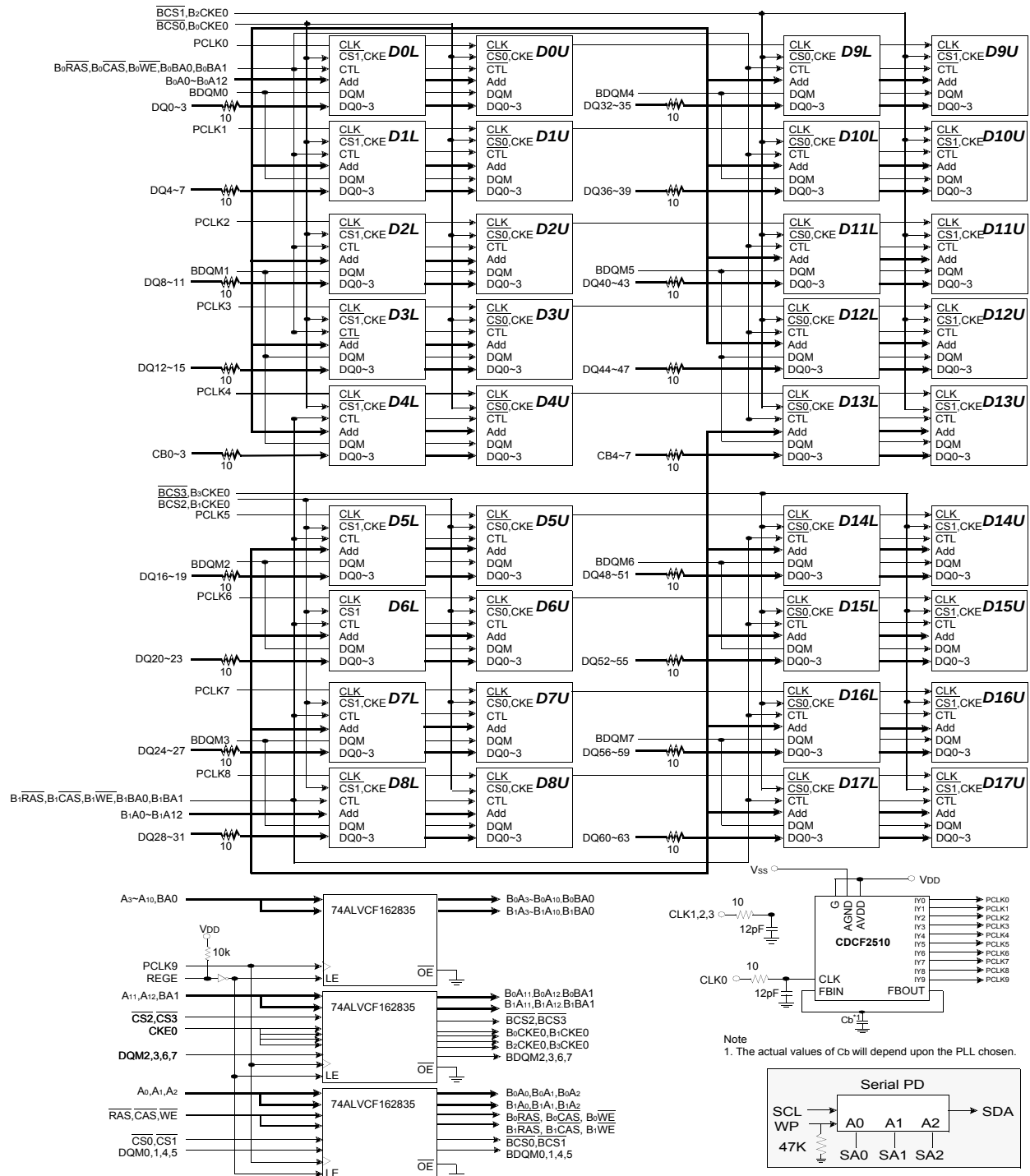
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Pin Configuration

Pin Number	Front Side	Pin Number	Back Side	Pin Number	Front Side	Pin Number	Back Side
1	VSS	43	VSS	85	VSS	127	VSS
2	DQ0	44	NC	86	DQ32	128	CKE0
3	DQ1	45	CS2#	87	DQ33	129	CS3#
4	DQ2	46	DQM2	88	DQ34	130	DQM6
5	DQ3	47	DQM3	89	DQ35	131	DQM7
6	VDD	48	NC	90	VDD	132	*A13
7	DQ4	49	VDD	91	DQ36	133	VDD
8	DQ5	50	NC	92	DQ37	134	NC
9	DQ6	51	NC	93	DQ38	135	NC
10	DQ7	52	CB2	94	DQ39	136	CB6
11	DQ8	53	CB3	95	DQ40	137	CB7
12	VSS	54	VSS	96	VSS	138	VSS
13	DQ9	55	DQ16	97	DQ41	139	DQ48
14	DQ10	56	DQ17	98	DQ42	140	DQ49
15	DQ11	57	DQ18	99	DQ43	141	DQ50
16	DQ12	58	DQ19	100	DQ44	142	DQ51
17	DQ13	59	VDD	101	DQ45	143	VDD
18	VDD	60	DQ20	102	VDD	144	VDD
19	DQ14	61	NC	103	DQ46	145	NC
20	DQ15	62	*VREF	104	DQ47	146	*VREF
21	CB0	63	*CKE1	105	CB4	147	REGE
22	CB1	64	VSS	106	CB5	148	VSS
23	VSS	65	DQ21	107	VSS	149	DQ53
24	NC	66	DQ22	108	NC	150	DQ54
25	NC	67	DQ23	109	NC	151	DQ55
26	VDD	68	VSS	110	VDD	152	VSS
27	WE#	69	DQ24	111	CAS#	153	DQ56
28	DQM0	70	DQ25	112	DQM4	154	DQ57
29	DQM1	71	DQ26	113	DQM5	155	DQ58
30	CS0#	72	DQ27	114	CS1#	156	DQ59
31	NC	73	VDD	115	RAS#	157	VDD
32	VSS	74	DQ28	116	VSS	158	DQ60
33	A0	75	DQ29	117	A1	159	DQ61
34	A2	75	DQ30	118	A3	160	DQ62
35	A4	76	DQ30	119	A5	161	DQ63
36	A6	77	DQ31	120	A7	162	VSS
37	A8	78	VSS	121	A9	163	*CLK3
38	A10/AP	79	*CLK2	122	BA0	164	NC
39	BA1	80	NC	123	A11	165	SA0
40	VDD	81	WP	124	VDD	166	SA1
41	VDD	82	SDA	125	*CLK1	167	SA2
42	CLK0	83	SCL	126	A12	168	VDD

* These pins are not used in this module.

Functional Block Diagram



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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	36	W
Short circuit current	I _{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (TA = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-10	-	10	uA	3

Notes: 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is <= 3ns.
2. V_{IL} (min) = 2.0V AC. The undershoot voltage duration is <= 3ns.
3. Any input 0V <= V_{IN} <= VDDQ.

Capacitance (TA = 25°C, f = 1MHz, VDD = 3.3V)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1)	C _{IN1}	-	15	pF
Input capacitance (RAS#, CAS#, WE#)	C _{IN2}	-	15	pF
Input capacitance (CKE0)	C _{IN3}	-	15	pF
Input capacitance (CLK0)	C _{IN4}	-	20	pF
Input capacitance (CS0# ~ CS3#)	C _{IN5}	-	15	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	-	15	pF
Data input/output capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	C _{OUT}	-	22	pF

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DC Characteristics

(Recommended operation condition unless otherwise noted, TA = 0°C to +70°C)

Parameter	Symbol	Test Condon	Version			Unit	Note
			-GA	-GH	-GL		
Operating current (One bank active)	lcc1	Burst length = 1 trc >= trc(min) lcl = 0 mA	2660	2660	2660	mA	1
Precharge standby current in power-down mode	lcc2P	CKE <= VIL(max), tcc = 10ns	422			mA	
	lcc2PS	CKE & CLK <=VIL(max), tcc = ∞	74			mA	
Precharge standby current in non power-down mode	lcc2N	CKE >= VIH (min), CS# >= VIH (min), tcc = 10ns Input signals are changed one time during 20ns	1070			mA	
	lcc2NS	CKE >= VIH(min), CLK <= VIL(max), tcc = ∞ Input signals are stable	362			mA	
Active standby current in power- down mode	lcc3P	CKE <= VIL(max), tcc = 10ns	566			mA	
	lcc3PS	CKE & CLK <= VIL(max), tcc = ∞	218			mA	
Active standby current in non power-down mode (One bank active)	lcc3N	CKE >= VIH(min), CS# >= VIH(min), tcc = 10ns Input signals are changed one time during 20ns	1430			mA	
	lcc3NS	CKE >= VIH(min), CLK <= VIL (max), tcc = ∞ Input signals are stable	902			mA	
Operating current (Burst mode)	lcc4	lcl = 0 mA Page burst 2 Banks actived tccd = 2CLKs	3020	2840	2840	mA	1
Refresh current	lcc5	trc >= trc(min)	4640	4460	4460	mA	2
Self refresh current	lcc6	CKE <= 0.2V	458			mA	
Note: 1. Measured with outputs open. 2.Refresh period is 64ms.							

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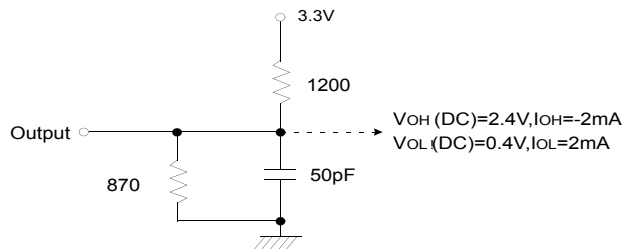
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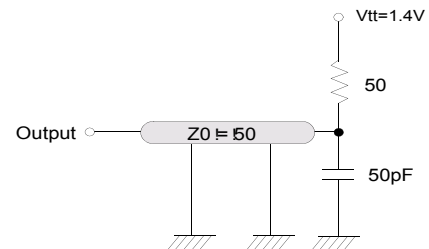
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AC Operating Test Conditions (VDD = 3.3V, TA = 0°C to +70°C)

Parameter	Value	Unit
AC input levels (V _H /V _L)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	t _r /t _f = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig.1)DC output load circuit



(Fig.2) AC output load circuit

Operating AC Parameter

Parameter	Symbol	Version			Unit	Note
		-GA	-GH	-GL		
Row active to row active delay	t _{RRD} (min)	15	20	20	ns	1
RAS# to CAS# delay	t _{RCD} (min)	20	20	20	ns	1
Row precharge time	t _{RP} (min)	20	20	20	ns	1
Row active time	t _{RAS} (min)	45	50	50	ns	1
	t _{RAS} (max)	100			us	
Row cycle time	t _{RC} (min)	65	70	70	ns	1
Last data in to row precharge	t _{RDL} (min)	2			CLK	2
Last data in to Active delay	t _{DAL} (min)	2 CLK + t _{RP}			-	
Last data in to new col. address delay	t _{CDL} (min)	1			CLK	1
Last data in to burst stop	t _{BDL} (min)	1			CLK	2
Col. address to col. address delay	t _{CCD} (min)	1			CLK	2
Number of valid output data	CAS Latency = 3	2			CLK	3
	CAS Latency = 2	1			ea	4

Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.

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Operating AC Parameter

Parameter		Symbol	-GA		-GH		-GL		Unit	Note
			Min	Max	Min	Max	Min	Max		
CLK cycle time	CAS latency = 3	tCC	7.5	1000	-	1000	10	1000	ns	1
	CAS latency = 2		-		10		-			
CLK to valid output delay	CAS latency = 3	tSAC		5.4		-		6	ns	1,2
	CAS latency = 2			-		6		-		
Output data hold time	CAS latency = 3	tOH	3		-		3		ns	2
	CAS latency = 2		-		3		-			
CLK high pulse width		tCH	2.5		3		3		ns	3
CLK low pulse width		tCL	2.5		3		3		ns	3
Input setup time		tSS	1.5		2		2		ns	3
Input hold time		tSH	0.8		1		1		ns	3
CLK to output in Low-Z		tSLZ	1		1		1		ns	2
CLK to output in Hi-z	CAS latency = 3	tSHZ		5.4		-		6	ns	
	CAS latency = 2			-		6		-		

Notes: 1. Parameters depend on programmed CAS latency.
 2. If clock rising time is longer than 1ns, (tr/2-0.5)ns should be added to the parameter.
 3. Assumed input rise and fall time (tr & tf) = 1ns.
 if tr & tf is longer than 1ns, transient time compensation should be considered,
 i.e. [(tr + tf)/2-1]ns should be added to the parameter.

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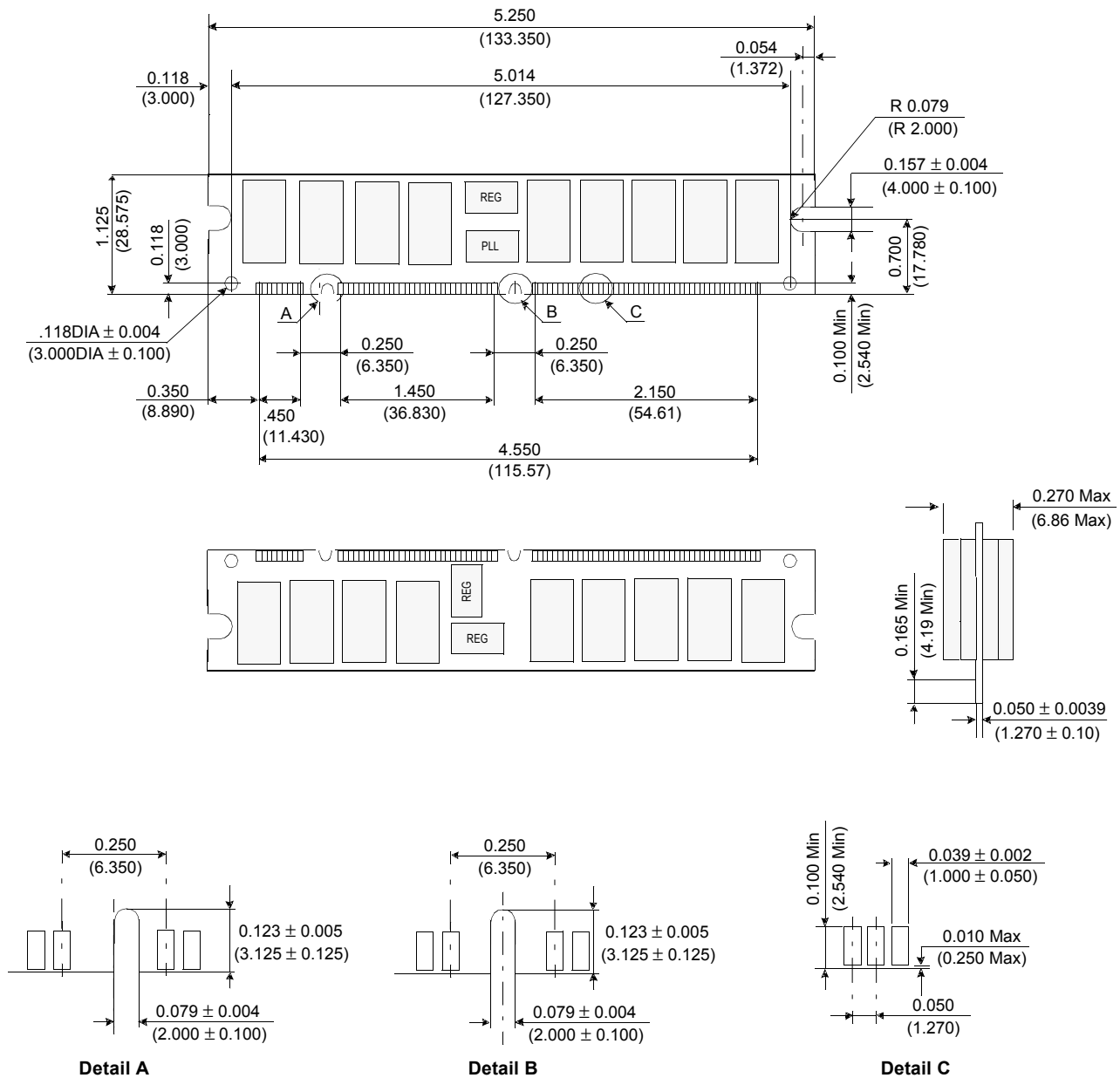
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Package Dimensions

Units : Inches (Millimeters)


 Tolerances : ± 0.005 (.13) unless otherwise specified