

<b>Product Specifications</b>		
PART NO.:	<b>VL495T5763E-E7Y</b>	<b>REV: 1.1</b>

## General Information

### 2GB 256Mx72 DDR2 SDRAM VLP ECC REGISTERED Mini-DIMM 244-PIN

## Description

The VL495T5763E is a 256Mx72 DDR2 SDRAM high density Mini-DIMM. This memory module consists of nine CMOS 256Mx8 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, a 25-bit registered buffer in BGA package, a zero delay PLL clock in BGA package, and a 2K EEPROM in an 8-pin MLF package. This module is a 244-pin mini dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

## Features

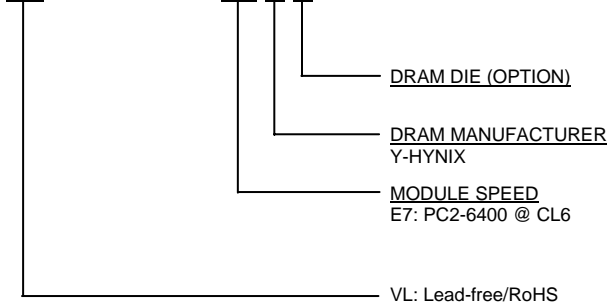
- 244-pin, registered mini dual in-line memory module (Mini-DIMM)
- JEDEC pin out
- Supports ECC error detection and correction
- Fast data transfer rate: PC2-6400
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL\_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Differential clock inputs (CK, CK#)
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 6 (DDR2-800)
- Write latency = Read latency - 1 tCK
- Eight internal component banks for concurrent operation
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD)
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 18.29mm (0.720”), double sided components

## Pin Description

Pin Name	Function
A0~A14	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS8	Data Strobes
DQS0#~DQS8#	Data Strobes Complement
ODT0	On-die Termination Control
CK, CK#	Clock Input
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
CB0~CB7	Check Bits
DM0~DM8	Data Masks
VDD	Voltage Supply 1.8V +/- 0.1V
VSS	Ground
SA0~SA1	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
VREF	SSTL_18 Reference Voltage
NC	No Connect

## Order Information:

**VL495T5763E - E7 Y X**





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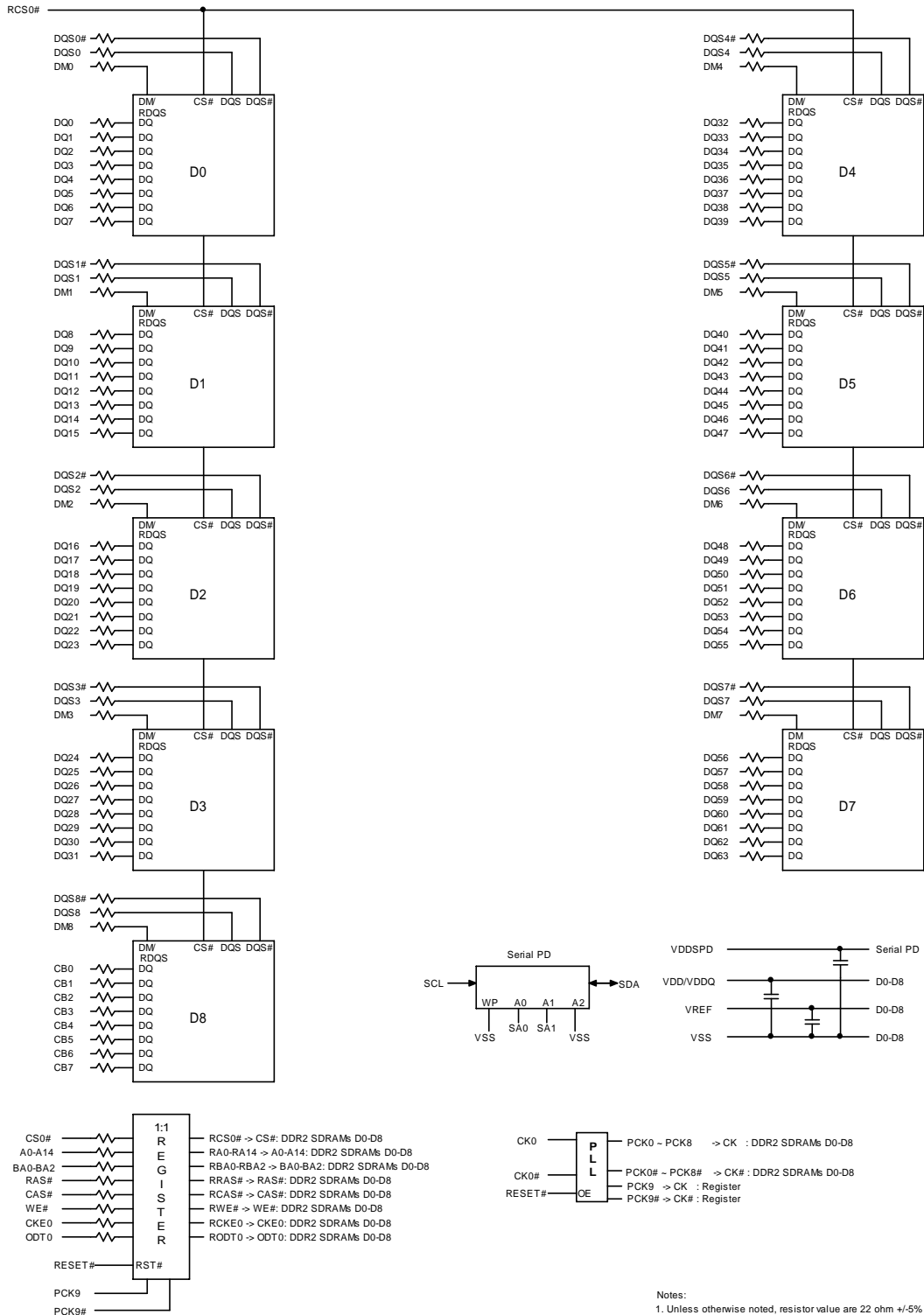
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## Pin Configuration

244-PIN DDR2 Mini-DIMM FRONT SIDE								244-PIN DDR2 Mini-DIMM BACK SIDE							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	32	VSS	63	VDDQ	93	VSS	123	VSS	154	DQ28	185	A3	215	DM5
2	VSS	33	DQ24	64	A2	94	DQS5#	124	DQ4	155	DQ29	186	A1	216	NC
3	DQ0	34	DQ25	65	VDD	95	DQS5	125	DQ5	156	VSS	187	VDD	217	VSS
4	DQ1	35	VSS	KEY		96	VSS	126	VSS	157	DM3	KEY		218	DQ46
5	VSS	36	DQS3#	66	VSS	97	DQ42	127	DM0	158	NC	188	CK0	219	DQ47
6	DQS0#	37	DQS3	67	VSS	98	DQ43	128	NC	159	VSS	189	CK0#	220	VSS
7	DQS0	38	VSS	68	NC	99	VSS	129	VSS	160	DQ30	190	VDD	221	DQ52
8	VSS	39	DQ26	69	VDD	100	DQ48	130	DQ6	161	DQ31	191	A0	222	DQ53
9	DQ2	40	DQ27	70	A10/ AP	101	DQ49	131	DQ7	162	VSS	192	BA1	223	VSS
10	DQ3	41	VSS	71	BA0	102	VSS	132	VSS	163	CB4	193	VDD	224	NC
11	VSS	42	CB0	72	VDD	103	SA2	133	DQ12	164	CB5	194	RAS#	225	NC
12	DQ8	43	CB1	73	WE#	104	NC	134	DQ13	165	VSS	195	VDDQ	226	VSS
13	DQ9	44	VSS	74	VDDQ	105	VSS	135	VSS	166	DM8	196	CS0#	227	DM6
14	VSS	45	DQS8#	75	CAS#	106	DQS6#	136	DM1	167	NC	197	VDDQ	228	NC
15	DQS1#	46	DQS8	76	VDDQ	107	DQS6	137	NC	168	VSS	198	ODT0	229	VSS
16	DQS1	47	VSS	77	CS1# *	108	VSS	138	VSS	169	CB6	199	A13	230	DQ54
17	VSS	48	CB2	78	OTD1 *	109	DQ50	139	NC	170	CB7	200	VDD	231	DQ55
18	RESET#	49	CB3	79	VDDQ	110	DQ51	140	NC	171	VSS	201	NC	232	VSS
19	NC	50	VSS	80	NC	111	VSS	141	VSS	172	NC	202	VSS	233	DQ60
20	VSS	51	NC	81	VSS	112	DQ56	142	DQ14	173	VDDQ	203	DQ36	234	DQ61
21	DQ10	52	VDDQ	82	DQ32	113	DQ57	143	DQ15	174	CKE1 *	204	DQ37	235	VSS
22	DQ11	53	CKE0	83	DQ33	114	VSS	144	VSS	175	VDD	205	VSS	236	DM7
23	VSS	54	VDD	84	VSS	115	DQS7#	145	DQ20	176	A15 *	206	DM4	237	NC
24	DQ16	55	BA2	85	DQS4#	116	DQS7	146	DQ21	177	A14	207	NC	238	VSS
25	DQ17	56	NC	86	DQS4	117	VSS	147	VSS	178	VDDQ	208	VSS	239	DQ62
26	VSS	57	VDDQ	87	VSS	118	DQ58	148	DM2	179	A12	209	DQ38	240	DQ63
27	DQS2#	58	A11	88	DQ34	119	DQ59	149	NC	180	A9	210	DQ39	241	VSS
28	DQS2	59	A7	89	DQ35	120	VSS	150	VSS	181	VDD	211	VSS	242	SDA
29	VSS	60	VDD	90	VSS	121	SA0	151	DQ22	182	A8	212	DQ44	243	SCL
30	DQ18	61	A5	91	DQ40	122	SA1	152	DQ23	183	A6	213	DQ45	244	VDDSPD
31	DQ19	62	A4	92	DQ41			153	VSS	184	VDDQ	214	VSS		

\*: These pins are not used in this module.  
RESET# (Pin 18) is connected to both OE of the PLL and RESET# of the register

## Function Block Diagram



<b>Product Specifications</b>		
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<b>Absolute Maximum Ratings</b>					
Symbol	Parameter		MIN	MAX	Unit
VDD	Voltage on VDD pin relative to VSS		-1.0	2.3	V
VDDQ	Voltage on VDDQ pin relative to VSS		-0.5	2.3	V
VDDL	Voltage on VDDL pin relative to VSS		-0.5	2.3	
VIN, VOUT	Voltage on any pin relative to VSS		-0.5	2.3	V
TSTG	Storage temperature		-55	100	°C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-5	5	uA
		CS#, CKE, ODT	-5	5	uA
		CK, CK#	-250	250	uA
		DM	-2	2	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	DQ, DQS, DQS#	-5	5	uA
IVREF	VREF supply leakage current; VREF = Valid VREF level		-18	18	uA

<b>DC Operating Conditions</b>						
Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Note:

- VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
- VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
- VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
- VDDQ tracks with VDD; VDDL tracks with VDD.

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Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 95	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 – 85°C, operation temperature range, all DRAM specifications will be supported. The refresh rate is required to double when 85°C < TOPER <= 95°C.				

Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.200	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.200	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A14, BA0~BA2, RAS#, CAS#, WE#)	CIN1	6.5	7.5	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	6.5	7.5	pF
Input capacitance (CK0, CK0#)	CIN3	6	7	pF
Input/Output capacitance (DQ, DQS, DQS#, DM, CB)	CIO	6.5	7.5	pF

# Product Specifications

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## IDD Specification

Condition	Symbol	-E7	Unit
<b>Operating one bank active-pre-charge;</b> $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS\ MIN(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0	1255	mA
<b>Operating one bank active-read-pre-charge;</b> IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RAS} = t_{RAS\ MIN(IDD)}$ ; $t_{RCD} = t_{RCD(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD1	1345	mA
<b>Pre-charge power-down current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P	508	mA
<b>Pre-charge quiet standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q	850	mA
<b>Pre-charge standby current;</b> All banks idle; $t_{CK} = t_{CK(IDD)}$ ; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING.	IDD2N	895	mA
<b>Active power-down current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	715	mA
	Slow PDN Exit MRS(12) = 1	562	mA
<b>Active standby current;</b> All banks open; $t_{CK} = t_{CK(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N	1120	mA
<b>Operating burst write current;</b> All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W	2560	mA
<b>Operating burst read current;</b> All banks open; Continuous burst reads; IOUT = 0mA; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$ ; $t_{RAS} = t_{RAS\ MAX(IDD)}$ ; $t_{RP} = t_{RP(IDD)}$ ; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R	2380	mA
<b>Burst refresh current;</b> $t_{CK} = t_{CK(IDD)}$ ; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5	2470	mA
<b>Self refresh current;</b> CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6	135
<b>Operating bank interleave read current;</b> All bank interleaving reads; IOUT = 0mA; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$ ; $t_{CK} = t_{CK(IDD)}$ ; $t_{RC} = t_{RC(IDD)}$ ; $t_{RRD} = t_{RRD(IDD)}$ ; $t_{RCD} = 1 * t_{CK(IDD)}$ ; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7	3145	mA
Notes: IDD specification is based on Hynix A-die components. *: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode. **: Value calculated reflects all module ranks in this operating condition.			

# Product Specifications

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VL495T5763E-E7Y

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## AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-800 (-E7)		Unit	
		Min	Max		
<b>Clock Timing</b>					
Clock Cycle Time	CL6	$t_{CK(6)}$	2500	8000	ps
	CL5	$t_{CK(5)}$	-	-	ps
CK high-level width	$t_{CH(avg)}$	0.48	0.52	$t_{CK}$	
CK high-level width	$t_{CL(avg)}$	0.48	0.52	$t_{CK}$	
Half clock period	$t_{HP}$	MIN ( $t_{CH}$ , $t_{CL}$ )	-	ps	
Clock jitter	$t_{JIT}$	-100	100	ps	
<b>Data Timing</b>					
DQ output access time from CK/CK#	$t_{AC}$	-400	400	ps	
Data-out high impedance window from CK/CK#	$t_{HZ}$	-	$t_{AC(MAX)}$	ps	
Data-out low impedance window from CK/CK#	$t_{LZ}$	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps	
DQ and DM input setup time relative to DQS	$t_{DS}$	50	-	ps	
DQ and DM input hold time relative to DQS	$t_{DH}$	125	-	ps	
DQ and DM input pulse width ( for each input)	$t_{DIPW}$	0.35	-	$t_{CK}$	
Data hold skew factor	$t_{QHS}$	-	300	ps	
DQ-DQS hold, DQS to first DQ to go non-valid, per access	$t_{QH}$	$t_{HP} - t_{QHS}$	-	ps	
<b>Data Strobe Timing</b>					
DQS input high pulse width	$t_{DQSH}$	0.35	-	$t_{CK}$	
DQS input low pulse width	$t_{DQSL}$	0.35	-	$t_{CK}$	
DQS output access time from CK/CK#	$t_{DQSCK}$	-350	+350	ps	
DQS failing edge to CK rising-setup time	$t_{DSS}$	0.2	-	$t_{CK}$	
DQS failing edge from CK rising-hold time	$t_{DSH}$	0.2	-	$t_{CK}$	
DQS-DQ skew, DQS to last DQ valid, per group, per access	$t_{DQSQ}$	-	200	ps	
DQS read preamble	$t_{RPRE}$	0.9	1.1	$t_{CK}$	
DQS read preamble	$t_{RPST}$	0.4	0.6	$t_{CK}$	
DQS read preamble	$t_{WPRE}$	0.35	-	$t_{CK}$	
DQS read preamble	$t_{WPST}$	0.4	0.6	$t_{CK}$	
Write command to first DQS latching transition	$t_{DQSS}$	WL-0.25	WL+0.25	$t_{CK}$	

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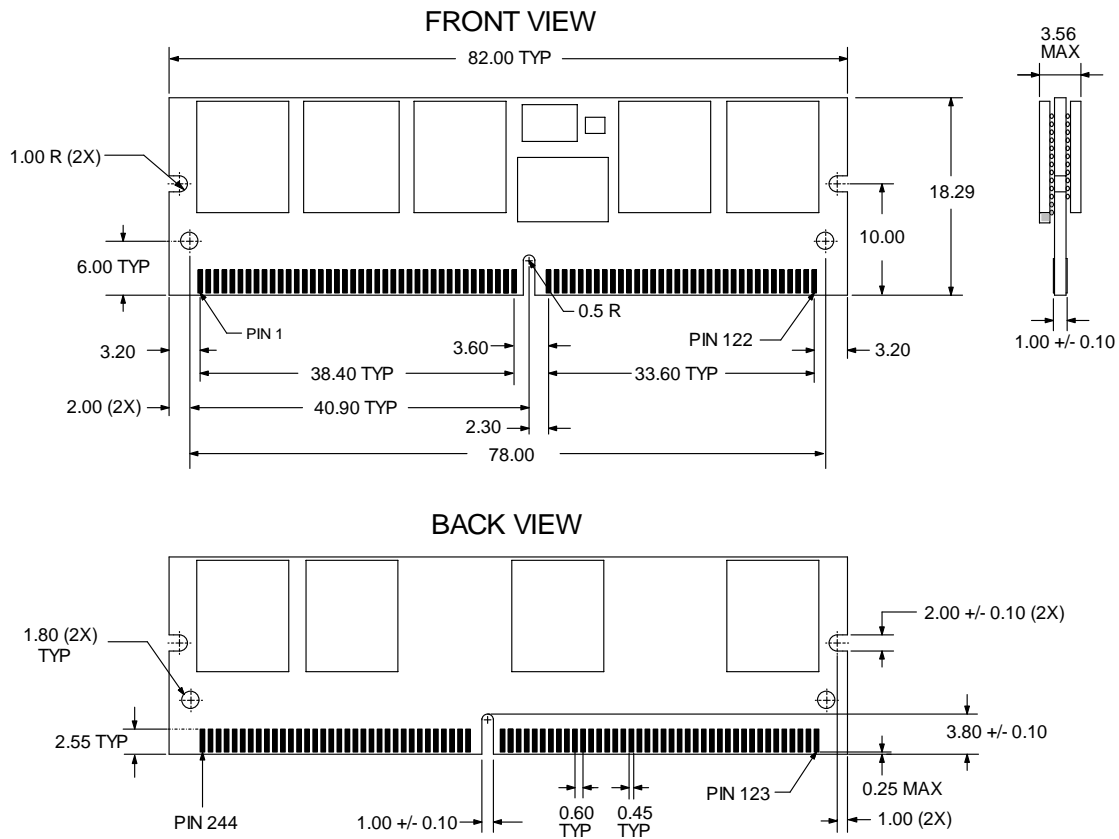
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## AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-800 (-E7)		Unit
		Min	Max	
<b>Command and Address Timing</b>				
Address and control input pulse width for each input	$t_{IPW}$	0.6	-	$t_{CK}$
Address and control input setup time	$t_{IS}$	175	-	ps
Address and control input hold time	$t_{IH}$	250	-	ps
CAS# to CAS# command delay	$t_{CCD}$	2	-	ps
ACTIVE to ACTIVE (same bank) command	$t_{RC}$	57.5/60	-	ns
ACTIVE bank a to ACTIVE bank b command	$t_{RRD}$	7.5	-	ns
ACTIVE to READ or WRITE delay	$t_{RCD}$	12.5/15	-	ns
Four Bank Activate period	$t_{FAW}$	35	-	ns
ACTIVE to PRECHARGE command	$t_{RAS}$	45	70,000	ns
Internal READ to precharge Command delay	$t_{RTP}$	7.5	-	ns
Write recovery time	$t_{WR}$	15	-	ns
Auto precharge write recovery + precharge time	$t_{DAL}$	$t_{WR} + t_{IRP}$	-	nCK
Internal WRITE to READ Command delay	$t_{WTR}$	7.5	-	ns
PRECHARGE command period	$t_{RP}$	15	-	ns
LOAD MODE command cycle time	$t_{MRD}$	2	-	$t_{CK}$
CKE low to CK, CK# uncertainty	$t_{DELAY}$	$t_{IS} + t_{CK} + t_{IH}$	-	ns
<b>Self Refresh</b>				
Refresh to Active or Refresh to Refresh command interval	$t_{RFC}$	195	-	ns
Average periodic Refresh interval	$t_{REFI}$	-	7.8	us
Exit Self Refresh to non-READ command	$t_{XSNR}$	$t_{RFC(MIN)} + 10$	-	ns
Exit Self Refresh to READ	$t_{XSRD}$	200	-	$t_{CK}$
<b>ODT</b>				
ODT turn-on delay	$t_{AOND}$	2	2	$t_{CK}$
ODT turn-on	$t_{AON}$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 700$	ps
ODT turn-off delay	$t_{AOFD}$	2.5	2.5	$t_{CK}$
ODT turn-off	$t_{AOF}$	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	ps
ODT turn-on(power-down mode)	$t_{AONPD}$	$t_{AC(MIN)} + 2000$	$2t_{CK} + t_{AC(MAX)} + 1000$	ps
ODT turn-off (power-down mode)	$t_{AOFPD}$	$t_{AC(MIN)} + 2000$	$2.5t_{CK} + t_{AC(MAX)} + 1000$	ps
ODT to power-down entry latency	$t_{ANPD}$	3	-	$t_{CK}$
ODT power-down exit latency	$t_{AXPD}$	8	-	$t_{CK}$
OCD drive mode output delay	$t_{OIT}$	0	12	ns
<b>Power Down</b>				
Exit active power-down to READ command, MR[bit12=0]	$t_{XARD}$	2	-	$t_{CK}$
Exit active power-down to READ command, MR[bit12=1]	$t_{XARDS}$	7-AL	-	$t_{CK}$
Exit precharge power-down to any non-READ command	$t_{XP}$	2	-	$t_{CK}$
CKE minimum high/low time	$t_{CKE}$	3	-	$t_{CK}$

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## Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.  
 2. The dimensional diagram is for reference only.



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**Revision History:**

Date	Rev.	Page	Changes
11/08/09	1.0	All	Spec release
08/26/10	1.1	All	Updated datasheet