Product Specifications		
PART NO.:	**VL474S2858B-GAS**	**REV: 1.2**

General Information

1GB 128Mx72 SDRAM PC133 ECC UNBUFFERED SODIMM 144-PIN

Description

The VL474S2858B is a 128Mx72 synchronous dynamic RAM high density SODIMM. This memory module consists of nine stacked CMOS 128Mx8 bits with 4 banks synchronous DRAMs in TSOP-II 400 mil packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features

- Unbuffered 8 byte SDRAM 144-pin SODIMM
- Onboard PLL clock driver
- High speed - 133MHz @CL3
- Single 3.3V ±0.3V power supply
- Burst mode operation
- 13/11/2 Addressing (Row/Column/Bank)
- Programmable burst lengths (BL): 1, 2, 4, 8, or full page
- Auto precharge option
- Serial presence-detect (SPD) with EEPROM
- Auto & Self refresh capability (8192 Cycles/64ms)
- LVTTL compatible inputs and outputs
- MRS cycle with address key programs
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB height: 31.75mm (1.250”), double sided component

Pin Description

Pin Name	Function
A0~A12	Address Inputs
BA0~BA1	Bank Address Inputs
DQ0~DQ63	Data Input/Output
CB0~CB7	Check bits
CLK0	Clock Input
CKE0, CKE1	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
DQM0~DQM7	Data Input/Output Mask
VDD	Voltage Supply 3.3V (+/-0.3V)
VSS	Ground
SDA	SPD Data Input/Output
SCL	SPD Clock Input
VREF *	Power supply for Reference
NC	No Connect
* These pins are not used in this module.	

Order Information:

VL 474S2858B - GA S X

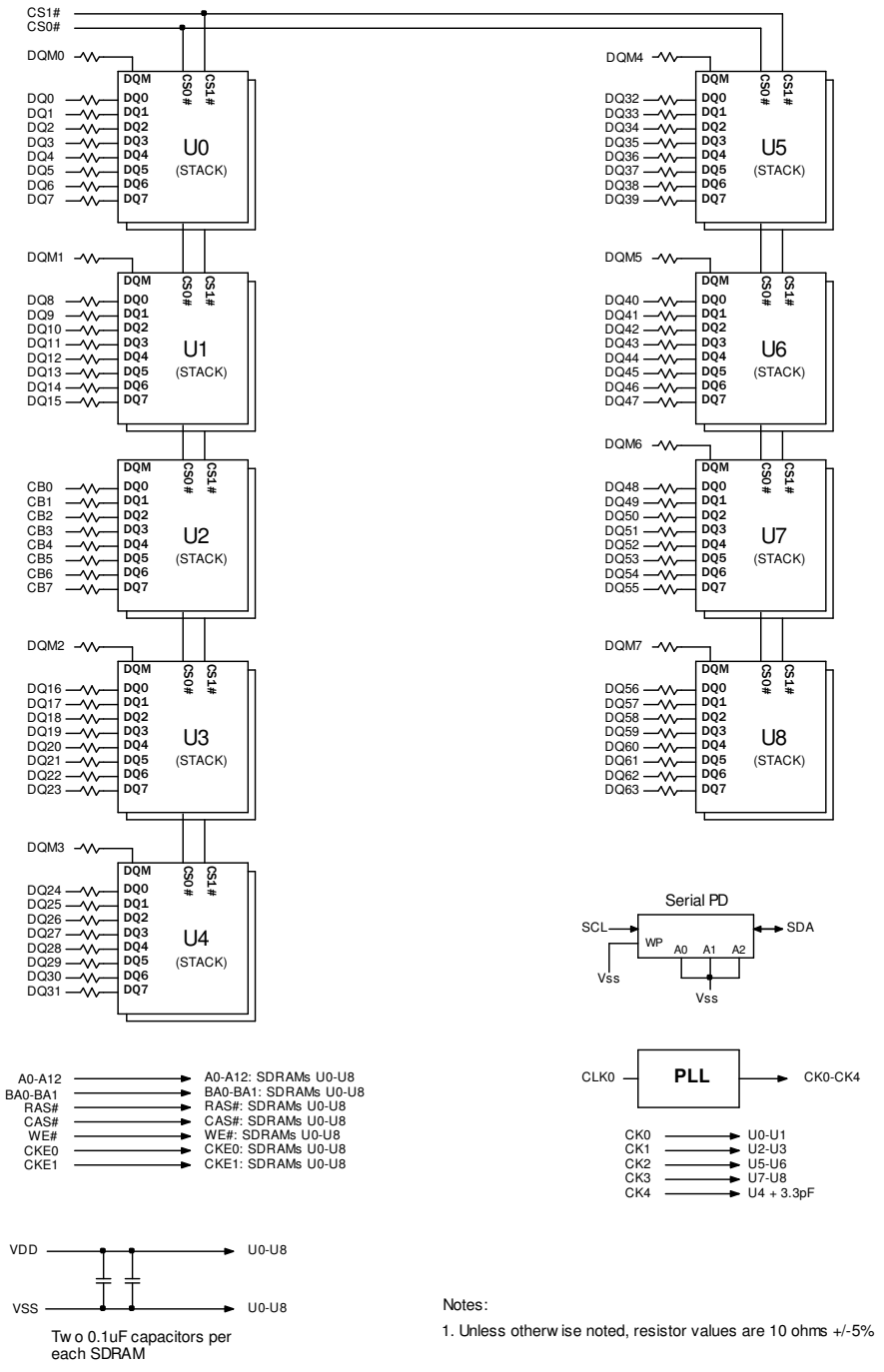
- X: DRAM DIE (Option)
- S: DRAM MANUFACTURER — S - SAMSUNG
- GA: MODULE SPEED — GA: PC133 @ CL3
- VL: Lead-free/RoHS

Pin Configuration

144-PIN SDRAM SODIMM FRONT SIDE				144-PIN SDRAM SODIMM BACK SIDE			
Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VSS	2	VSS	73	NC	74	CLK1 *
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	CB2	78	CB6
7	DQ2	8	DQ34	79	CB3	80	CB7
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10/AP	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	VDD	46	VDD	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	CB0	58	CB4	129	VDD	130	VDD
59	CB1	60	CB5	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	CS0#	70	A12	141	SDA	142	SCL
71	CS1#	72	A13 *	143	VDD	144	VDD

* These pins are not used in this module.

Function Block Diagram



Notes:

1. Unless otherwise noted, resistor values are 10 ohms +/-5%

Absolute Maximum Ratings

Symbol	Parameter	Value	Unit
VIN, VOUT	Voltage on any pin relative to VSS	-1.0 ~ 4.6	V
VDD, VDDQ	Voltage on VDD supply relative to VSS	-1.0 ~ 4.6	V
TSTG	Storage temperature	-55 ~ +150	^{0}C
PD	Power dissipation	18	W
IOS	Short circuit current	50	mA

Note:

Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions

(TA= 0^{o}C to +70^{o}C)

Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD, VDDQ	Supply voltage	3.0	3.3	3.6	V	
VIH	Input high voltage	2.0	3.0	VDDQ + 0.3	V	1
VIL	Input low voltage	-0.3	0	0.8	V	2
VOH	Output high voltage	2.4	-	-	V	IOH=-2mA
VOL	Output low voltage	-	-	0.4	V	IOL= 2mA
IIL	Input leakage current (Inputs)	-10	-	10	uA	3

Note:

1. VIH (max) = 5.6V AC. The overshoot voltage duration is <= 3ns.
2. VIL (min) = 2.0V AC. The undershoot voltage duration is <= 3ns.
3. Any input 0V <= VIN <= VDDQ.

Input/Output Capacitance

TA=25^{0}C, f=1MHz, VDD = 3.3V

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	CIN1	49	72.4	pF
Input capacitance (CKL0)	CIN2	15	18	pF
Input capacitance (CS0#, CS1#), (CKE0, CKE1)	CIN3	26.5	38.2	pF
Input capacitance (DQM0 ~ DQM7)	CIN4	9	11.6	pF
Input/Output capacitance (DQ0 ~ DQ63), (CB0 ~ CB7)	CIO	12	16	pF

DC Characteristics (Recommended operation condition unless otherwise noted, T_A = 0°C to 70°C)

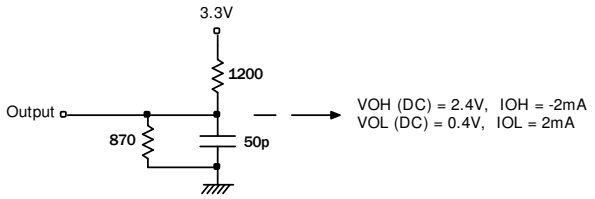
Parameter/Condition	Symbol	Version	Unit	Note
		GA (PC133)		
Operating current: Active mode; Burst = 2; READ or WRITE; t_{RC} = t_{RC} (MIN)	IDD1	905	mA	1
Standby current: power-down mode; CKE = HIGH; All banks idle	IDD2	176	mA	
Standby current: Active mode; CS# = HIGH; CKE = HIGH; All banks active after t_{RCD} met; No accesses in progress	IDD3	248	mA	
Operating current: Burst mode; Page burst; READ or WRITE; All banks active	IDD4	950	mA	1
Auto refresh current: CS# = HIGH; CKE = HIGH; t_{RFC} = t_{RFC} (MIN)	IDD5	1940	mA	2
Self refresh current: CKE ≤ 0.2V	IDD6	108	mA	

Note: ICCs were calculated using Samsung D-die components. Other manufacturers' DRAMs may have different values.

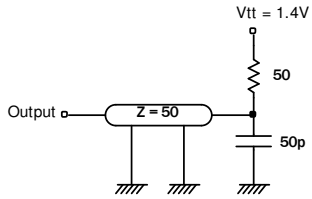
1. Measured with outputs open.
2. Refresh period is 64 ms.

AC Operating Test Conditions (VDD = 3.3V, TA = 0°C to +70°C)

Parameter	Value	Unit
AC input levels (VIH/VIL)	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig. 1) DC output load circuit



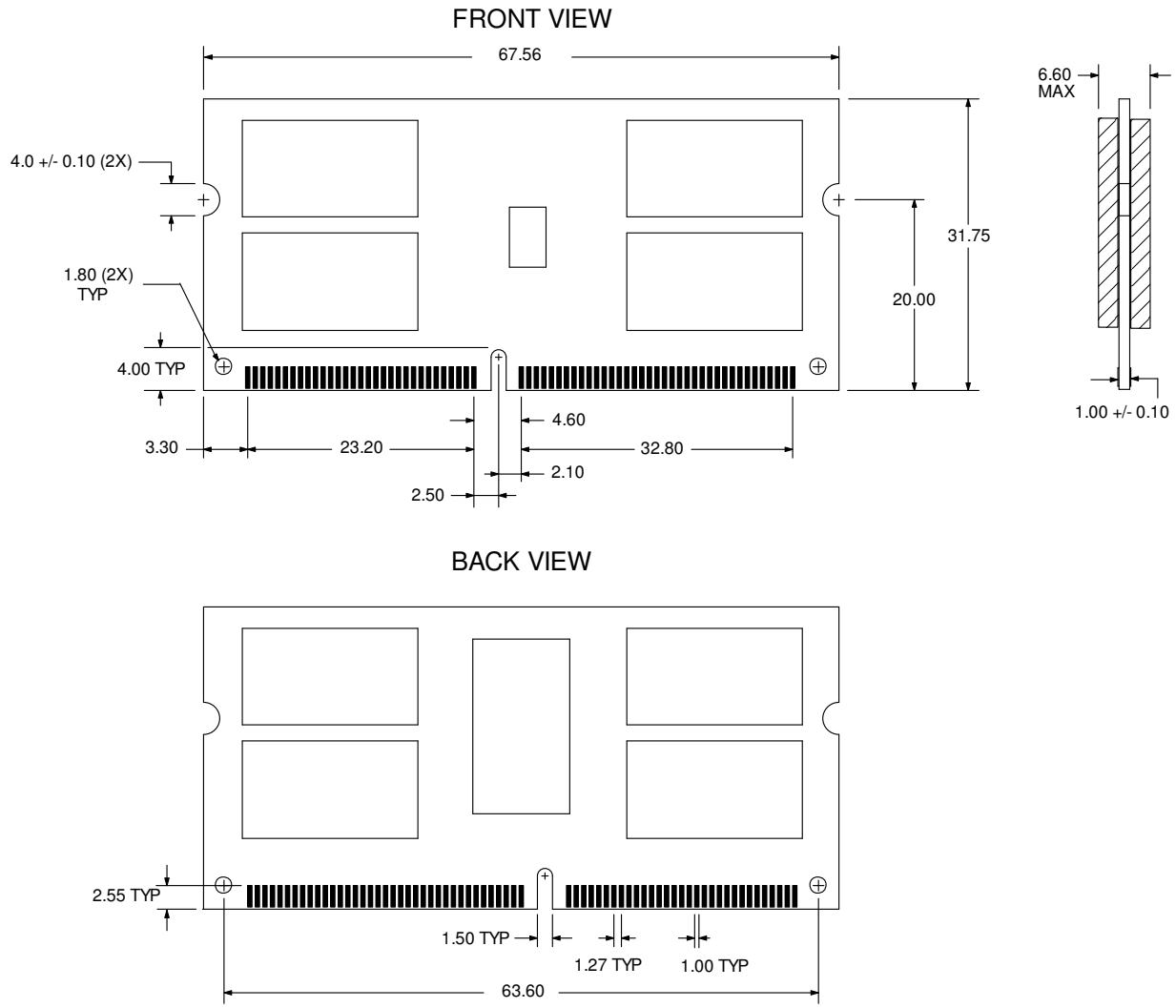
(Fig. 2) AC output load circuit

AC TIMING PARAMETERS & SPECIFICATIONS

Parameter		Symbol	Version		Unit	Note
			GA (PC133)			
			Min	Max		
Row active to row active delay		tRRD(min)	15		ns	1
RAS# to CAS# delay		tRCD(min)	20		ns	1
Row precharge time		tRP(min)	20		ns	1
Row active time		tRAS(min)	45	100	us	
Row cycle time		tRC(min)	65		ns	2
Last data in to row precharge		tRDL(min)	2		t_{CK}	2
Last data in to Active delay		tDAL(min)	2 CLK + tRP		-	8
Last data in to new col. address delay		tCDL(min)	1		t_{CK}	2
Last data in to burst stop		tBDL(min)	1		t_{CK}	2
Col. address to col. address delay		tCCD(min)	1		t_{CK}	3
Number of valid output data	CAS Latency = 3	-	2		ea	4
CLK cycle time	CAS Latency = 3	tCC	7.5	1000	ns	5
CLK to valid output delay	CAS Latency = 3	tSAC		5.4	ns	5, 6
Output data hold time	CAS Latency = 3	tOH	3		ns	6
CLK high pulse width		tCH	2.5		ns	7
CLK low pulse width		tCL	2.5		ns	7
Input setup time		tIS	1.5		ns	7
Input hold time		tIH	0.8		ns	7
CLK to output in Low-Z		tSLZ	1		ns	6
CLK to output in Hi-Z	CAS Latency = 3	tSHZ		5.4	ns	

Notes: 1. The minimum number of clock cycles is determined by dividing the minimum time required with clock cycle time and then rounding off to the next higher integer.
2. Minimum delay is required to complete write.
3. All parts allow every cycle column address change.
4. In case of row precharge interrupt, auto precharge and read burst stop.
5. Parameters depend on programmed CAS latency.
6. If clock rising time is longer than 1ns, (tr/2-0.5) ns should be added to the parameter.
7. Assumed input rise and fall time (tr & tf) = 1ns.
if tr & tf is longer than 1ns, transient time compensation should be considered,
i.e., [(tr + tf)/2-1] ns should be added to the parameter.
8. When a Write command with Auto Precharge has been issued, a time of tDAL(min) has be full filled before the next Activate Command can be applied.
For each of the terms, if not already an integer, round up to the next highest integer. tCK is equal to the actual system clock time.

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.13 unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
04/10/2008	1.0	All	Spec release
10/22/2010	1.2	All	Update All