



Product Specifications

PART NO:

VL466S6555E-GAM

REV:

1.0

General Information

512MB 64Mx64 SDRAM PC133 UNBUFFERED SODIMM 144-PIN

Description: The VL466S6555E is a 64M x 64 synchronous dynamic RAM high density memory module. This memory module consists of sixteen CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in BGA packages and a 2K EEPROM in 8-pin TSSOP package. This module is a 144-pin small-outline dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each SDRAM.

Features:

- Unbuffered 8 byte SDRAM 144pin SODIMM
High Speed - 133MHz, CL3
- Burst Mode Operation
- Auto & Self refresh Capability (8192 Cycles/64ms)
- LVTTTL compatible inputs and outputs
- Single 3.3V ± 0.3 V power supply
- 13/10/4 Addressing (Row/Column/Bank)
- MRS cycle with address key programs
- Serial Presence Detect (SPD) with EEPROM
- PCB height: **1000 (mil)**, double sided component
- Gold edge contacts

Pin Name	Function
A0-A12	Address inputs
BA0, BA1	Bank Select Address
DQ0-DQ63	Data Input/Output
CLK0, CLK1	Clock Input
CKE0, CKE1	Clock Enable Input
CS0#, CS1#	Chip Select Input
RAS#	Row Address Strobe
CAS#	Column Address Input
WE#	Write Enable
DQM0-DQM7	Data input/output mask
VDD	Power Supply (3.3V)
VSS	Ground
*VREF	Power Supply for Reference
SDA	Serial Data Input/Output
SCL	SPD Clock Input
NC	No Connect

* These pins are not used in this module.

Order Information:

VL466S6555E-GAMX

DRAM DIE (option)

DRAM MANUFACTURER
M - MICRON

MODULE SPEED
GA: PC133 @ CL3

VL: Lead-free/RoHS

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Pin Configuration

Pin Number	Front Side	Pin Number	Back Side	Pin Number	Front Side	Pin Number	Back Side
1	VSS	2	VSS	73	NC	74	CLK1
3	DQ0	4	DQ32	75	VSS	76	VSS
5	DQ1	6	DQ33	77	NC	78	NC
7	DQ2	8	DQ34	79	NC	80	NC
9	DQ3	10	DQ35	81	VDD	82	VDD
11	VDD	12	VDD	83	DQ16	84	DQ48
13	DQ4	14	DQ36	85	DQ17	86	DQ49
15	DQ5	16	DQ37	87	DQ18	88	DQ50
17	DQ6	18	DQ38	89	DQ19	90	DQ51
19	DQ7	20	DQ39	91	VSS	92	VSS
21	VSS	22	VSS	93	DQ20	94	DQ52
23	DQM0	24	DQM4	95	DQ21	96	DQ53
25	DQM1	26	DQM5	97	DQ22	98	DQ54
27	VDD	28	VDD	99	DQ23	100	DQ55
29	A0	30	A3	101	VDD	102	VDD
31	A1	32	A4	103	A6	104	A7
33	A2	34	A5	105	A8	106	BA0
35	VSS	36	VSS	107	VSS	108	VSS
37	DQ8	38	DQ40	109	A9	110	BA1
39	DQ9	40	DQ41	111	A10/AP	112	A11
41	DQ10	42	DQ42	113	VDD	114	VDD
43	DQ11	44	DQ43	115	DQM2	116	DQM6
45	VDD	46	VDD	117	DQM3	118	DQM7
47	DQ12	48	DQ44	119	VSS	120	VSS
49	DQ13	50	DQ45	121	DQ24	122	DQ56
51	DQ14	52	DQ46	123	DQ25	124	DQ57
53	DQ15	54	DQ47	125	DQ26	126	DQ58
55	VSS	56	VSS	127	DQ27	128	DQ59
57	NC	58	NC	129	VDD	130	VDD
59	NC	60	NC	131	DQ28	132	DQ60
61	CLK0	62	CKE0	133	DQ29	134	DQ61
63	VDD	64	VDD	135	DQ30	136	DQ62
65	RAS#	66	CAS#	137	DQ31	138	DQ63
67	WE#	68	CKE1	139	VSS	140	VSS
69	CS0#	70	A12	141	SDA	142	SCL
71	CS1#	72	A13*	143	VDD	144	VDD

These pins are not used in this module.



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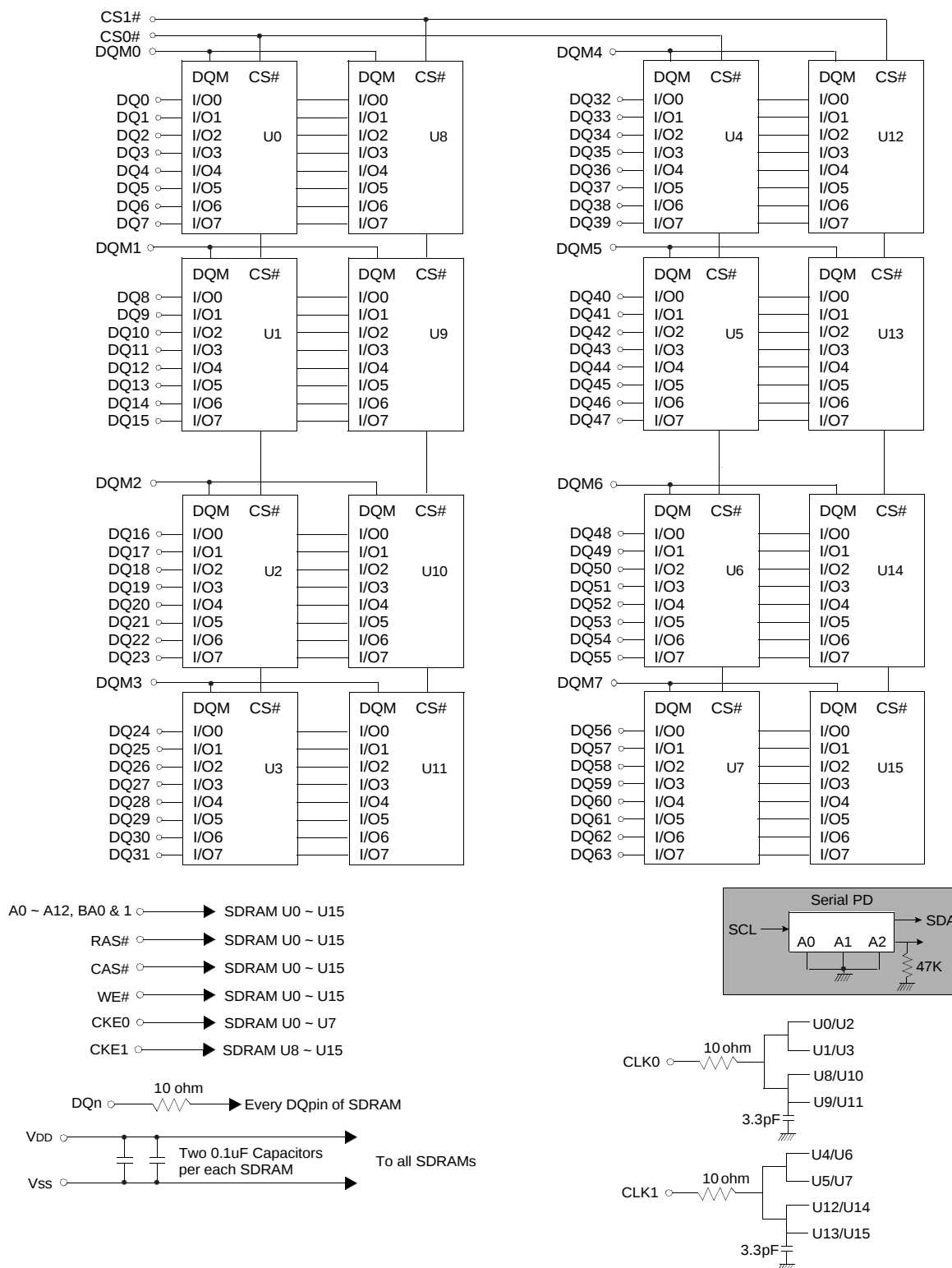
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Functional Block Diagram





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Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V _{IN} , V _{OUT}	-1.0 ~ 4.6	V
Voltage on VDD supply relative to Vss	VDD, VDDQ	-1.0 ~ 4.6	V
Storage temperature	T _{STG}	-55 ~ +150	°C
Power dissipation	P _D	16	W
Short circuit current	I _{OS}	50	mA

Note: Permanent device damage may occur if "ABSOLUTE MAXIMUM RATINGS" are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

Recommended DC Operating Conditions (TA = 0°C to +70°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Supply voltage	VDD, VDDQ	3.0	3.3	3.6	V	
Input high voltage	V _{IH}	2.0	3.0	VDDQ+0.3	V	1
Input low voltage	V _{IL}	-0.3	0	0.8	V	2
Output high voltage	V _{OH}	2.4	-	-	V	I _{OH} = -2mA
Output low voltage	V _{OL}	-	-	0.4	V	I _{OL} = 2mA
Input leakage current (Inputs)	I _{IL}	-5	-	5	uA	3

Notes: 1. V_{IH} (max) = 5.6V AC. The overshoot voltage duration is ≤ 3ns.
2. V_{IL} (min) = 2.0V AC. The undershoot voltage duration is ≤ 3ns.
3. Any input 0V ≤ V_{IN} ≤ VDDQ.

Capacitance (TA = 25°C, f = 1MHz, VDD = 3.3V)

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0 ~ A12, BA0 ~ BA1)	C _{IN1}	44	64.8	pF
Input capacitance (RAS#, CAS#, WE#)	C _{IN2}	44	64.8	pF
Input capacitance (CKE0, CKE1)	C _{IN3}	24	34.4	pF
Input capacitance (CLK0, CLK1)	C _{IN4}	24	32	pF
Input capacitance (CS0#, CS1#)	C _{IN5}	24	34.4	pF
Input capacitance (DQM0 ~ DQM7)	C _{IN6}	9	11.6	pF
Data input/output capacitance (DQ0 ~ DQ63)	C _{OUT}	12	16	pF

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DC Characteristics (Recommended operation condition unless otherwise noted, $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

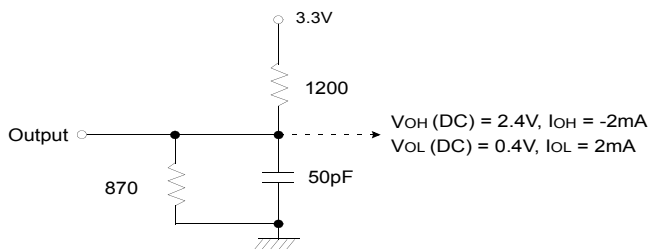
Parameter	Symbol	Test Condon	Version	Unit	Note
			-GA		
Operating current (One bank active)	I _{CC1}	Burst length = 1 trc >= trc(min) I _{OL} = 0 mA	640	mA	1
Precharge standby current in power-down mode	I _{CC2}	CKE <= V _{IL} (max), t _{CC} = 15ns	32	mA	
Active standby current in non power-down mode (One bank active)	I _{CC3}	CKE >= V _{IH} (min), CS# >= V _{IH} (min), t _{CC} = 10ns Input signals are changed one time during 20ns	80	mA	
Operating current (Burst mode)	I _{CC4}	I _{OL} = 0 mA Page burst 2 Banks actived t _{CCD} = 2CLKs	456	mA	1
Refresh current	I _{CC5}	trc >= trc(min)	1136	mA	2
Self refresh current	I _{CC6}	CKE <= 0.2V	48	mA	

Note: IDD specification is based on Qimonda F-die components.

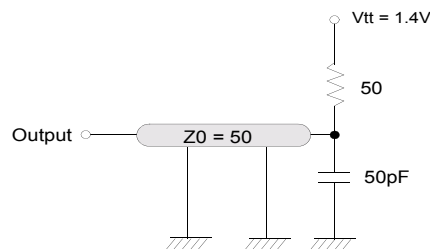
1. Measured with outputs open.
2. Refresh period is 64ms.

AC Operating Test Conditions (V_{DD} = 3.3V, $T_A = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Parameter	Value	Unit
AC input levels (V _{IH} /V _{IL})	2.4/0.4	V
Input timing measurement reference level	1.4	V
Input rise and fall time	tr/tf = 1/1	ns
Output timing measurement reference level	1.4	V
Output load condition	See Fig.2	



(Fig. 1) DC output load circuit



(Fig. 2) AC output load circuit

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Operating AC Parameter

Parameter	Symbol	-GA		Unit	Note ^{1, 2, 3}
		Min.	Max.		
Clock and Clock Enable					
Clock Frequency	t_{CK}	7.5	-	ns	CL3
Access Time from Clock	t_{AC}	-	5.4	ns	CL3 _{3, 4, 5}
Clock High Pulse Width	t_{CH}	2.5	-	ns	
Clock Low Pulse Width	t_{CL}	2.5	-	ns	
Transition time	t_T	0.3	1.2	ns	
Setup and Hold Times					
Input Setup Time	t_{IS}	1.5	-	ns	6
Input Hold Time	t_{IH}	0.8	-	ns	6
CKE Setup Time	t_{CKS}	1.5	-	ns	6
CKE Hold Time	t_{CKH}	0.8	-	ns	6
Mode Register Set-up to Active delay	t_{RSC}	-	-	t_{CK}	
Power Down Mode Entry Time	t_{SB}	0	7	ns	
Common Parameters					
Row to Column Delay Time	t_{RCD}	20	-	ns	7
Row Precharge Time	t_{RP}	20	-	ns	7
Row Active Time	t_{RAS}	44	120k	ns	7
Row Cycle Time	t_{RC}	66	-	ns	7
Row Cycle Time during Auto Refresh	t_{RFC}	66	-	ns	
Activate(a) to Activate(b) Command period	t_{RRD}	15	-	ns	7
CAS(a) to CAS(b) Command period	t_{CCD}	1	-	t_{CK}	
Refresh Cycle					
Refresh Period (8192 cycles)	t_{REF}	-	64	ms	
Self Refresh Exit Time	t_{SREX}	-	-	t_{CK}	
Data Out Hold Time	t_{OH}	3	-	ns	3, 5
Read Cycle					
Data Out to Low Impedance Time	t_{LZ}	1	-	ns	
Data Out to High Impedance Time	t_{HZ}	-	5.4	ns	
DQM Data Out Disable Latency	t_{DQZ}	-	2	t_{CK}	

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Operating AC Parameter (cont')

Parameter	Symbol	-GA		Unit	Note ^{1, 2, 3}
		Min.	Max.		
Write Cycle					
Last Data Input to Precharge (Write without Auto Precharge)	t_{WR}	15	-	ns	8
Last Data Input to Activate(Write with Auto Precharge)	$t_{DAL(min.)}$	-	5	t_{CK}	9
DQM Write Mask Latency	t_{DQM}	0	-	t_{CK}	

NOTE:

- 1) $T_A = 0$ to $70\text{ }^{\circ}\text{C}$; $V_{SS} = 0\text{ V}$; V_{DD} , $V_{DDQ} = 3.3\text{ V} \pm 0.3\text{ V}$, $t_T = 1\text{ ns}$
- 2) For proper power-up see the operation section of this data sheet.
- 3) AC timing tests for LV-TTL versions have $V_{IL} = 0.4\text{ V}$ and $V_{IH} = 2.4\text{ V}$ with the timing referenced to the 1.4 V crossover point. The transition time is measured between V_{IH} and V_{IL} . All AC measurements assume $t_T = 1\text{ ns}$ with the AC output load circuit shown in figure below. Specified t_{AC} and t_{OH} parameters are measured with a 50 pF only, without any resistive termination and with an input signal of 1V / ns edge rate between 0.8 V and 2.0 V.
- 4) If clock rising time is longer than 1 ns, a time $(t_T/2 - 0.5)\text{ ns}$ has to be added to this parameter.
- 5) Access time from clock t_{ac} is 4.6 ns for PC133 components with no termination and 0 pF load, Data out hold time t_{oh} is 1.8 ns for PC133 components with no termination and 0 pF load.
- 6) If t_T is longer than 1 ns, a time $(t_T - 1)\text{ ns}$ has to be added to this parameter.
- 7) These parameter account for the number of clock cycles and depend on the operating frequency of the clock, as follows: the number of clock cycles = specified value of timing period (counted in fractions as a whole number)
- 8) It is recommended to use two clock cycles between the last data-in and the precharge command in case of a write command without Auto-Precharge. One clock cycle between the last data-in and the precharge command is also supported, but restricted to cycle times t_{ck} greater or equal the specified t_{WR} value, where t_{ck} is equal to the actual system clock time.
- 9) When a Write command with Auto Precharge has been issued, a time of $t_{DAL(min)}$ has to be fulfilled before the next Activate Command can be applied. For each of the terms, if not already an integer, round up to the next highest integer. t_{CK} is equal to the actual system clock time.

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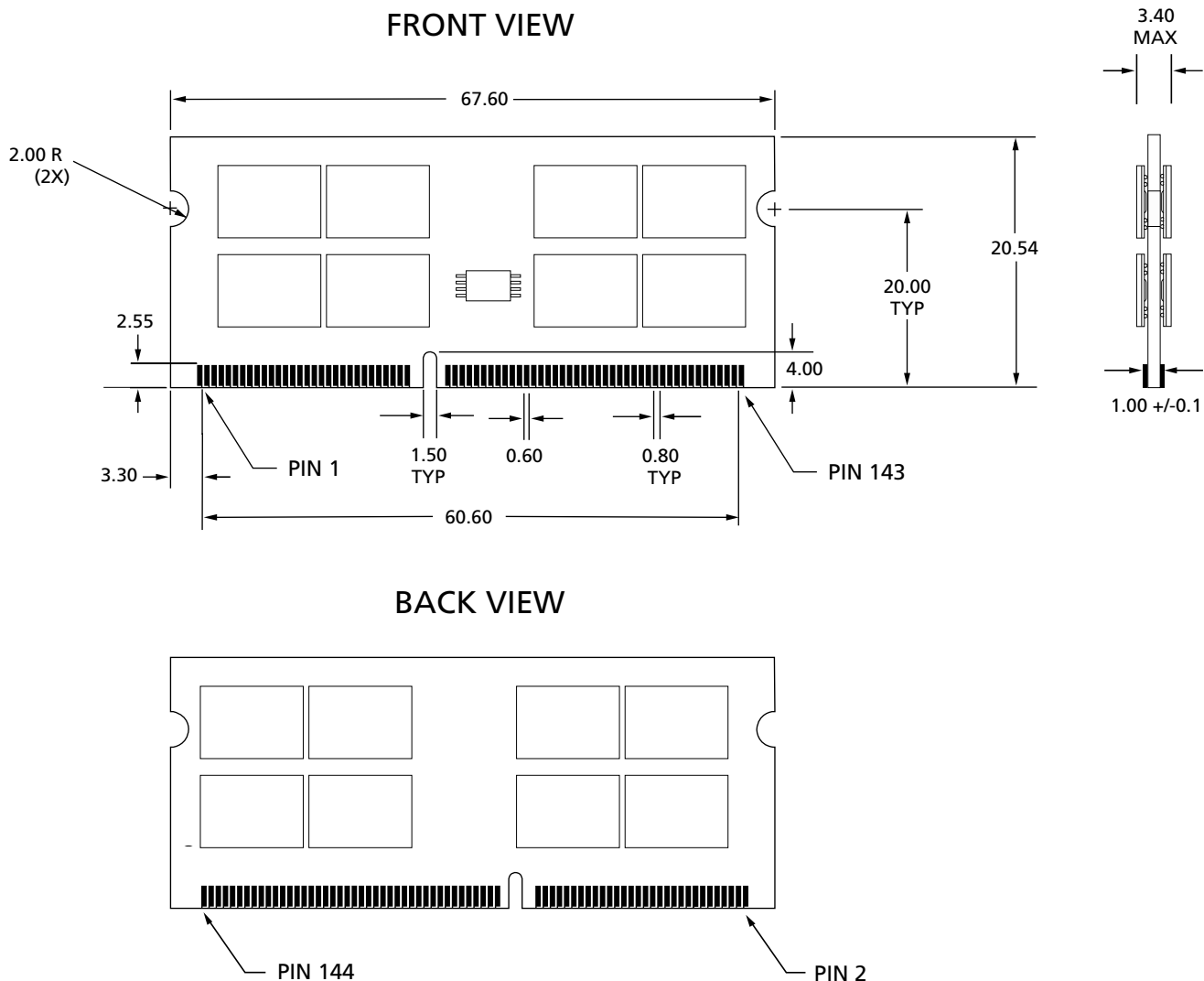
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Package Dimensions



Note: 1. All dimension are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
05/16/2010	1.0	All	Spec released