

Product Specifications		
PART NO.:	VL395T5160A-E6M	REV: 1.1

General Information

4GB 512Mx72 DDR2 SDRAM ECC FULLY BUFFERED DIMM (FBDIMM) 240-PIN

Description

The VL395T5160A is a 512Mx72 DDR2 SDRAM high density Fully buffered DIMM (FBDIMM). This memory module consists of thirty-six CMOS 256Mx4 bit with 8 banks DDR2 synchronous DRAMs in BGA packages, an AMB chip in BGA packages, and a 2K EEPROM in an 8-pin MLF package. This module is a 240-pin fully buffered, dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

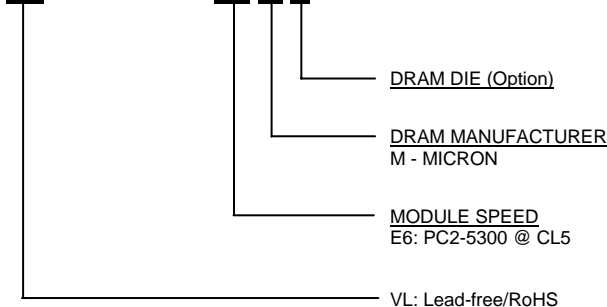
- 240-pin, fully buffered, dual in-line memory module (FBDIMM)
- Fast data transfer rate: PC2-5300
- 3.2Gb/s, 4.0Gb/s
- Supports ECC error detection and correction
- VDD = VDDQ = 1.8V for DDR2 SDRAM
- VDDSPD = 1.7V to 3.6V
- VCC = 1.5V for advance memory buffer (AMB)
- Buffer interface with high-speed differential point-to-point link at 1.5V
- Channel error detection & reporting
- Channel fail over mode support
- Serial presence detect with EEPROM
- 8 banks
- Posted CAS
- Programmable CAS# latency: 5 (DDR2-667)
- Automatic DDR2 DRAM bus and channel calibration
- MBIST and IBIST Test functions
- Hot add-on and Hot Remove Capability
- Transparent mode for DRAM test support
- Gold edge contacts
- Lead-free, RoHS compliant
- Supports 95°C operation with 2X refresh ($t_{REFI} = 7.8\mu s$ at or below 85°C; $t_{REFI} = 3.9\mu s$ above 85°C)
- PCB: Height 30.35mm (1.195"), double sided components

Pin Description

Pin Name	Function
SCK	System clock input, positive line
SCK#	System clock input, negative line
PN[13:0]	Primary northbound data, positive lines
PN#[13:0]	Primary northbound data, negative lines
PS[9:0]	Primary southbound data, positive lines
PS#[9:0]	Primary southbound data, negative lines
SN[13:0]	Secondary northbound data, positive lines
SN#[13:0]	Secondary northbound data, negative lines
SS[9:0]	Secondary southbound data, positive lines
SS#[9:0]	Secondary southbound data, negative lines
SCL	Serial presence detect (SPD) clock input
SDA	SPD data input/ output
SA[2:0]	SPD address inputs, also used to select the FBDIMM number in the AMB
VID[1:0]	Voltage ID: These pins must be unconnected for DDR2-based FBDIMMs; VID[0] is VDD value: OPEN = 1.8V, GND = 1.5V; VID[1] is VCC value: OPEN = 1.5V, GND = 1.2V
RESET#	AMB reset signal
VCC	AMB core power and AMB channel interface power (1.5V)
VDD	DRAM power and AMB DRAM I/O power (1.8V)
VTT	DRAM address/command/clock termination power (VDD/2)
VDDSPD	SPD power
VSS	Ground
DNU/M_Test	The DNU/M_Test pin provides an external connection on R/Cs AD for testing the margin of VREF, which is produced by a voltage divider on the module. It is not intended to be used in normal system operation and must not be connected (DNU) in a system. This test pin may have other features on future card designs and will be included in this specification at that time.

Order Information:

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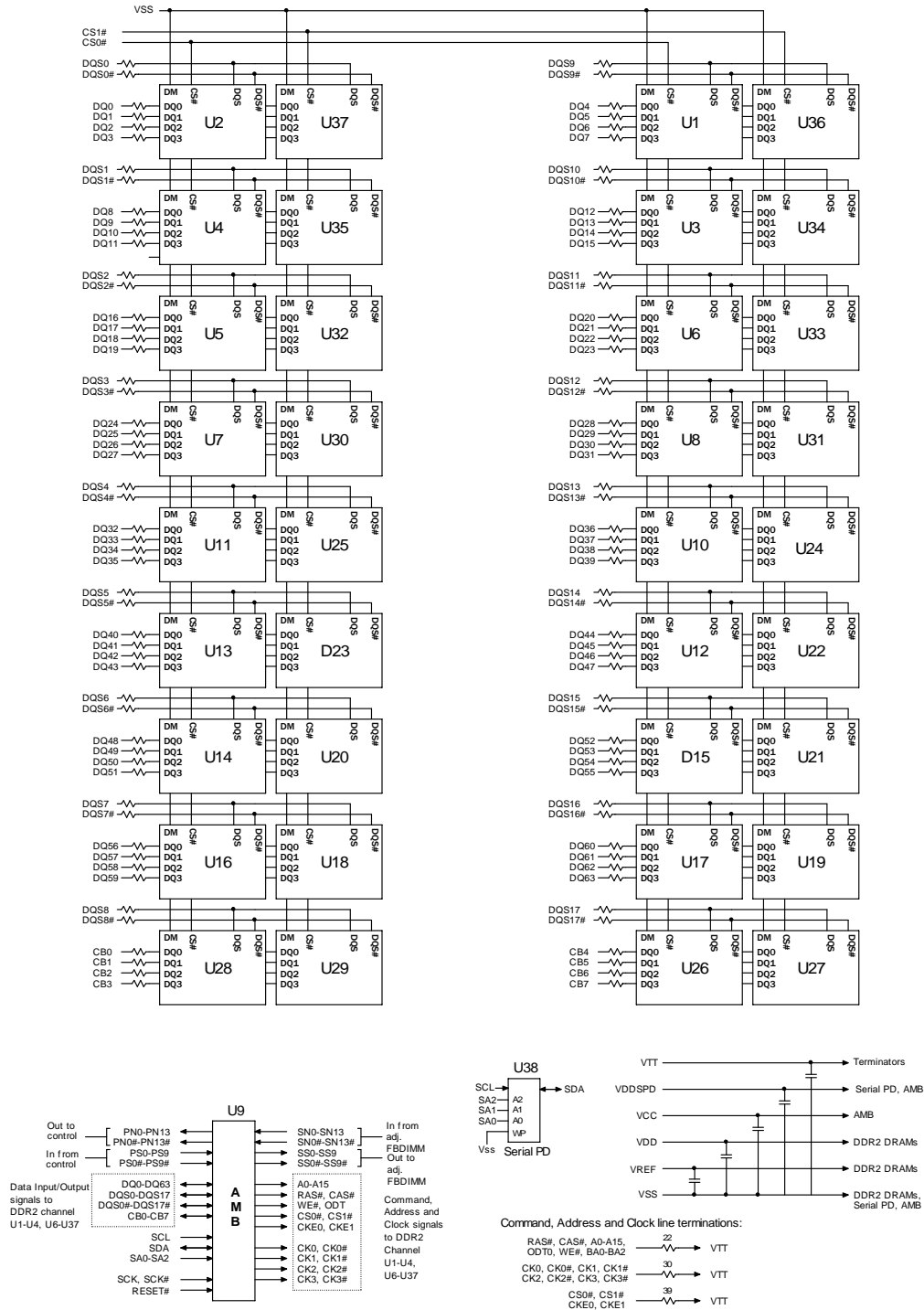
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Pin Configuration

240-PIN DDR2 FBDIMM FRONT								240-PIN DDR2 FBDIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VDD	31	PN3	61	PN9#	91	PS9#	121	VDD	151	SN3	181	SN9#	211	SS9#
2	VDD	32	PN3#	62	VSS	92	VSS	122	VDD	152	SN3#	182	VSS	212	VSS
3	VDD	33	VSS	63	PN10	93	PS5	123	VDD	153	VSS	183	SN10	213	SS5
4	VSS	34	PN4	64	PN10#	94	PS5#	124	VSS	154	SN4	184	SN10#	214	SS5#
5	VDD	35	PN4#	65	VSS	95	VSS	125	VDD	155	SN4#	185	VSS	215	VSS
6	VDD	36	VSS	66	PN11	96	PS6	126	VDD	156	VSS	186	SN11	216	SS6
7	VDD	37	PN5	67	PN11#	97	PS6#	127	VDD	157	SN5	187	SN11#	217	SS6#
8	VSS	38	PN5#	68	VSS	98	VSS	128	VSS	158	SN5#	188	VSS	218	VSS
9	VCC	39	VSS	69	VSS	99	PS7	129	VCC	159	VSS	189	VSS	219	SS7
10	VCC	40	PN13	70	PS0	100	PS7#	130	VCC	160	SN13	190	SS0	220	SS7#
11	VSS	41	PN13#	71	PS0#	101	VSS	131	VSS	161	SN13#	191	SS0#	221	VSS
12	VCC	42	VSS	72	VSS	102	PS8	132	VCC	162	VSS	192	VSS	222	SS8
13	VCC	43	VSS	73	PS1	103	PS8#	133	VCC	163	VSS	193	SS1	223	SS8#
14	VSS	44	NC	74	PS1#	104	VSS	134	VSS	164	NC	194	SS1#	224	VSS
15	VTT	45	NC	75	VSS	105	NC	135	VTT	165	NC	195	VSS	225	NC
16	VID1	46	VSS	76	PS2	106	NC	136	VID0	166	VSS	196	SS2	226	NC
17	RESET#	47	VSS	77	PS2#	107	VSS	137	DNU/M_Test	167	VSS	197	SS2#	227	VSS
18	VSS	48	PN12	78	VSS	108	VDD	138	VSS	168	SN12	198	VSS	228	SCK
19	NC	49	PN12#	79	PS3	109	VDD	139	NC	169	SN12#	199	SS3	229	SCK#
20	NC	50	VSS	80	PS3#	110	VSS	140	NC	170	VSS	200	SS3#	230	VSS
21	VSS	51	PN6	81	VSS	111	VDD	141	VSS	171	SN6	201	VSS	231	VDD
22	PN0	52	PN6#	82	PS4	112	VDD	142	SN0	172	SN6#	202	SS4	232	VDD
23	PN0#	53	VSS	83	PS4#	113	VDD	143	SN0#	173	VSS	203	SS4#	233	VDD
24	VSS	54	PN7	84	VSS	114	VSS	144	VSS	174	SN7	204	VSS	234	VSS
25	PN1	55	PN7#	85	VSS	115	VDD	145	SN1	175	SN7#	205	VSS	235	VDD
26	PN1#	56	VSS	86	NC	116	VDD	146	SN1#	176	VSS	206	NC	236	VDD
27	VSS	57	PN8	87	NC	117	VTT	147	VSS	177	SN8	207	NC	237	VTT
28	PN2	58	PN8#	88	VSS	118	SA2	148	SN2	178	SN8#	208	VSS	238	VDDSPD
29	PN2#	59	VSS	89	VSS	119	SDA	149	SN2#	179	VSS	209	VSS	239	SA0
30	VSS	60	PN9	90	PS9	120	SCL	150	VSS	180	SN9	210	SS9	240	SA1

Function Block Diagram





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FBDIMM/DDR2 SDRAM Addressing	
Parameter	4GB
Refresh count	8K
Device bank addressing	8 (BA0 - BA2)
Device page size per bank	1KB
Device configuration	1Gb(256Meg x 4)
Row addressing	16K (A0 - A13)
Column Addressing	1K (A0 - A9, A11)
Module rank addressing	2 (CS0#, CS1#)

Absolute Maximum Ratings				
Symbol	Parameter	MIN	MAX	Unit
V _{IN} , V _{OUT}	Voltage on any pin relative to V _{SS}	-0.3	1.75	V
V _{CC}	Voltage on V _{CC} pin relative to V _{SS}	-0.3	1.75	V
V _{DD}	Voltage on V _{DD} pin relative to V _{SS}	-0.5	2.3	V
V _{TT}	Voltage on V _{TT} pin relative to V _{SS}	-0.5	2.3	V
T _{STG}	Storage temperature	-55	150	°C
T _{CASE}	DDR2 SDRAM device operating temperature (ambient)	0	85	°C
		85	95	
T _j	AMB device operating temperature (ambient)	0	110	°C

Note:
 Stress greater than those listed may cause permanent damage to the device. This is a stress rating only, and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may adversely affect reliability.

DDR2 SDRAMs OF FBDIMM should require this specification				
Symbol	Parameter	DRAM	Unit	
t _{REFI}	0°C <= TCASE <= 85°C	Average periodic refresh interval	7.8	us
	85°C < TCASE <= 95°C		3.9	us



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Input DC Operating Conditions						
Parameter	Symbol	Min	Nom	Max	Unit	Notes
AMB supply voltage	VCC	1.455	1.50	1.54	V	
DDR2 SDRAM supply voltage	VDD	1.7	1.8	1.9	V	
Termination voltage	VTT	0.48xVDD	0.50xVDD	0.52xVDD	V	
EEPROM supply voltage	VDDSPD	1.7	-	3.6	V	
SPD Input HIGH (logic 1) voltage	VIH(DC)	2.1	-	VDDSPD	V	1
SPD Input LOW (logic 0) voltage	VIL(DC)	-	-	0.8	V	1
RESET Input HIGH (Logic 1) voltage	VIH(DC)	1.0	-	-	V	2
RESET Input LOW (Logic 0) voltage	VIL(DC)	-	-	0.5	V	1
Leakage Current (RESET)	IL	-90	-	90	uA	2
Leakage Current (link)	IL	-5	-	5	uA	3

Timing Parameters						
Parameter	Symbol	Min	Typ	Max	Unit	Notes
Electrical idle (EI) assertion pass-through timing	tEI Propagate	-	-	4	CK	
EI de-assertion pass-through timing	tEID	-	-	Bitlock	CK	2
EI assertion duration	tEI	100	-	-	CK	1,2
FBDIMM command to DDR@ clock out that latches command	-	-	8.1	-	ns	3
FBDIMM command to DDR2 WRITE	-	-	TBD	-	ns	
DDR2 READ to FBDIMM (last FBDIMM)	-	-	5.0	-	ns	4
Resample pass-through time	-	-	1.075	-	ns	
Resynch pass-through time	-	-	2.075	-	ns	
Bitlock interval	t Bitlock	-	-	119	frames	1
Framelock interval	t Framelock	-	-	154	frames	1



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Power Specification				
(VDD Max = 1.900V, VCC Max = 1.54V)				
Condition	Symbol	E6 (DDR2-667)	Notes	Unit
Idle Current, single or last FBDIMM: L0 state, idle (0 BW); primary channel enabled, secondary channel disabled, CKE HIGH; command and address lines stable, DDR2 SDRAM clock active.	Icc_IDLE_0	2600	@1.5V	mA
	Idd_IDLE_0	2340	@1.8V	mA
Idd_Idle_0 Total Power	P_IDE_0	8.5		W
Idle current, first FBDIMM: L0 state, idle (0 BW); primary and secondary channels enabled, CKE HIGH; command and address lines stable, DDR2 SDRAM clock active.	Icc_IDLE_1	3400	@1.5V	mA
	Idd_IDLE_1	2340	@1.8V	mA
Idd_Idle_1 Total Power	P_IDE_1	9.8		W
Active Power: L0 state; 50% DDR2 SDRAM BW, 67% READ, 33% WRITE; primary and secondary channels enabled, CKE HIGH; DDR2 SDRAM clock active.	Icc_ACTIVE_1	3900	@1.5V	mA
	Idd_ACTIVE_1	3995	@1.8V	mA
Idd_Active_1 Total Power	P_ACTIVE_1	13.7		
Active Power, data pass-through: L0 state; 50% DDR2 SDRAM BW to downstream FBDIMM, 67% READ, 33% WRITE; primary and secondary channels enabled; command and address lines stable, CKE HIGH; DDR2 SDRAM clock active.	Icc_ACTIVE_2	3700	@1.5V	mA
	Idd_ACTIVE_2	2340	@1.8V	mA
Idd_Active_2 Total Power	P_ACTIVE_2	10.3		W
Training: Primary and secondary channels enabled; 100% toggle on all channel lanes; DDR2 SDRAM devices idle (0 BW); CKE HIGH, command and address lines stable; DDR2 SDRAM clock active.	Icc_Training (for AMB spec, Not in SPD)	4000	@1.5V	mA
	Idd_Training (for AMB spec, Not in SPD)	2340	@1.8V	mA
Idd_Training Total Power	P_TRAINING	10.7		W
Note: Power specification is based on Micron components. Other DRAM Manufacturers specification may be different.				

VTT Currents				
Description	Symbol	Typ	Max	Unit
Idle current, DDR2 SDRAM device power down	ITT1	500	700	mA
Active power, 50% DDR2 SDRAM BW	ITT2	500	700	mA

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Reference Clock Input Specifications

Parameter	Symbol	Values		Unit	Note
		MIN	MAX		
Reference clock frequency @3.2 Gb/s (nominal 133.33 MHz)	fRefclk-3.2	126.67	133.40	MHz	1, 2
Reference clock frequency @4.0 Gb/s (nominal 166.67 MHz)	fRefclk-4.0	158.33	166.75	MHz	1, 2
Rise time, fall time	T _{SCK-RISE} , T _{SCK-FALL}	175	700	ps	3
Voltage high	V _{SCK-HIGH}	660	850	mV	
Voltage low	V _{SCK-LOW}	-150		mV	
Absolute crossing point	V _{CROSS-ABS}	250	550	mV	4
Relative crossing	V _{CROSS-REL}	calculated	calculated		4, 5
Percent mismatch between rise and fall times	T _{SCK-RISE-FALL-MATCH}	-	10	%	
Duty cycle of reference clock	T _{SCK-DUTYCLE}	40	60	%	
Clock leakage current	I _{ICK}	-10	10	uA	6, 7
Clock input capacitance	C _{ICK}	0.5	2	pF	7
Clock input capacitance delta	C _{LCK(D)}	-0.25	0.25	pF	8
Transport delay	T ₁		5	ns	9, 10
Phase jitter sample size	NSAMPLE	10 ¹⁶		Periods	11
Reference clock jitter, filtered	T _{REF-JITTER}		40	ps	12, 13
Reference clock deterministic jitter	T _{REF-DJ}		TBD	ps	

Notes:

1. 133 MHz for PC2-4200 and 166MHz for PC2-5300.
2. Measured with SSC disabled.
3. Measured differentially through the range of 0.175V to 0.525V.
4. The crossing point must meet the absolute and relative crossing point specification simultaneously.
5. V_{CROSS_REL(MIN)} and V_{CROSS_REL(MAX)} are derived using the following calculation : Min = 0.5(V_{HAVG} - 0.710) + 0.250; AND Max = 0.5(V_{HAVG} - 0.710) + 0.550, where V_{HAVG} is the average of V_{SCK-HIGHM}.
6. Measured with a single-ended input voltage of 1V.
7. Applies to reference clocks SCK and SCK#.
8. Difference between SCK and SCK# input.
9. T₁ = [T_{datapath-Tclockpath}] (excluding PLL loop delays). This parameter is not a direct clock output parameter but indirectly determines the clock output parameter T_{REF-JITTER}.
10. The net transport delay is the difference in time of flight between associated data and clock paths. The data path is defined from the reference clock source, through the TX, to data arrival at the data sampling point in the RX. The clock path is defined from the reference clock source to clock arrival at the same sampling point. The path delays are caused by copper trace routes, on-chip routing, on-chip buffering, etc. They include the time-of flight of interpolators or other clock adjustment mechanisms. They do not include the phase delays caused by finite PLL loop bandwidth because these delays are modeled by the PLL transfer functions.
11. Direct measurement of phase jitter records over 1016 periods is impractical. It is expected that the jitter will be measured over a smaller, yet statistically significant, sample size and the total jitter at 10¹⁶ samples extrapolated from an estimate of the sigma of the random jitter components.
12. Measured with SCC enabled on reference clock generator.
13. As measured after the phase jitter filter. This number is separate from the receiver jitter budget that is defined by the TRXTotal - MIN parameters.

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Differential Transmitter Output Specifications

Parameter	Symbol	Values		Unit	Comments
		MIN	MAX		
Differential peak-to-peak output voltage for large voltage swing	V _{TX-DIFFP-P-L}	900	1300	mV	EQ1, Note1
Differential peak-to-peak output voltage for regular voltage swing	V _{TX-DIFFP-P-R}	800	-	mV	EQ1, Note1
Differential peak-to-peak output voltage for small voltage swing	V _{TX-DIFFP-P-S}	520	-	mV	EQ1, Note1
DC common code output voltage for large voltage swing	V _{TX-CM-L}	-	375	mV	EQ2, Note1
DC common code output voltage for small voltage swing	V _{TX-CM-S}	135	280	mV	EQ2, Note1,2
De-emphasized differential output voltage ratio for -3.5 dB de-emphasis	V _{TX-DE-3.5-Ratio}	-3.0	-4.0	dB	1,3,4
De-emphasized differential output voltage ratio for -6.0 dB de-emphasis	V _{TX-DE-6.0-Ratio}	-5.0	-7.0	dB	1,2,3
AC peak-to-peak common mode output voltage for large swing	V _{TX-CM-ACP-P-L}	-	90	mV	EQ7, Note1,5
AC peak-to-peak common mode output voltage for regular swing	V _{TX-CM-ACP-P-R}	-	80	mV	EQ7, Note1,5
AC peak-to-peak common mode output voltage for small swing	V _{TX-CM-ACP-P-S}	-	70	mV	EQ7, Note1,5
Maximum single-ended voltage in EI condition DC + AC	V _{TX-IDLE-SE}	-	50	mV	6
Maximum single-ended voltage in EI condition DC + AC	V _{TX-IDLE-SE-DC}	-	20	mV	6
Maximum peak-to-peak differential voltage in EI condition	V _{TX-IDLE-DIFFP-P}	-	40	mV	
Single-ended voltage (w. r. t. VSS) on D+/D-	V _{TX-SE}	-75	750	mV	1,7
Minimum TX eye width , 3.2 and 4.0 Gb/s	T _{TX-EYE-MIN}	0.7	-	UI	1,8
Minimum TX eye width 4.8 Gb/s	T _{TX-EYE-MIN4.8}	TBD	-	UI	1,8
Maximum TX deterministic jitter, 3.2 and 4.8 Gb/s	T _{TX-DJ-DD}	-	0.2	UI	1,8,9
Maximum TX deterministic jitter, 4.8 Gb/s	T _{TX-DJ-DD-4.8}	-	TBD	UI	1,8,9
Instantaneous pulse width	T _{TX-PULSE}	0.85	-	UI	10
Differential TX output rise/fall time	T _{TX-RISE} T _{TX-FALL}	30	90	ps	20-80% voltage, Note1
Mismatch between rise and fall times	T _{TX-RF-MISMATCH}	-	20	ps	
Differential return loss	RL _{TX-DIFF}	8	-	dB	1 GHz-2.4 GHz, Note11
Common mode return loss	RL _{TX-CM}	6	-	dB	1 GHz-2.4 GHz, Note11
Transmitter termination impender	R _{TX}	41	55	Ohm	12
D+/D-TX impedance difference	R _{TX-MATCH-DC}	-	4	%	EQ 4; Boundaries are applied separately to high and low output voltage states
Lane-to lane skew at TX	L _{TX-SKEW1}	-	100+3UI	ps	13,15
Lane-to lane skew at TX	L _{TX-SKEW2}	-	100=2UI	ps	14,15

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Differential Receiver Input Specifications

Parameter	Symbol	Values		Unit	Comments
		MIN	MAX		
Differential peak-to-peak input voltage for large voltage swing	VRX-DIFFP-P	170	TBD	mV	EQ5, Note1
Maximum single-ended voltage in EI condition	VRX-IDLE-SE	-	75	mV	2,3
Maximum single-ended voltage in EI condition (DC only)	VRX-IDLE-SE-DC	-	50	mV	2,3
Maximum peak-to-peak differential voltage in EI condition	VRX-IDLE-DIFFP-P	-	65	mV	3
Single-ended voltage (w. r. t. VSS) on D+/D-	VRX-SE	-300	900	mV	4
Single-pulse peak differential input voltage	VRX-DIFF-PULSE	85	-	mV	4,5
Amplitude ratio between adjacent symbols	VRX-DIFF-ADJ-RATIO	-	TBD		4,6
Maximum RX inherent timing error, 3.2 and 4.0 Gb/s	TRX-TJ-MAX	-	0.4	UI	4,7,8
Maximum RX inherent deterministic timing error, 3.2 and 4.8 Gb/s	TRX-TJ-MAX4.8	-	TBD	UI	4,7,8
Single-pulse width as zero-voltage crossing	VRX-DJ-DD	-	0.3	UI	4,7,8,9
Single-pulse width at minimum-level crossing	VRX-DJ-DD-4.8	-	TBD	UI	4,7,8,9
Differential RX input rise/fall time	TRX-PW-ZC	0.55	-	UI	4,5
Common mode input voltage	TRX-PW-ML	0.2	-	UI	4,5
Differential RX output rise/fall time	TRX-RISE TRX-FALL	50	-	ps	20-80% voltage
Common mode of input voltage	VRX-CM	120	400	mV	EQ6, Note1, 10
AC peak-to-peak common mode of input voltage	VRX-CM-ACP-P	-	270	mV	EQ7, Note1
Ratio of VRX-CM-ACP-P to minimum VRX-DIFFP-P	VRX-CM-EH-RATOP	-	45	%	11
Differential return loss	RLRX-DIFF	9	-	dB	1GHz-2.4 GHz, Note12
Common mode return loss	RLRX-CM	6	-	dB	1GHz-2.4 GHz, Note12
RX termination impedance	RRX	41	55	Ohm	13
D+/D- RX Impedance difference	RRX-MATCH-DC	-	4	%	EQ8
Lane-to lane PCB skew at RX	LRX-PCB-SKEW	-	6	UI	Lane-to-lane skew at the receiver that must be tolerated. Note 14
Minimum RX drift tolerance	TRX-DRIFT	400	-	ps	15
Minimum data tracking 3dB bandwidth	FTRK	0.2	-	MHz	16
Electrical idle entry detect time	TEI-ENTRY-DETECT	-	60	ns	17
Electrical idle exit detect time	TEI-EXIT-DETECT	-	30	ns	
Bit Error Ratio	BER	-	10 ⁻¹²		18

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Notes:

1. Specified at the package pins into a timing and voltage compliant test setup. Note that signal levels at the pad will be lower than at the pin.
2. Single-ended voltages below that value that are simultaneously detected on D+ and D- are interpreted as the Electrical Idle condition. Worst-case margins are determined for the case with transmitter using small voltage swing.
3. Multiple lanes need to detect the EI condition before the device can act upon the EI detection.
4. Specified at the package pins into a timing and voltage compliance test setup.
5. The single-pulse mask provides sufficient symbol energy for reliable RX reception. Each symbol must comply with both the single-pulse mask and the cumulative eyemask.
6. The relative amplitude ratio limit between adjacent symbols prevents excessive inter symbol interference in the RX. Each symbol must comply with the peak amplitude ratio with regard to both the preceding and subsequent symbols.
7. This number does not include the effects of SSC or reference clock jitter.
8. This number includes setup and hold of the Rx sampling flop.
9. Defined as the dual-dirac deterministic timing error.
10. Allows for 15 mV DC offset between transmit and receive devices.
11. The received differential signal must satisfy both this ratio as well as the absolute maximum AC peak-to-peak common mode specification. For example, if VRX-DIFFP-P is 200 mV, the maximum AC peak-to-peak common mode is the lesser of (200 mV*0.45 = 90 mV) and VRX-CM-ACP-P.
12. One of the components that contribute to the deterioration of the return loss is the ESD structure which needs to be carefully designed.
13. The termination small signal resistance; tolerance across voltage from 100 mV to 400 mV shall not exceed +/-5 W with regard to the average of the values measured at 100 mV and at 400 mV for that pin.
14. This number represents the lane-to-lane skew between TX and RX pins and does not include the transmitter output skew from the component of the end-to-end channel skew in the AMB specification.
15. Measured from the reference clock edge to the center of the input eye. This specification must be met across specified voltage and temperature ranges for a single component. Drift rate of change is significantly below the tracking capability of the receiver.
16. This bandwidth number assume the specified minimum data transition density. Maximum jitter at 0.2 MHz is 0.05 UI.
17. The specified time includes the time required to forward the EI entry condition.
18. BER per differential lane.

$$VRX-DIFFP-P = 2 \times [VRX-D+ - VRX-D-] \quad (EQ5)$$

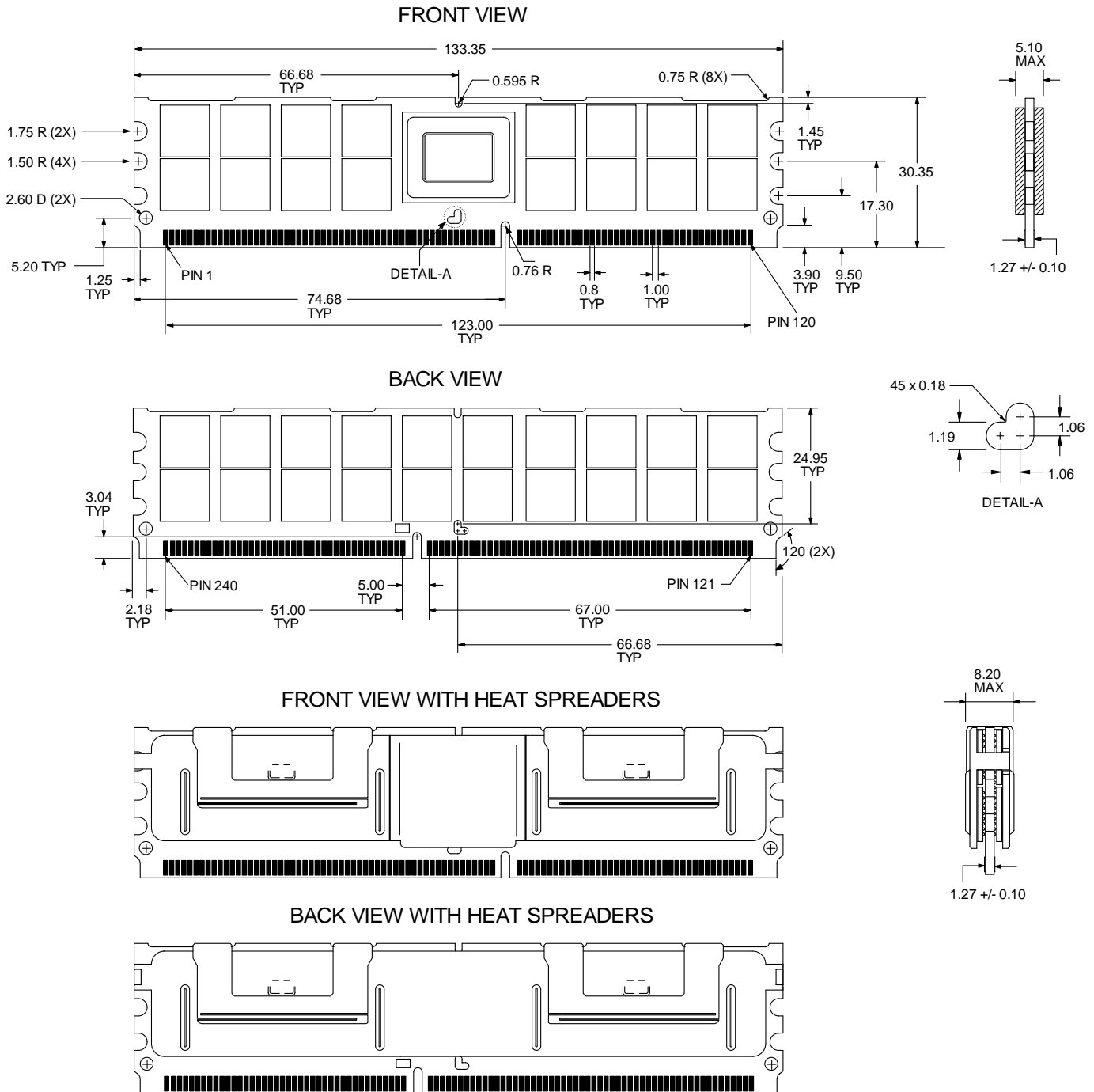
$$(VRX-CM = DC(AVG) \text{ of } [VRX-D+ + VRX-D-] / 2) \quad (EQ6)$$

$$VRX-CM-AC = ((Max[VRX-D+ + VRX-D-] / 2) - (Min[VRX-D+ + VRX-D-] / 2)) \quad (EQ7)$$

$$RRX-MATCH-DC = 2 \times (([RRX-D+ - RRX-D-]) / ([RRX-D+ + RRX-D-])) \quad (EQ8)$$

Product Specifications		
PART NO.:	VL395T5160A-E6M	REV: 1.1

Package Dimensions



Note: 1. All dimension are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
 2. The dimensional diagram is for reference only.



Product Specifications		
PART NO.:	VL395T5160A-E6M	REV: 1.1

Revision History:

Date	Rev.	Page	Changes
07/01/2008	1.0	All	Spec release
12/21/2010	1.1	6	Update Power Specification table