



Product Specifications		
PART NO.:	VL378T2863A-D5M	REV: 1.0

General Information

1GB 128Mx64 DDR2 SDRAM NON-ECC UNBUFFERED DIMM 240-PIN

Description

The VL378T2863A is a 128M x 64 DDR2 SDRAM high density DIMM. This memory module consists of eight CMOS 128Mx8 bit with 8 banks DDR2 Synchronous DRAMs in BGA packages, and a 2K EEPROM in 8-pin TSSOP package. This module is a 240-pin dual in-line memory module and is intended for mounting into a connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR2 SDRAM.

Features

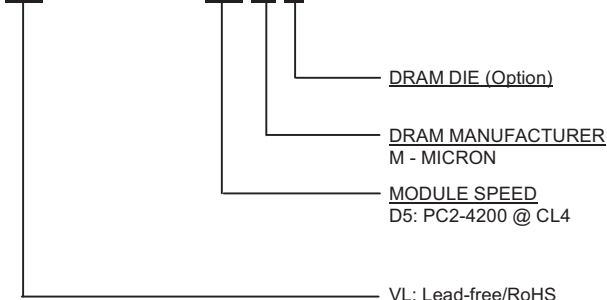
- 240-pin, unbuffered dual in-line memory module (UDIMM)
- Fast data transfer rate: PC2-4200
- VDD = VDDQ = 1.8V
- JEDEC standard 1.8V (SSTL_18 compatible)
- VDDSPD = 1.7V to 3.6V
- Differential data strobe (DQS, DQS#) option
- Four-bit pre-fetch architecture
- DLL aligns DQ and DQS transition with CK
- Nominal and dynamic on-die termination (ODT)
- Programmable CAS# latency: 4 (DDR2-533)
- Write latency = Read latency - 1 tCK
- Programmable burst; length (4, 8)
- Adjustable data-output drive strength
- Auto & self refresh, (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Gold edge contacts
- Lead-free, RoHS compliant
- PCB: Height 30.00mm (1.181”), double sided components

Pin Description

Pin Name	Function
A0~A13	Address Inputs
A10/AP	Address Input/ Autoprecharge
BA0~BA2	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes
DQS0#~DQS7#	Data Strobes Complement
ODT0	On-die Termination Control
CK0, CK0# ~ CK2, CK2#	Clock Input
CKE0	Clock Enables
CS0#	Chip Selects
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply 1.8V +/- 0.1V
VDDQ	I/O Power 1.8V +/- 0.1V
VSS	Ground
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
DM0~DM7	Data Masks
VREF	SSTL_18 Reference Voltage
VDDSPD	SPD Voltage Supply 1.7V to 3.6V
NC	No Connect

Order Information:

VL378T2863A-D5 M X





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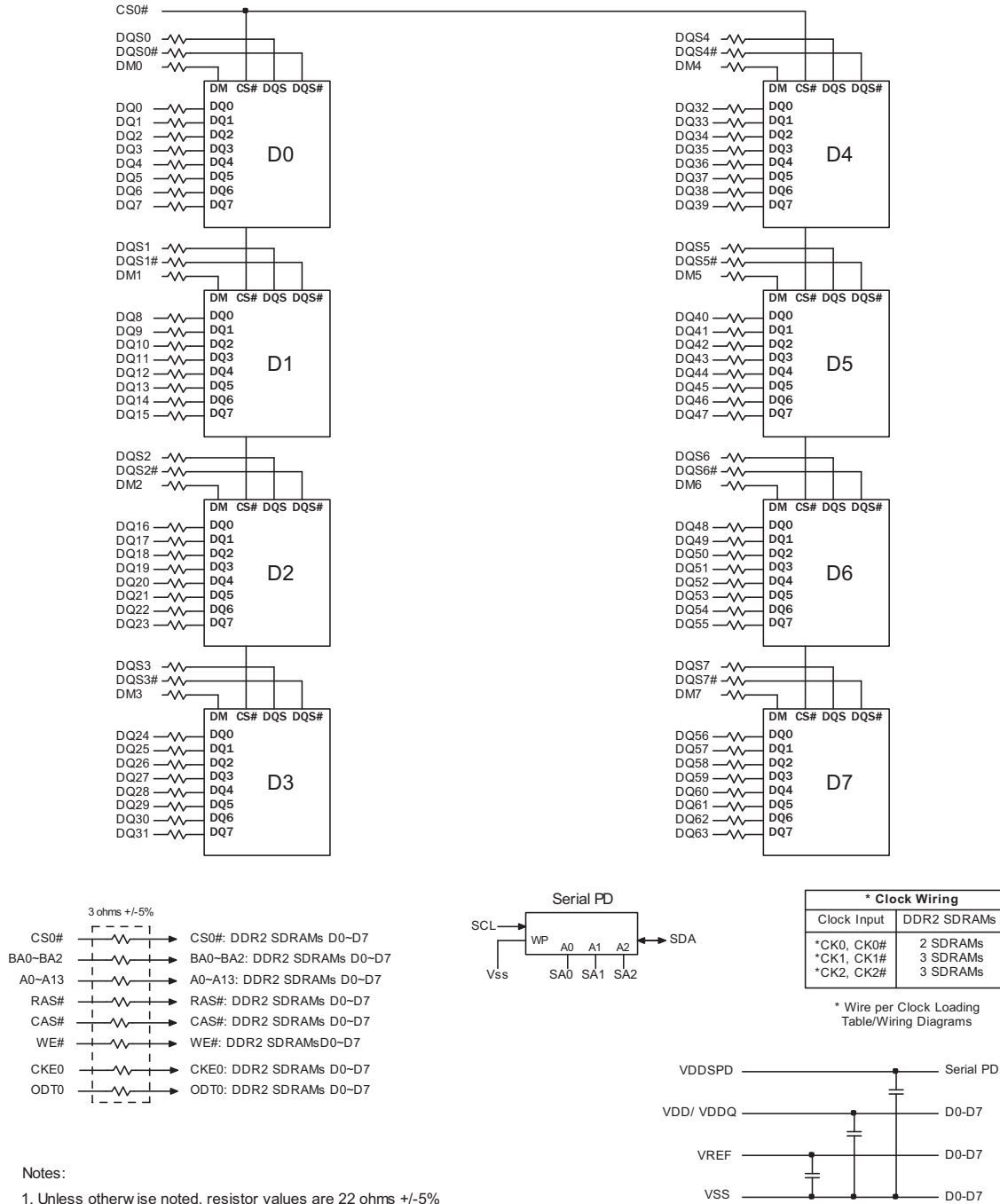
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Pin Configuration

240-PIN DDR2 DIMM FRONT SIDE								240-PIN DDR2 DIMM BACK SIDE							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name		
1	VREF	31	DQ19	61	A4	91	VSS	121	VSS	151	VSS	181	VDDQ	211	DM5
2	VSS	32	VSS	62	VDDQ	92	DQS5#	122	DQ4	152	DQ28	182	A3	212	NC
3	DQ0	33	DQ24	63	A2	93	DQS5	123	DQ5	153	DQ29	183	A1	213	VSS
4	DQ1	34	DQ25	64	VDD	94	VSS	124	VSS	154	VSS	184	VDD	214	DQ46
5	VSS	35	VSS	65	VSS	95	DQ42	125	DM0	155	DM3	185	CK0	215	DQ47
6	DQS0#	36	DQS3#	66	VSS	96	DQ43	126	NC	156	NC	186	CK0#	216	VSS
7	DQS0	37	DQS3	67	VDD	97	VSS	127	VSS	157	VSS	187	VDD	217	DQ52
8	VSS	38	VSS	68	NC	98	DQ48	128	DQ6	158	DQ30	188	A0	218	DQ53
9	DQ2	39	DQ26	69	VDD	99	DQ49	129	DQ7	159	DQ31	189	VDD	219	VSS
10	DQ3	40	DQ27	70	A10/AP	100	VSS	130	VSS	160	VSS	190	BA1	220	CK2
11	VSS	41	VSS	71	BA0	101	SA2	131	DQ12	161	CB4*	191	VDDQ	221	CK2#
12	DQ8	42	CB0*	72	VDDQ	102	NC	132	DQ13	162	CB5*	192	RAS#	222	VSS
13	DQ9	43	CB1*	73	WE#	103	VSS	133	VSS	163	VSS	193	CS0#	223	DM6
14	VSS	44	VSS	74	CAS#	104	DQS6#	134	DM1	164	DM8*	194	VDDQ	224	NC
15	DQS1#	45	DQS8#*	75	VDDQ	105	DQS6	135	NC	165	NC	195	ODT0	225	VSS
16	DQS1	46	DQS8*	76	CS1#*	106	VSS	136	VSS	166	VSS	196	A13	226	DQ54
17	VSS	47	VSS	77	ODT1*	107	DQ50	137	CK1	167	CB6*	197	VDD	227	DQ55
18	RESET#*	48	CB2*	78	VDDQ	108	DQ51	138	CK1#	168	CB7*	198	VSS	228	VSS
19	NC	49	CB3*	79	VSS	109	VSS	139	VSS	169	VSS	199	DQ36	229	DQ60
20	VSS	50	VSS	80	DQ32	110	DQ56	140	DQ14	170	VDDQ	200	DQ37	230	DQ61
21	DQ10	51	VDDQ	81	DQ33	111	DQ57	141	DQ15	171	CKE1*	201	VSS	231	VSS
22	DQ11	52	CKE0	82	VSS	112	VSS	142	VSS	172	VDD	202	DM4	232	DM7
23	VSS	53	VDD	83	DQS4#	113	DQS7#	143	DQ20	173	NC	203	NC	233	NC
24	DQ16	54	BA2	84	DQS4	114	DQS7	144	DQ21	174	NC	204	VSS	234	VSS
25	DQ17	55	NC	85	VSS	115	VSS	145	VSS	175	VDDQ	205	DQ38	235	DQ62
26	VSS	56	VDDQ	86	DQ34	116	DQ58	146	DM2	176	A12	206	DQ39	236	DQ63
27	DQS2#	57	A11	87	DQ35	117	DQ59	147	NC	177	A9	207	VSS	237	VSS
28	DQS2	58	A7	88	VSS	118	VSS	148	VSS	178	VDD	208	DQ44	238	VDDSPD
29	VSS	59	VDD	89	DQ40	119	SDA	149	DQ22	179	A8	209	DQ45	239	SA0
30	DQ18	60	A5	90	DQ41	120	SCL	150	DQ23	180	A6	210	VSS	240	SA1

*: These pins are not used in this module.

Function Block Diagram



Product Specifications		
PART NO.:	VL378T2863A-D5M	REV: 1.0

Absolute Maximum Ratings					
Symbol	Parameter	MIN	MAX	Unit	
VDD	Voltage on VDD pin relative to VSS	-1.0	2.3		V
VDDQ	Voltage on VDDQ pin relative to VSS	-0.5	2.3		V
VDDL	Voltage on VDDL pin relative to VSS	-0.5	2.3		V
VIN, VOUT	Voltage on any pin relative to VSS	-0.5	2.3		V
TSTG	Storage temperature	-55	150		°C
IL	Input leakage current; Any input 0V<VIN<VDD; VREF input 0V<VIN<0.95V; Other pins not under test = 0V	Address, BA, RAS#, CAS#, WE#	-40	40	uA
		CS#, CKE, ODT	-40	40	uA
		CK0, CK0#	-10	10	uA
		CK1, CK1#, CK2, CK2#	-15	15	uA
		DM	-5	5	uA
IOZ	Output leakage current; 0V<VOUT<VDDQ; DQs and ODT are disabled	-5	5		uA
IVREF	VREF supply leakage current; VREF = Valid VREF level	-16	16		uA

DC Operating Conditions						
Symbol	Parameter	Min	Typical	Max	Unit	Notes
VDD	Supply voltage	1.7	1.8	1.9	V	1
VDDQ	I/O supply voltage	1.7	1.8	1.9	V	4
VDDL	VDDL supply voltage	1.7	1.8	1.9	V	4
VREF	I/O reference voltage	0.49 x VDDQ	0.50 x VDDQ	0.51 x VDDQ	V	2
VTT	I/O termination voltage	VREF-0.04	VREF	VREF+0.04	V	3

Note:

1. VDD, VDDQ must track each other. VDDQ must be less than or equal to VDD.
2. VREF is expected to equal VDDQ/2 of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on VREF may not exceed +/-1percent of the DC value. Peak-to-peak AC noise on VREF may not exceed +/-2 percent of VREF. This measurement is to be taken at the nearest VREF bypass capacitor.
3. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF and must track variations in the DC level of VREF.
4. VDDQ tracks with VDD; VDDL tracks with VDD.



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Operating Temperature Condition				
Symbol	Parameter	Rating	Units	Notes
TOPER	Operating temperature	0 - 85	°C	1,2
Notes: 1. Operating temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51-2. 2. At 0 – 85°C, operation temperature range, all DRAM specifications will be supported.				

Input DC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(DC)	Input High (Logic 1) Voltage	VREF + 0.125	VDDQ + 0.300	V
VIL(DC)	Input Low (Logic 0) Voltage	-0.300	VREF - 0.125	V

Input AC Logic Level				
All voltages referenced to VSS				
Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.250	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.250	V

Input/Output Capacitance				
TA=25°C, f=100MHz				
Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A13, BA0~BA2, RAS#, CAS#, WE#)	CIN1	12	20	pF
Input capacitance (CKE0, ODT0, CS0#)	CIN2	12	20	pF
Input capacitance (CK0, CK0#)	CIN3	6	8	pF
Input capacitance (CK1, CK1#, CK2, CK2#)	CIN3	7	10	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	6.5	8	pF

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IDD Specification

Condition	Symbol	-D5	Unit
Operating one bank active-pre-charge current; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD0*	560	mA
Operating one bank active-read-pre-charge current; $I_{OUT} = 0\text{mA}$; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RAS} = t_{RAS\ MIN(IDD)}$; $t_{RCD} = t_{RCD(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	IDD1*	760	mA
Pre-charge power-down current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2P**	56	mA
Pre-charge quiet standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	IDD2Q**	320	mA
Pre-charge standby current; All banks idle; $t_{CK} = t_{CK(IDD)}$; CKE is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are SWITCHING	IDD2N**	320	mA
Active power-down current; All banks open; $t_{CK} = t_{CK(IDD)}$; CKE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING.	Fast PDN Exit MRS(12) = 0	240	mA
	Slow PDN Exit MRS(12) = 1	80	mA
Active standby current; All banks open; $t_{CK} = t_{CK(IDD)}$; $t_{RP} = t_{RP(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD3N**	360	mA
Operating burst write current; All banks open; Continuous burst writes; BL = 8; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	IDD4W*	1000	mA
Operating burst read current; All banks open; Continuous burst reads; $I_{OUT} = 0\text{mA}$; BL = 4; CL = CL(IDD); AL = 0; $t_{CK} = t_{CK(IDD)}$; $t_{RAS} = t_{RAS\ MAX(IDD)}$; $t_{RP} = t_{RP(IDD)}$; CKE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W.	IDD4R*	1000	mA
Burst refresh current; $t_{CK} = t_{CK(IDD)}$; Refresh command at every $t_{RFC(IDD)}$ interval; CKE is HIGH; CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING.	IDD5**	1680	mA
Self refresh current; CK and CK# at 0V; CKE < 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING.	Normal	IDD6**	56
Operating bank interleave read current; All bank interleaving reads; $I_{OUT} = 0\text{mA}$; BL = 8; CL = CL(IDD); AL = $t_{RCD(IDD)} - 1 * t_{CK(IDD)}$; $t_{CK} = t_{CK(IDD)}$; $t_{RC} = t_{RC(IDD)}$; $t_{RRD} = t_{RRD(IDD)}$; $t_{RCD} = 1 * t_{CK(IDD)}$; CKE is HIGH; CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTs; Data bus inputs are SWITCHING.	IDD7*	2160	mA
Notes: IDD specification is based on Micron E-die components. *: Value calculated as one module rank in this operating condition, and all other module ranks in IDD2P (CKE LOW) mode. **: Value calculated reflects all module ranks in this operating condition.			



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AC TIMING PARAMETERS & SPECIFICATIONS					
Parameter	Symbol	DDR2-533 (-D5)		Unit	
		MIN	MAX		
Clock Timing					
Clock Cycle Time	CL4	$t_{CK(4)}$	3750	8000	ps
CK high-level width		$t_{CH(avg)}$	0.48	0.52	t_{CK}
CK low-level width		$t_{CL(avg)}$	0.48	0.52	t_{CK}
Half clock period		t_{HP}	MIN (t_{CH}, t_{CL})	-	ps
Clock jitter		t_{JIT}	-125	125	ps
Data Timing					
DQ output access time from CK/CK#		t_{AC}	-500	500	ps
Data-out high impedance window from CK/CK#		t_{HZ}	-	$t_{AC(MAX)}$	ps
Data-out low impedance window from CK/CK#		t_{LZ}	$t_{AC(MIN)}$	$t_{AC(MAX)}$	ps
DQ and DM input setup time relative to DQS		t_{DS}	100	-	ps
DQ and DM input hold time relative to DQS		t_{DH}	225	-	ps
DQ and DM input pulse width (for each input)		t_{DIPW}	0.35	-	t_{CK}
Data hold skew factor		t_{QHS}	-	400	ps
DQ-DQS hold, DQS to first DQ to go non-valid, per access		t_{QH}	$t_{HP} - t_{QHS}$	-	ps
Data valid output window (DVW)		t_{DVW}	$t_{QH} - t_{DQSQ}$	-	ns
Data Strobe Timing					
DQS input high pulse width		t_{DQSH}	0.35	-	t_{CK}
DQS input low pulse width		t_{DQSL}	0.35	-	t_{CK}
DQS output access time from CK/CK#		t_{DQSCK}	-450	450	ps
DQS failing edge to CK rising-setup time		t_{DSS}	0.2	-	t_{CK}
DQS failing edge from CK rising-hold time		t_{DSH}	0.2	-	t_{CK}
DQS-DQ skew, DQS to last DQ valid, per group, per access		t_{DQSQ}	-	300	ps
DQS read preamble		t_{RPRE}	0.9	1.1	t_{CK}
DQS read preamble		t_{RPST}	0.4	0.6	t_{CK}
DQS read preamble setup time		t_{WPRES}	0	-	ps
DQS read preamble		t_{WPRE}	0.25	-	t_{CK}
DQS read preamble		t_{WPST}	0.4	0.6	t_{CK}
Write command to first DQS latching transition		t_{DQSS}	-0.25	0.25	t_{CK}



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AC TIMING PARAMETERS & SPECIFICATIONS

Parameter	Symbol	DDR2-533 (-D5)		Unit
		MIN	MAX	
Command and Address Timing				
Address and control input pulse width for each input	t_{IPW}	0.6	-	t_{CK}
Address and control input setup time	t_{IS}	250	-	ps
Address and control input hold time	t_{IH}	375	-	ps
CAS# to CAS# command delay	t_{CCD}	2	-	ps
ACTIVE to ACTIVE (same bank) command	t_{RC}	55	-	ns
ACTIVE bank a to ACTIVE bank b command	t_{RRD}	7.5	-	ns
ACTIVE to READ or WRITE delay	t_{RCD}	15	-	ns
Four Bank Activate period	t_{FAW}	37.5	-	ns
ACTIVE to PRECHARGE command	t_{RAS}	40	70,000	ns
Internal READ to precharge Command delay	t_{RTP}	7.5	-	ns
Write recovery time	t_{WR}	15	-	ns
Auto precharge write recovery + precharge time	t_{DAL}	$t_{WR} - t_{RP}$	-	ns
Internal WRITE to READ Command delay	t_{WTR}	7.5	-	ns
PRECHARGE command period	t_{RP}	15	-	ns
PRECHARGE ALL command period	t_{RPA}	$t_{RP} + t_{CK}$	-	ns
LOAD MODE command cycle time	t_{MRD}	2	-	t_{CK}
CKE low to CK, CK# uncertainty	t_{DELAY}	$t_{IS} + t_{CK} + t_{IH}$	-	ns
Self Refresh				
Refresh to Active or Refresh to Refresh command interval	t_{RFC}	127.5	-	ns
Average periodic Refresh interval	t_{REFI}	-	7.8	us
Exit Self Refresh to non-READ command	t_{XSNR}	$t_{RFC} + 10$	-	ns
Exit Self Refresh to READ	t_{XSRD}	200	-	t_{CK}
Exit Self Refresh timing reference	t_{ISXR}	t_{IS}	-	ps
ODT				
ODT turn-on delay	t_{AOND}	2	2	t_{CK}
ODT turn-on	t_{AON}	$t_{AC(MIN)}$	$t_{AC(MAX)} + 1000$	ps
ODT turn-off delay	t_{AOFD}	2.5	2.5	t_{CK}
ODT turn-off	t_{AOF}	$t_{AC(MIN)}$	$t_{AC(MAX)} + 600$	ps
ODT turn-on(power-down mode)	t_{AONPD}	$t_{AC(MIN)} + 2000$	$2 * t_{CK(AVG)} + t_{AC(MAX)} + 1000$	ps
ODT turn-off (power-down mode)	t_{AOFPD}	$t_{AC(MIN)} + 2000$	$2.5 * t_{CK(AVG)} + t_{AC(MAX)} + 1000$	ps
ODT to power-down entry latency	t_{ANPD}	3	-	t_{CK}
ODT power-down exit latency	t_{AXPD}	8	-	t_{CK}
Power Down				
Exit active power-down to READ command, MR[bit12=0]	t_{XARD}	2	-	t_{CK}
Exit active power-down to READ command, MR[bit12=1]	t_{XARDS}	6 - AL	-	t_{CK}
Exit precharge power-down to any non-READ command	t_{XP}	2	-	t_{CK}
CKE minimum high/low time	t_{CKE}	3	-	t_{CK}



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Revision History:

Date	Rev.	Page	Changes
09/28/09	1.0	All	Spec release