Product Specifications		
PART NO.:	**VL368L3223E-B3S**	**REV: 1.0**

General Information

256MB 32Mx64 DDR SDRAM NON-ECC UNBUFFERED DIMM 184-PIN

Description

The VL368L3223E is a 32Mx64 Double Data Rate SDRAM high density DIMM. This memory module is single rank, consists of eight CMOS 32Mx8 bits with 4 banks Synchronous DRAMs in TSOP-II packages and a 2K EEPROM in an 8-pin TSSOP package. This module is a 184-pin dual in-line memory module and is intended for mounting into an edge connector socket. Decoupling capacitors are mounted on the printed circuit board for each DDR SDRAM.

Features

- 184-pin, dual in-line memory module (DIMM)
- Two data transfers per clock cycle
- VDD = VDDQ = 2.5V +/-0.2V for DDR333
- JEDEC standard 2.5V I/O (SSTL_2 compatible)
- VDDSPD = 2.3V to 3.6V
- Bi-directional data-strobe (DQS)
- Differential clock inputs (CK and CK#)
- DLL aligns DQ and DQS transition with CK transition
- Programmable read latency: DDR333 (2.5 clock)
- Programmable burst; length (2, 4, 8)
- Programmable burst (sequential & interleave)
- Auto & Self refresh, 7.8us refresh interval (8K/64ms refresh)
- Serial presence detect (SPD) with EEPROM
- Lead-free, RoHS compliant
- JEDEC pinout
- Gold edge contacts
- PCB: Height 28.57mm (1.125”), double sided component
- Ambient operating temperature (T_A): - Commercial ($0^oC <= T_A <= 70^oC$)
  - Industrial ($-40^oC <= T_A <= +85^oC$)

Pin Description

Pin Name	Function
A0~A12	Address Inputs
BA0~BA1	Bank Address Inputs
DQ0~DQ63	Data Input/Output
DQS0~DQS7	Data Strobes Input/Output
DM0-DM7	Data Mask
CK0, CK0#~ CK2, CK2#	Clock Input
CKE0	Clock Enables Input
CS0#	Chip Selects Input
RAS#	Row Address Strobes
CAS#	Column Address Strobes
WE#	Write Enable
VDD	Voltage Supply
VDDQ	Voltage Supply for DQS
VSS	Ground
VREF	Power Supply Reference
VDDSPD	SPD Voltage Supply
SA0~SA2	SPD Address
SDA	SPD Data Input/Output
SCL	SPD Clock Input
NC	No Connect

Order Information:

VL368L3223E - B3 S X - X

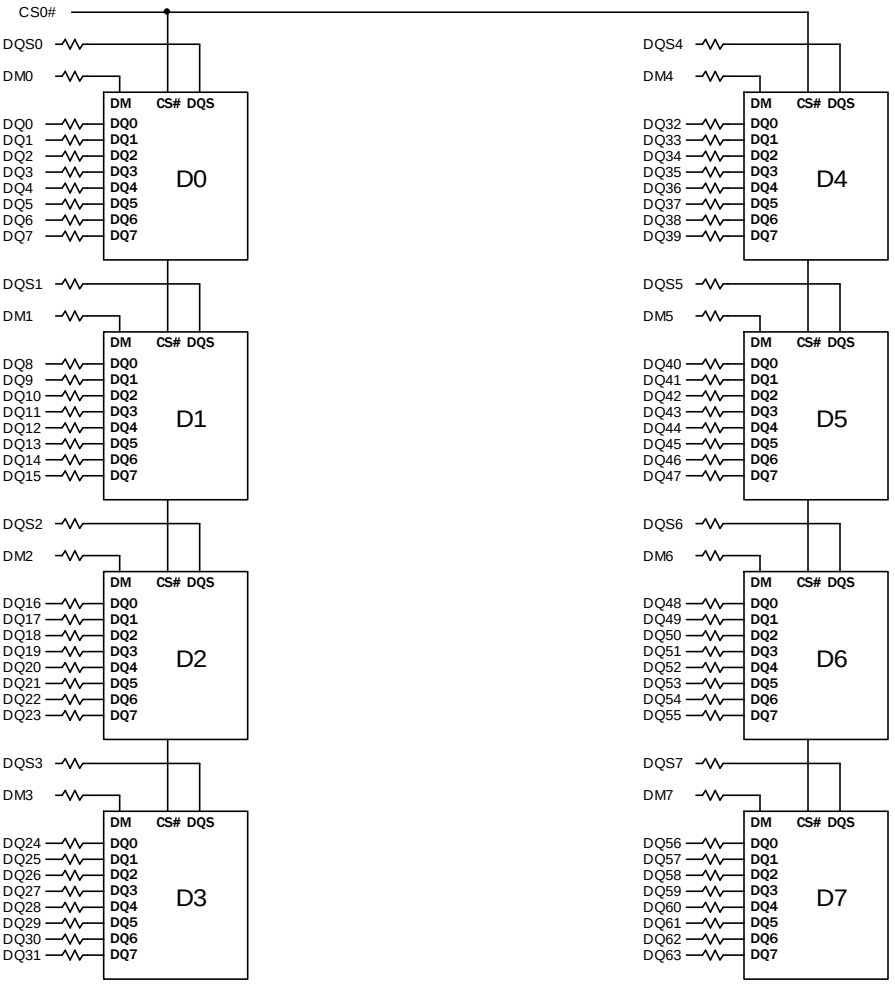
- OPERATING TEMPERATURE
  None: Commercial
  I: Industrial
- DRAM DIE (Option)
- DRAM MANUFACTURER
  S - SAMSUNG
- MODULE SPEED
  B3: PC2700 @CL2.5
- VL: Lead-free/RoHS

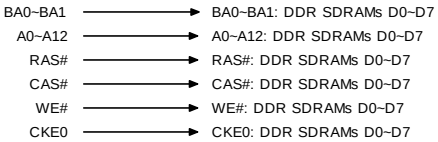
Pin Configuration

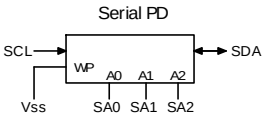
184-PIN DDR DIMM FRONT								184-PIN DDR DIMM BACK							
Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name	Pin	Name
1	VREF	24	DQ17	47	DQS8	70	VDD	93	VSS	116	VSS	139	VSS	162	DQ47
2	DQ0	25	DQS2	48	A0	71	NC	94	DQ4	117	DQ21	140	DM8*	163	NC
3	VSS	26	VSS	49	CB2*	72	DQ48	95	DQ5	118	A11	141	A10	164	VDDQ
4	DQ1	27	A9	50	VSS	73	DQ49	96	VDDQ	119	DM2	142	CB6*	165	DQ52
5	DQS0	28	DQ18	51	CB3*	74	VSS	97	DM0	120	VDD	143	VDDQ	166	DQ53
6	DQ2	29	A7	52	BA1	75	CK2#	98	DQ6	121	DQ22	144	CB7*	167	A13*
7	VDD	30	VDDQ	53	DQ32	76	CK2	99	DQ7	122	A8	145	VSS	168	VDD
8	DQ3	31	DQ19	54	VDDQ	77	VDDQ	100	VSS	123	DQ23	146	DQ36	169	DM6
9	NC	32	A5	55	DQ33	78	DQS6	101	NC	124	VSS	147	DQ37	170	DQ54
10	RESET#*	33	DQ24	56	DQS4	79	DQ50	102	NC	125	A6	148	VDD	171	Q55
11	VSS	34	vss	57	DQ34	80	DQ51	103	NC	126	DQ28	149	DM4	172	VDDQ
12	DQ8	35	DQ25	58	VSS	81	VSS	104	VDDQ	127	DQ29	150	DQ38	173	NC
13	DQ9	36	DQS3	59	BA0	82	NC	105	DQ12	128	DDQ	151	DQ39	174	DQ60
14	DQS1	37	A4	60	DQ35	83	DQ56	106	DQ13	129	DM3	152	VSS	175	DQ61
15	VDDQ	38	VDD	61	DQ40	84	DQ57	107	DM1	130	A3	153	DQ44	176	VSS
16	CK1	39	DQ26	62	VDDQ	85	VDD	108	VDD	131	DQ30	154	RAS#	177	DM7
17	CK1#	40	DQ27	63	WE#	86	DQS7	109	DQ14	132	VSS	155	DQ45	178	DQ62
18	VSS	41	A2	64	DQ41	87	DQ58	110	DQ15	133	DQ31	156	VDDQ	179	DQ63
19	DQ10	42	VSS	65	CAS#	88	DQ59	111	CKE1*	134	CB4*	157	CS0#	180	VDDQ
20	DQ11	43	A1	66	VSS	89	VSS	112	VDDQ	135	CB5*	158	CS1#*	181	SA0
21	CKE0	44	CB0*	67	DQS5	90	NC	113	NC	136	VDDQ	159	DM5	182	SA1
22	VDDQ	45	CB1*	68	DQ42	91	SDA	114	DQ20	137	CK0	160	VSS	183	SA2
23	DQ16	46	VDD	69	DQ43	92	SCL	115	A12	138	CK0#	161	DQ46	184	VDDSPD

Note: *: These pins are not used on this module.

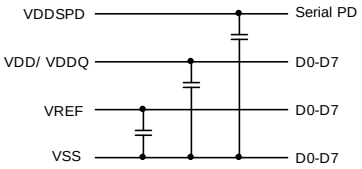
Function Block Diagram







Clock Wiring	
Clock Input	DDR SDRAMs
CK0, CK0#	02 SDRAMs
CK1, CK1#	02 SDRAMs
CK2, CK2#	03 SDRAMs



Notes:

1. Unless otherwise noted, resistor values are 22 ohms +/-5%

Absolute Maximum Ratings

Symbol	Parameter		Value	Unit
VIN, VOUT	Voltage on any pin relative to VSS		-0.5 ~ 3.6	V
VDD, VDDQ	Voltage on VDD & VDDQ supply relative to VSS		-1.0 ~ 3.6	V
TSTG	Storage temperature		-55 ~ +150	^{0}C
TA	Operating temperature	Commercial	0 ~ 70	^{0}C
		Industrial	-40 ~ +85	
PD	Power dissipation		8	W
IOS	Short circuit current		50	mA

Notes:

Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

DC Operating Conditions

All voltages referenced to VSS
TA = 0^{0}C to 70^{0}C

Symbol	Parameter		Min	Max	Unit	Note
VDD	Supply voltage		2.3	2.7	V	
VDDQ	I/O Supply voltage		2.3	2.7	V	
VREF	I/O Reference voltage		0.49 * VDDQ	0.51 * VDDQ	V	1
VTT	I/O Termination voltage		VREF-0.04	VREF+0.04	V	2
VIH(DC)	Input logic high voltage		VREF+0.15	VDDQ+0.30	V	
VIL(DC)	Input logic low voltage		-0.3	VREF-0.15	V	
VIN(DC)	Input voltage level, CK and CK#		-0.3	VDDQ+0.30	V	
VID(DC)	Input differential voltage, CK and CK#		0.3	VDDQ+0.60	V	3
VIX(DC)	Input crossing point voltage, CK and CK#		0.3	VDDQ+0.60	V	
II	Input leakage current	Address, CAS#,RAS#,WE#	-16	16	uA	
		CS#,CKE	-16	16	uA	
		CK, CK#	-6	6	uA	
		DM	-2	2	uA	
IOZ	Output leakage current		-5	5	uA	
IOH	Output high current(normal strength) VOUT = v + 0.84V		-16.8	-	mA	
IOL	Output high current(normal strength) VOUT = VTT - 0.84V		16.8	-	mA	
IOH	Output high current(half strength) VOUT = VTT + 0.45V		-9	-	mA	
IOL	Output high current(half strength) VOUT = VTT - 0.45V		9	-	mA	

Notes:
1. VREF is expected to be equal to 0.5*VDDQ of the transmitting device, and to track variations in the DC level of the same. Peak to peak noise on VREF may not exceed +/- 2% of the DC value.
2. VTT is not applied directly to the device. VTT is a system supply for signal termination resistors, is expected to be set equal to VREF, and must track variations in the DC level of VREF.
3. VID is the magnitude of the difference between the input level on CK and the input level of CK#.

AC Operating Conditions

All voltages referenced to VSS
TA = 0°C to 70°C

Symbol	Parameter	Min	Max	Unit
VIH(AC)	Input High (Logic 1) Voltage	VREF + 0.31	-	V
VIL(AC)	Input Low (Logic 0) Voltage	-	VREF - 0.31	V
VID(AC)	Input Differential Voltage, CK and CK# inputs	0.70	VDDQ + 0.60	V
VIX(AC)	Input Crossing Point Voltage, CK and CK# inputs	0.5*VDDQ - 0.2	0.5*VDDQ + 0.2	V

Input/Output Capacitance

TA=25°C, f=100MHz

Parameter	Symbol	Min	Max	Unit
Input capacitance (A0~A12, BA0~BA1, RAS#, CAS#, WE#)	CIN1	20	28	pF
Input capacitance (CKE0)	CIN2	20	28	pF
Input capacitance (CS0 #)	CIN3	20	28	pF
Input capacitance (CK0, CK0# ~ CK2, CK2#)	CIN4	10	13	pF
Input/Output capacitance (DQ, DQS, DQS#, DM)	CIO	8	9	pF

IDD Specification

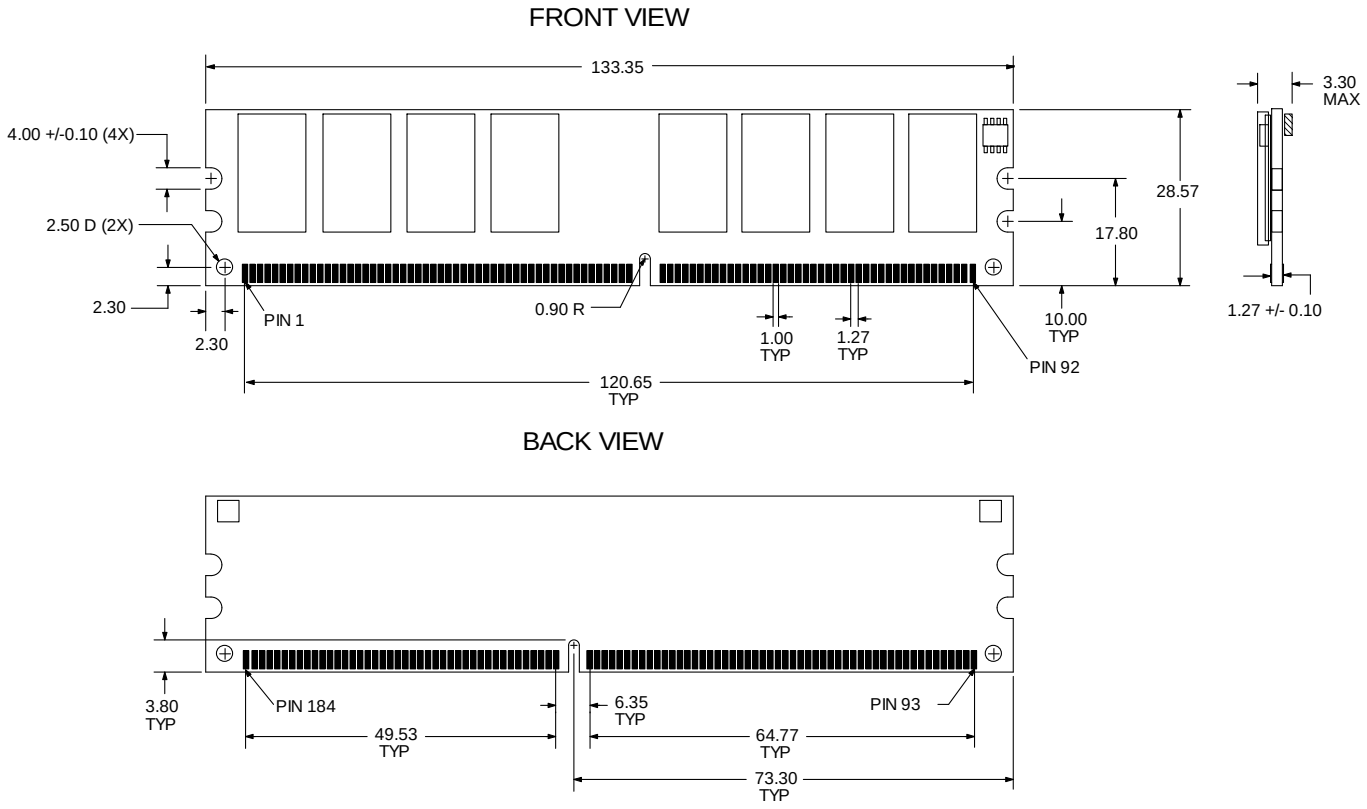
Condition	Symbol	B3 (DDR333)	Unit
OPERATING CURRENT: One device bank active; Active-Precharge; tRC=tRC(MIN); tCK=tCK(MIN); DQ,DM and DQS inputs change once per clock cycle; Address and control inputs change once every two clock cycles	IDD0*	360	mA
OPERATING CURRENT: One device bank; Active-Read-Precharge; BL=4; tRC=tRC(MIN); tCK=tCK(MIN); IOUT =0mA; Address and control inputs change once per clock cycle	IDD1*	400	mA
PRECHARGE POWER-DOWN STANDBY CURRENT: All device banks are idle; Power-down mode; tCK=tCK(MIN); CKE=LOW	IDD2P**	24	mA
IDLE STANDBY CURRENT: CS#=HIGH; All device banks are idle; tCK=tCK(MIN); CKE=HIGH; Address and other control inputs changing once per clock cycle. VIN =VREF for DQ,DQS and DM	IDD2F**	160	mA
ACITVE POWER-DOWN STANDBY CURRENT: One device bank active; Power-down mode; tCK=tCK(MIN); CKE=LOW	IDD3P**	80	mA
ACTIVE STANDBY CURRENT: CS#=HIGH; CKE=HIGH; One device bank active; tRC =tRAS(MAX); tCK=tCK(MIN); DQ, DM and DQS inputs change twice per clock cycle; Address and other control inputs changing once per clock cycle	IDD3N**	200	mA
OPERATING CURRENT: Burst = 2; Reads; Continnuous burst; One device bank active; Address and other control inputs changing once per clock cycle; tCK=tCK(MIN); IOUT=0mA	IDD4R*	600	mA
OPERATING CURRENT: Burst = 2; Writes; Continnuous burst; One device bank active; Address and other control inputs changing once per clock cycle; tCK=tCK(MIN); DQ, DM and DQS inputs change twice per clock cycle	IDD4W*	520	mA
AUTO REFRESH CURRENT: tRC=tRFC(MIN)	IDD5**	600	mA
SELF-REFRESH CURRENT: CKE< 0.2V	IDD6**	24	mA
OPERATING CURRENT: Four device bank interleaving Reads Burst=4 with auto precharge; tRC=tRC(MIN); tCK=tCK(MIN); Address and control inputs change only during Active READ, or WRITE commands	IDD7*	880	mA

Notes:
IDD specification is based on Samsung N-die components. Other manufacturers' DRAMs may have different values.
*: Value calculated as one module rank in this operation condition, and other module rank in IDD2P (CKE LOW) mode.
**: Value calculated as all module ranks in this operation condition.

AC Timing Parameters & Specifications

Parameter		Symbol	B3 (DDR333)		Unit
			MIN	MAX	
Row Cycle Time		tRC	60	-	ns
Refresh row cycle time		tRFC	72	-	ns
Row active		tRAS	42	70,000	ns
RAS# to CAS# delay		tRCD	18	-	ns
Row precharge time		tRP	18	-	ns
Row active to row active delay		tRRD	12	-	ns
Write recovery time		tWR	15	-	ns
Last data in to READ command		tWTR	1	-	tCK
Clock cycle time	CL=2	tCK	-	-	ns
	CL=2.5		6	12	ns
	CL=3		-	-	ns
Clock high level width		tCH	0.45	0.55	tCK
Clock low level width		tCL	0.45	0.55	tCK
DQS-out access time from CK/CK#		tDQSCK	-0.6	+0.6	ns
Output data access time from CK/CK#		tAC	-0.7	+0.7	ns
Data strobe edge to output data edge		tDQSQ	-	0.40	ns
Read preamble		tRPRE	0.9	1.1	tCK
Read postamble		tRPST	0.4	0.6	tCK
CK to valid DQS-in		tDQSS	0.75	1.25	tCK
DQS-in setup time		tWPRES	0	-	ns
DQS-in hold time		tWPRE	0.25	-	tCK
DQS falling edge to CK rising-setup time		tDSS	0.2	-	tCK
DQS falling edge to CK rising-hold time		tDSH	0.2	-	tCK
DQS-in high level width		tDQSH	0.35	-	tCK
DQS-in low level width		TDQSL	0.35	-	tCK
Address and control input setup time (fast)		tISF	0.75	-	ns
Address and control input hold time (fast)		tIHF	0.75	-	ns
Address and control input setup time (slow)		tISS	0.8	-	ns
Address and control input hold time (slow)		tIHS	0.8	-	ns
Data-out high impedance time from CK/CK#		tHZ	-0.7	+0.7	ns
Data-out low impedance time from CK/CK#		tLZ	-0.7	+0.7	ns
Mode regigster set cycle		tMRD	12	-	ns
DQ & DM setup time to DQS		tDS	0.45	-	ns
DQ & DM hold time to DQS		tDH	0.45	-	ns
Control & address input pulse width		tIPW	2.2	-	ns
DQ & DM input pulse width		tDIPW	1.75	-	ns
Exit self refresh to non-Read command		tXSNR	75	-	ns
Exit self refresh to Read command		tXSRD	200	-	tCK
Refresh interval time		tREFI		7.8	us
Output DQS valid window		tQH	tHP-tQHS	-	ns
Clock half period		tHP	tCLmin or tCHmin	-	ns
Data hold skew factor		tQHS		0.5	ns
DQS write postamble		tWPST	0.4	0.6	tCK
Active Read with auto precharge command		tRAP	18	-	ns
Auto precharge Write recovery + Precharge time		tDAL	tWR/tCK + tRP/tCK	-	tCK

Package Dimensions



Note: 1. All dimensions are in millimeters with tolerance +/- 0.15mm unless otherwise specified.
2. The dimensional diagram is for reference only.

Revision History:

Date	Rev.	Page	Changes
03/16/2011	1.0	All	Spec release